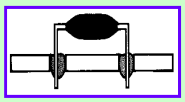
國立清華大學電機系

EE-6250
超大型積體電路測試
VLSI Testing

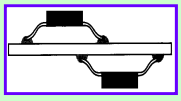
Chapter 9
Boundary Scan

Objectives

- Standards for board level testing
- Used for
  - Chips
  - Chip interconnections
  - Modules
  - Modules interconnections
  - Subsystems
  - Systems
  - Multi-chip modules
    - Die-to-board integration

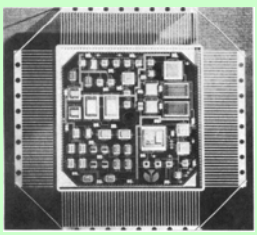


Through-hole mounting

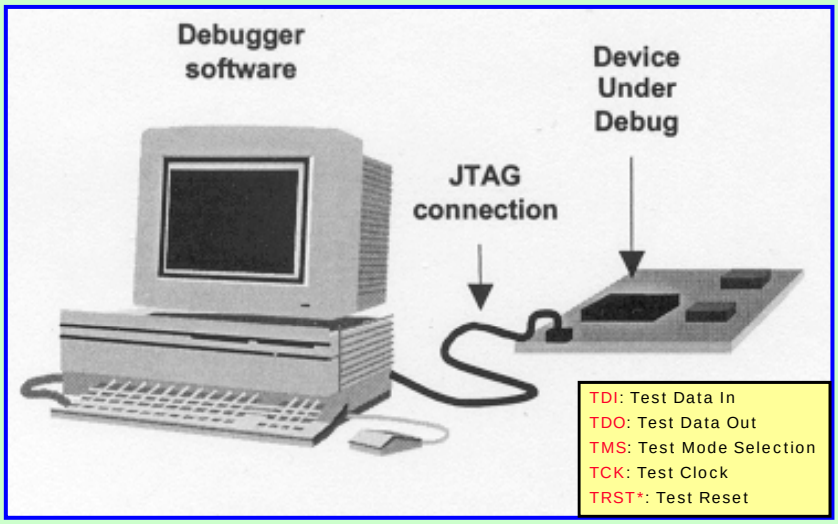


Surface mount

53 ICs + 40 discrete devices



Board Testing Setup



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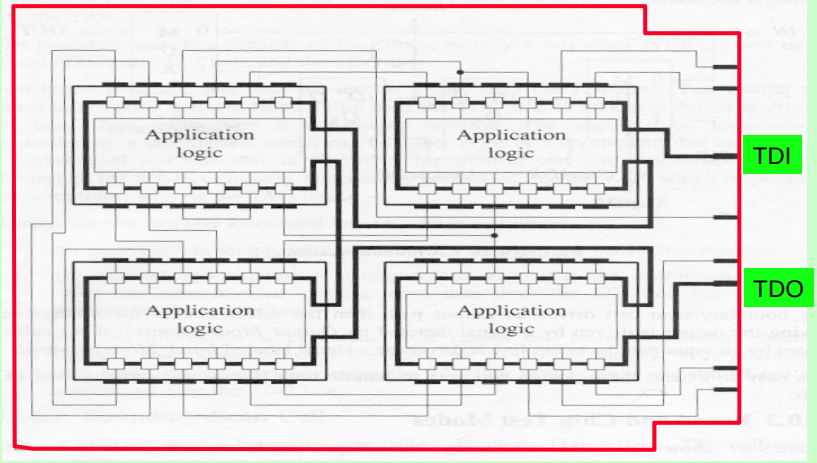
A Printed Circuit Board with Boundary Scan

Boundary scan use 4 or 5 wire bus to provide accessibility to the I/O pins of selected on-board IC → thereby facilitating board-level testing



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History

- **1985**
  - Joint European Test Action Group (JETAG, Philips)
- **1986**
  - VHSIC Element-Test & Maintenance (ETM) bus standard (IBM et al.)
  - VHSIC Test & Maintenance TM Bus Structure (IBM et al.)
- **1988**
  - Joint Test Action Group (JTAG) proposed Boundary Scan Standard
- **1990**
  - Boundary Scan approved as IEEE Std. 1149.1-1990
  - Boundary Scan Description Language (BSDL) proposed by HP
- **1993**
  - 1149.1a –1993 approved to replace 1149.1-1990
- **1994**
  - 1149.1b BSDL approved
- **1995**
  - 1149.5 approved

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Overview of P1149 Family

Number	Title	Status
1149.1	Testing of digital chips and Interconnections between Chips	Std. 1149.1-1990 Std. 1149.1a-1993 Std. 1149.1b-1994 (BSDL)
1149.2	Extended Digital Serial Interface	Near Completion
1149.3	Direct Access Testability Interface	Discontinue
1149.4	Mixed-Signal Test Bus	Started Nov. 1991
1149.5	Standard Module Test and Maintenance (MTM) Bus Protocol	Std. 1149.5-1995
1149	Unification	Not yet started

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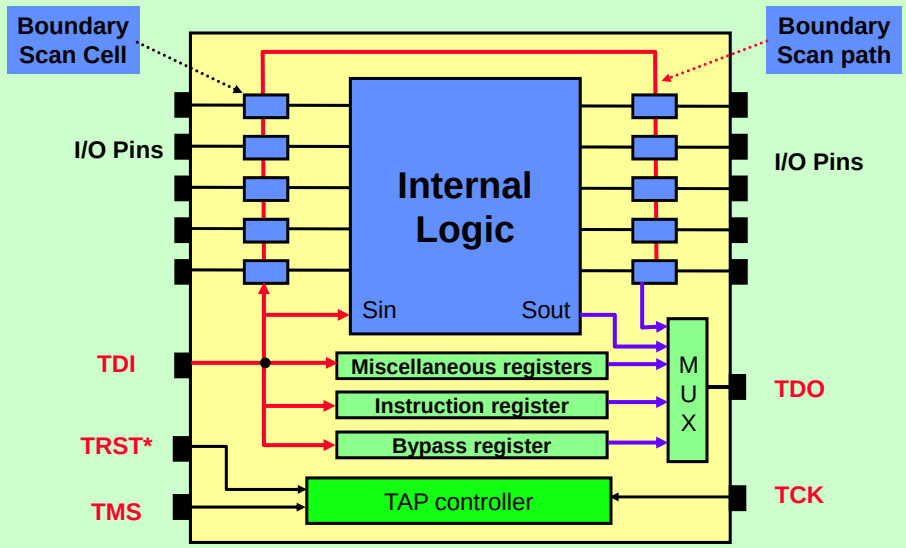
Basic Chip Architecture of 1149.1



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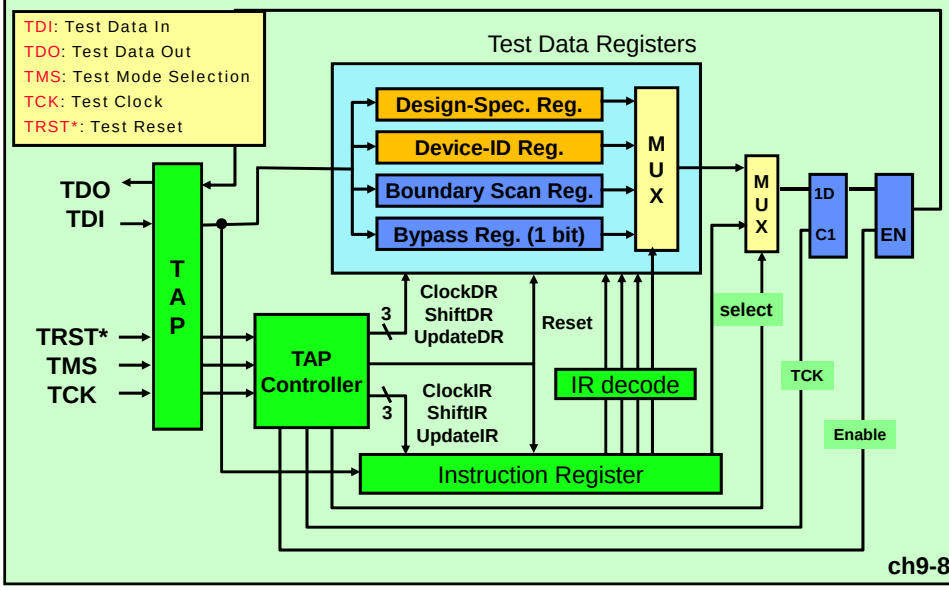
Boundary Scan Circuitry in a Chip



ch9-8

Hardware Components of 1149.1

- TAP (Test Access Port)
  - TMS, TCK, TDI, TDO, TRST* (optional)
- TAP Controller
  - A finite state machine with 16 states
  - Input: TCK, TMS
  - Output: 9 or 10 signals including ClockDR, UpdateDR, shiftDR, ClockIR, UpdateIR, ShiftIR, Select, Enable, TCK, and the optional TRST*
- IR (Instruction Register)
- TDR (Test Data Register)
  - Mandatory: boundary scan register and bypass register
  - Optional: device-ID register, design-specific registers, etc.

ch9-9

Bus Protocol

Serially send instruction over TDI into instruction register

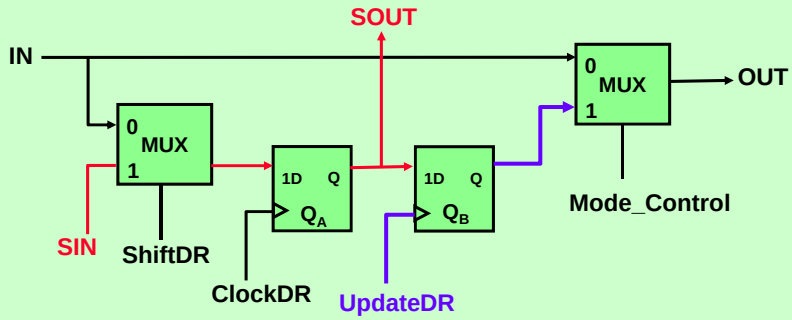
Test circuitry is configured To respond to instruction (Scan in data through TDI)

Execute test instruction

Shift out test results through TDO
New test data on TDI can be shifted in simultaneously

ch9-10

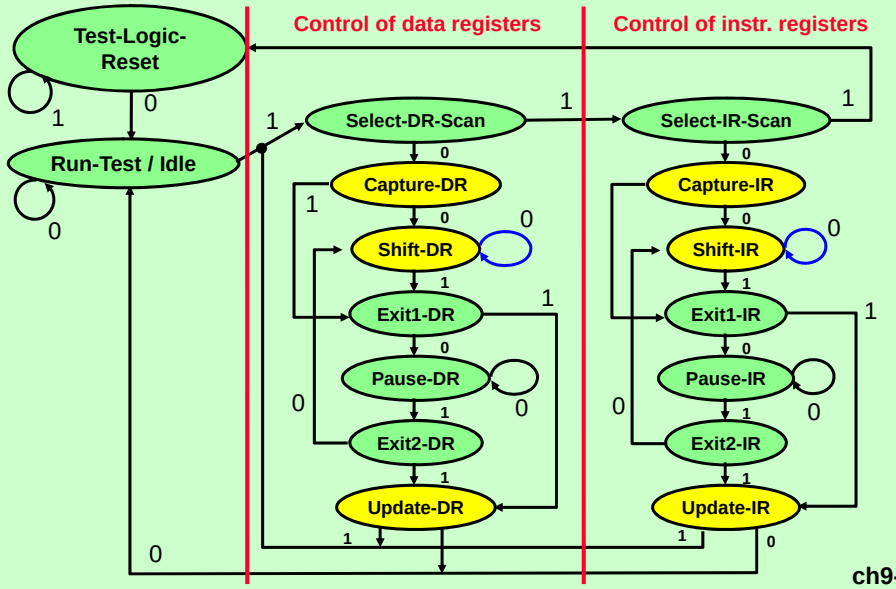
A Typical Boundary Scan Cell



- Operation Modes
  - Normal: Mode_control=0; IN→OUT
  - Scan: ShiftDR=1, ClockDR; TDI→...→SIN→SOUT→...→TDO
  - 捕 Capture: ShiftDR=0, ClockDR; IN→Q_A, OUT driven by IN or Q_B
  - 投 Update: Mode_Control=1, UpdateDR; Q_B→OUT

ch9-11

State Diagram of TAP Controller



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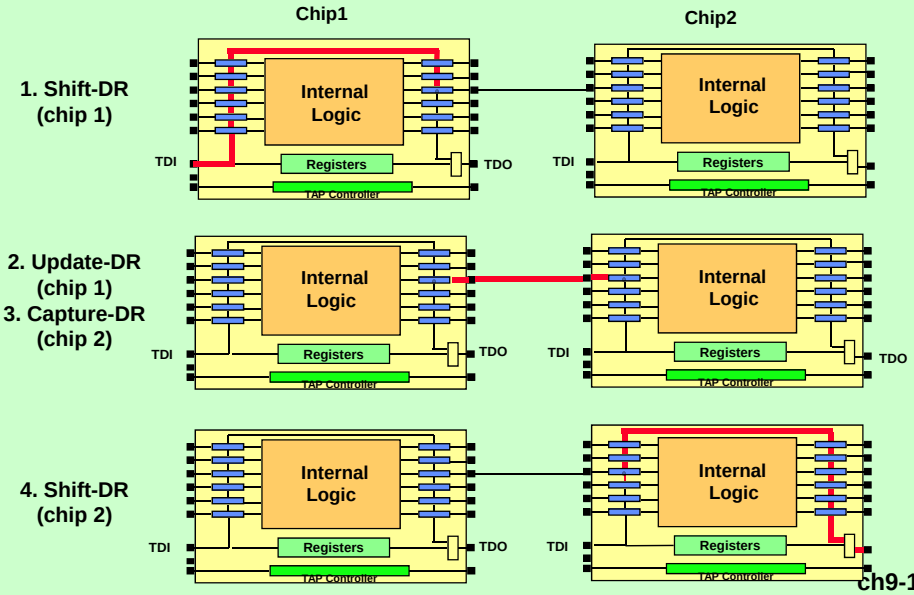
States of TAP Controller

- Test-Logic-Reset: normal mode
- Run-Test/Idle: wait for internal test such as BIST
- Select-DR-Scan: initiate a data-scan sequence
- Capture-DR: load test data in parallel
- Shift-DR: load test data in series
- Exit1-DR: Finish phase-1 shifting of data
- Pause-DR: Temporarily hold the scan operation (allow the bus master to reload data)
- Exit2-DR: finish phase-2 shifting of data
- Update-DR: parallel load from associated shift registers

Instruction Set

- EXTEST
  - Test Interconnection between chips and board
- SAMPLE/PRELOAD
  - Sample and shift out data or shift data only
- BYPASS
  - Bypass data through a chip
- Optional
  - Intest, RunBist, CLAMP, Idcode, usercode, High-Z, etc.

EXTEST



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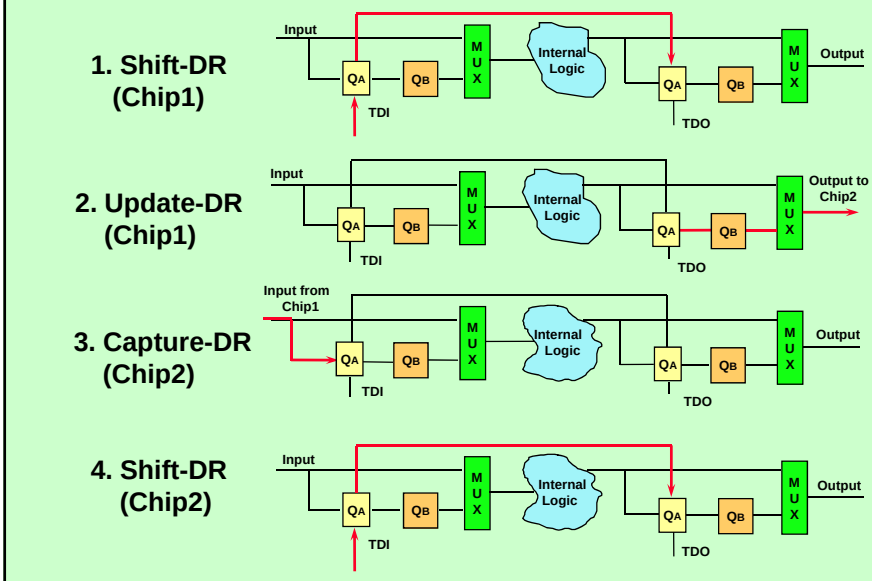
EXTEST



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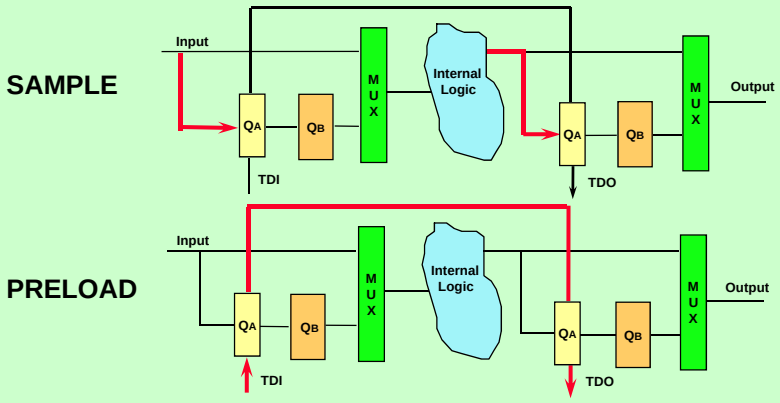
SAMPLE/PRELOAD



Sample/Preload is one instruction that allows

1. **Sample and shift (out) or**
2. **Shift (in) only**

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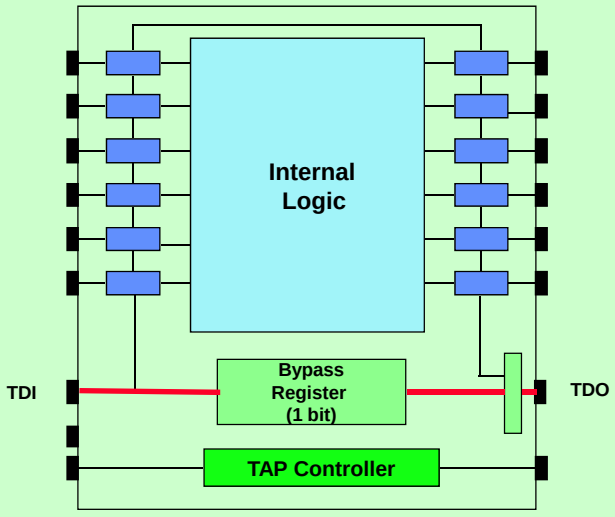
BYPASS



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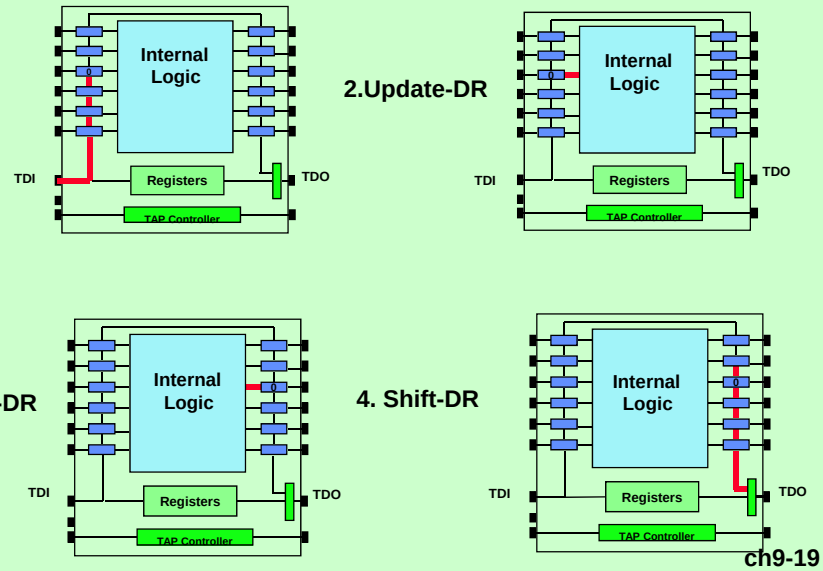
INTEST



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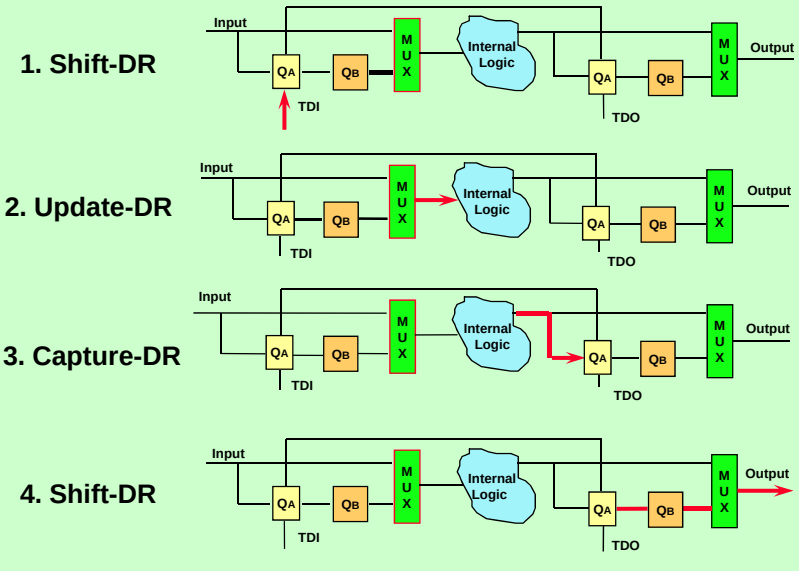
INTEST



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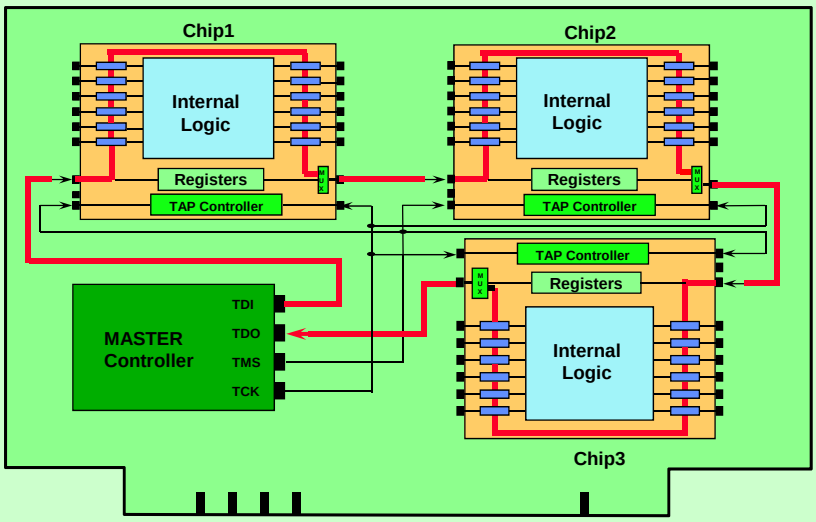
A Printed Circuit Board With 1149.1
(Ring configuration, test controller on board)



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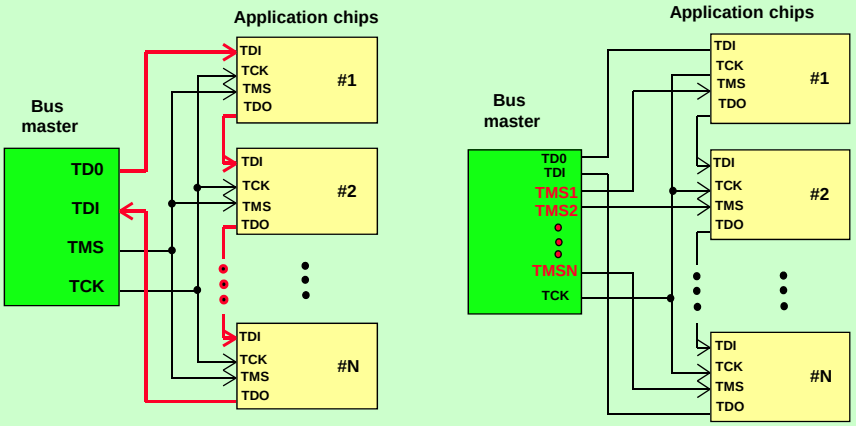
Test Bus Configuration



Ring configuration **Star configuration**

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