Chapter 6

Delay Testing

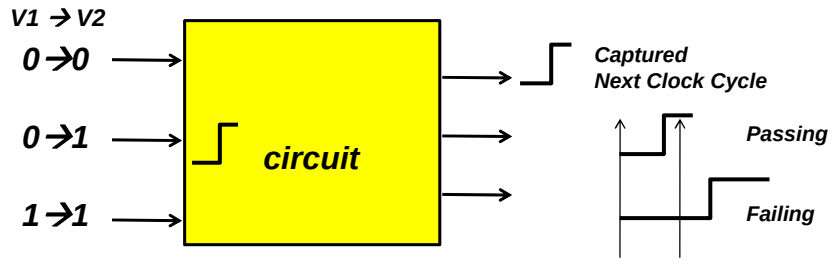
Acknowledgements:
Mainly based on the lecture notes of
"VLSI Test Principles and Architectures"

Introduction of Delay Testing

- **Delay Faulty:**
  - **Fault that cause delay across a circuit to violate certain timing constraint**
- **Delay Fault Models:**
  - **Path delay fault**
    - **Too much delay along a path**
  - **Transition fault (or Gate delay fault)**
    - **Too much delay across a particular gate**

Basic Delay Testing

- **Delay Test Pattern:**
  - A two-pattern test: <v1, v2>
  - v1 is an initialization vector
  - v2 causes the fault to be detected



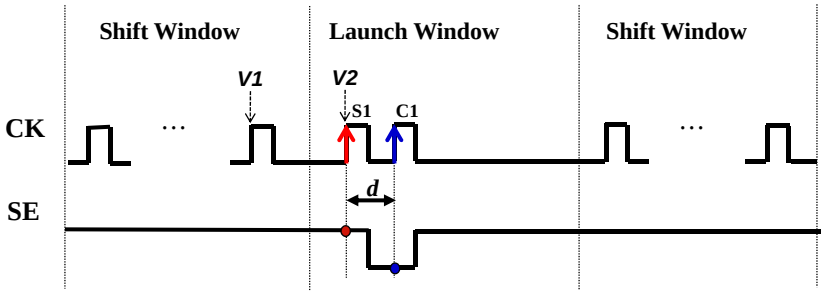
Challenge: The launch time and capture time are just away by a high-speed clock cycle time

Applications of Delay Tests

- **Launch-off shifting (LOS)**
  - Aka (also known as) skewed-load
  - v1 is arbitrary, v2 is derived by a 1-bit shift of v1
- **Launch-off capture (LOC)**
  - Aka broadside or double-capture
  - v1 is arbitrary, v2 is derived from v1 through the circuit function

Timing Sequence of Launch-off-Shifting

PROS: Easier Test Generation to achieve a Higher Fault Coverage
CONS: Hard to produce the Scan-Enable signal 'SE'
(Note: 'SE' has to go LOW between S1 and C1)



S1 is a shifting cycle
C1 is a capture cycle
d is the fast clock cycle time

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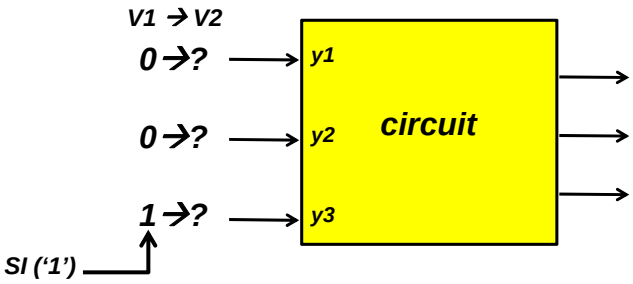
Example of LOS

Question:

v1 is {y1='0', y2='0', y3='1'}
What is vector v2 if using LOS?
Assuming scan chain order y3→y2→y1



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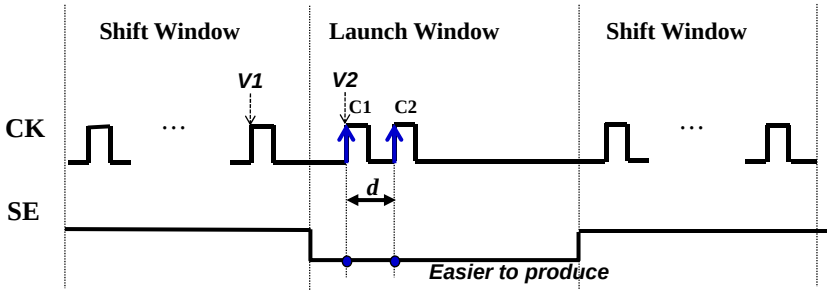
Timing Sequence of Launch-off-Capture

PROS: Scan-Enable signal 'SE' to easy to produce
CONS: Fault Coverage is Lower than LOS



C1 is a capture cycle
C2 is a capture cycle, too
***d* is the fast clock cycle time**

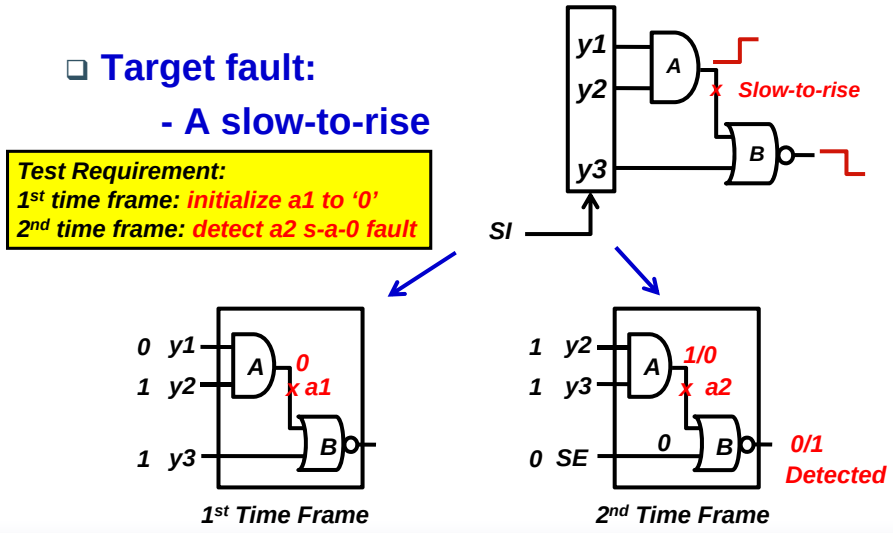
Transition Fault Model

- **Assumption:**
  - a large/gross delay is present at a circuit node
- **Path independence:**
  - Irrespective of which path the effect is propagated, the gross delay defect will be arriving late at an observable point
- **De-facto standard in Industry**
  - Simple and the number of faults is linear to circuit size
  - Also needs 2 vectors to test a fault
- **Formulation of transition-fault test generation:**
  - Node x slow-to-rise (x-STR) can be modeled simply as two stuck-at faults
  - (1) First time-frame: x/1 needs to be excited
  - (2) Second time-frame: x/0 needs to be excited and propagated

Ex: LOS Pattern Generation

- **Target fault:**
  - **A slow-to-rise**

Test Requirement:
1st time frame: initialize a1 to '0'
2nd time frame: detect a2 s-a-0 fault

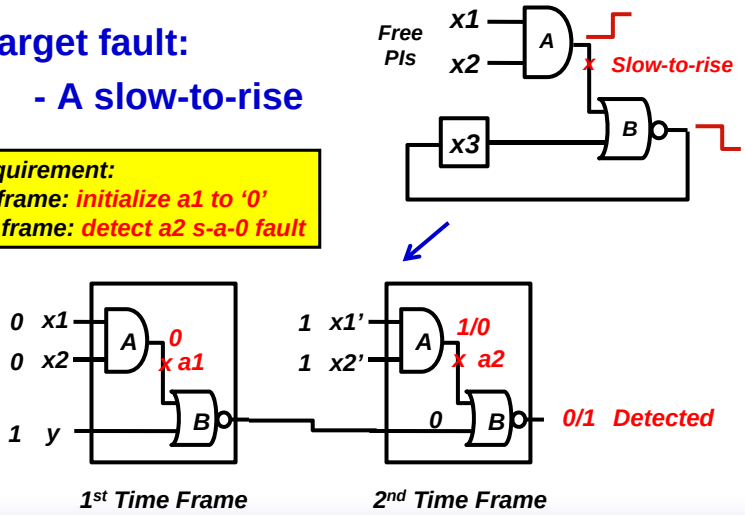


Final 1st Pattern: (y1, y2, y3, SE) = (0, 1, 1, 0) → Shifted to become 2nd Pattern

Ex: LOC Pattern Generation

- **Target fault:**
  - **A slow-to-rise**

Test Requirement:
1st time frame: initialize a1 to '0'
2nd time frame: detect a2 s-a-0 fault



Summary

- More and more ICs require delay testing (or called timing testing, performance testing), to ensure that an IC can perform up to its target speed.
- Better understand what LOS, LOC means, since It's industrial practice.
- Some IC, e.g., CPU, needs to go through speed binning process, to determine the "quality bin" of each IC and its sell price.
- Delay test is still a tough issue and still evolving. Rigorous delay testing also aims to detect "small defects" so as to reduce the test escape of latent defects that might hurt an IC's reliability in its field.