國立清華大學電機系

EE-6250
超大型積體電路測試
VLSI Testing

Chapter 10
High-Speed Interconnect Testing

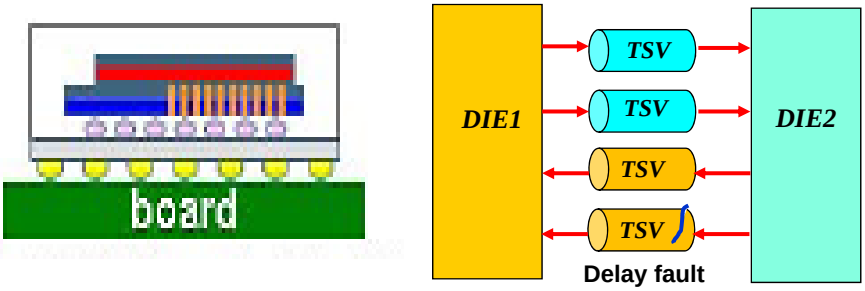
Outline

- Introduction
  - Problem, Objective, Review, and Motivation
- Pulse-Vanishing Test (PV-Test)
- VOT-Based Oscillation Test

Testing Interconnects in 3D IC

Problem Addressed:

To develop a low-cost method to test the delay fault associated with the TSV (Through Silicon Via)



3D-IC using TSVs

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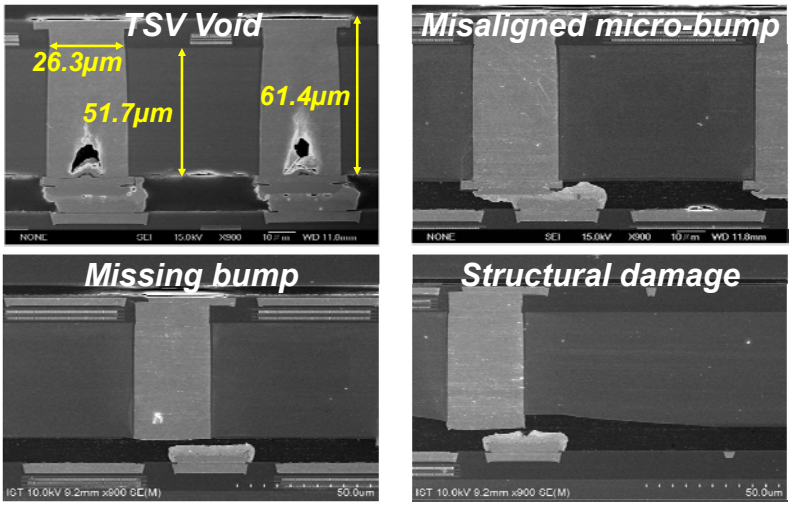
SEM Photos of TSV Defects (0.18um Through Silicon Stacking at ITRI)

A partially faulty TSV may not operate as fast as we expect (and it could deteriorate over time…)



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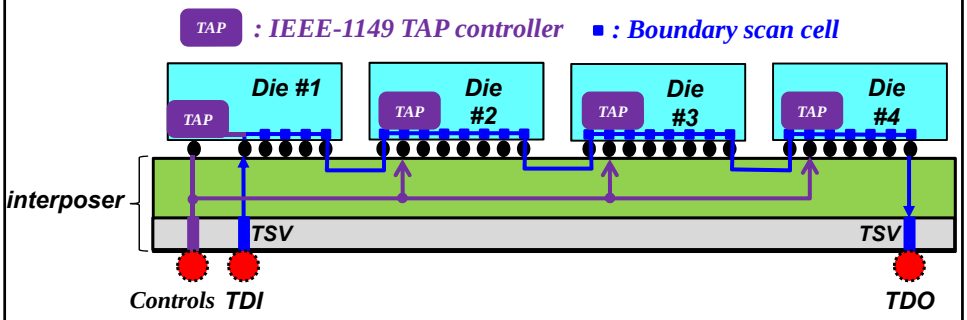
Testing Interconnects in 2.5-D IC

- For each die, interposer wires are like Pseudo-IOs
- Boundary scan cells needed for (1) Die Test, and (2) Interconnect Test



Controls: Boundary Scan Control Signals {TCK, TRST, TMS}

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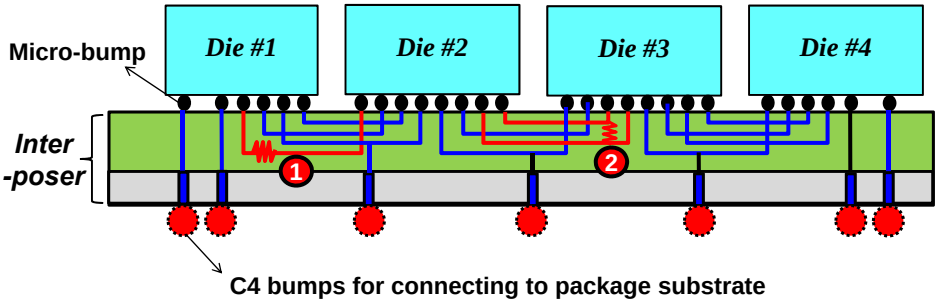
Parametric Faults in High-Speed Die-to-Die Interposer Wires

(1) Resistive Open Fault in an interposer wire ①
(2) Resistive Bridging Fault between two interposer wires ②



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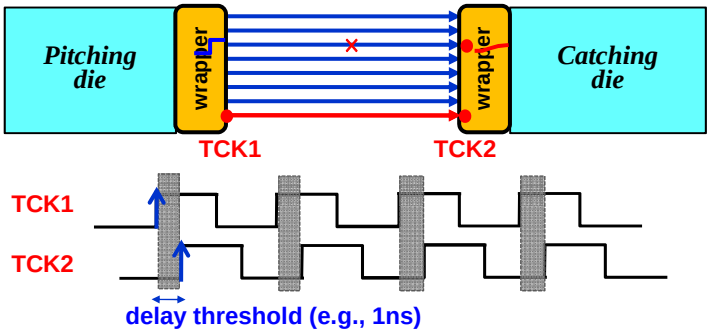
Objective and Challenge

Objective: To detect parametric faults (e.g., <1ns delay fault)
➔May need to maintain a pitcher-catcher timing relationship across dies
(This type of cross-die clock synchronization may not be easy)
➔ There are so other choices…



Note: test clocks TCK1 and TCK2 are low-speed test clocks (e.g., 10MHz)

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Outline

- **Introduction**
- **Pulse-Vanishing Test (PV-Test)**
  - **At-speed testing for high-speed interconnects**
- **VOT-Based Oscillation Test**

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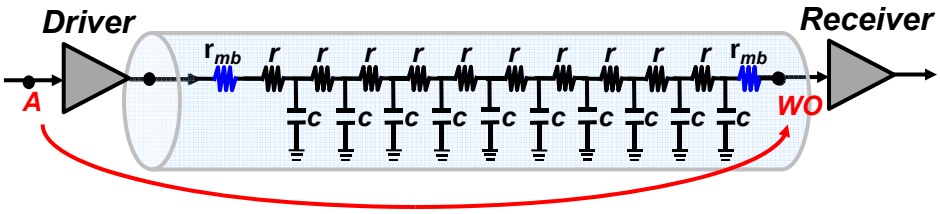
Electrical Model of an Interposer Wire

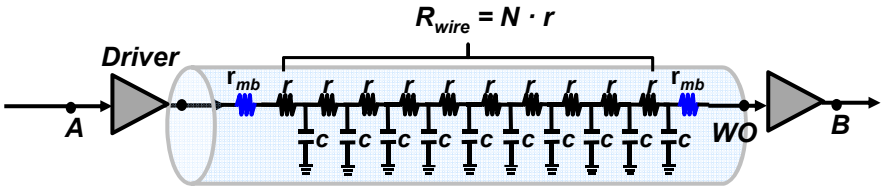
An interposer wire is decomposed into multiple segments of r and c

r_{mb} is the resistance of the micro-bump

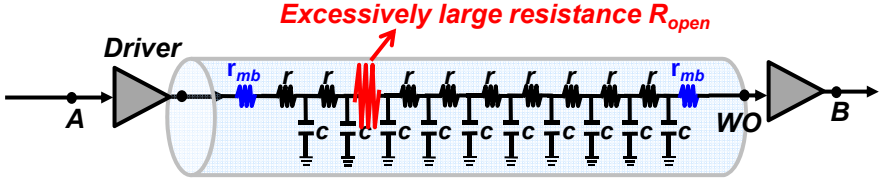


'IW-delay': interposer wire delay from A to WO

Resistive Open Fault Model

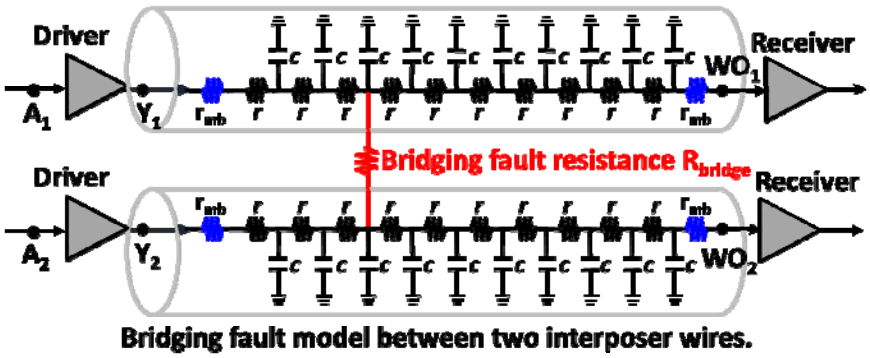


(a) Fault-free model of an interconnect.



(b) Faulty model of an interconnect with a resistive open fault.

Resistive Bridging Fault Model



Bridging fault model between two interposer wires.

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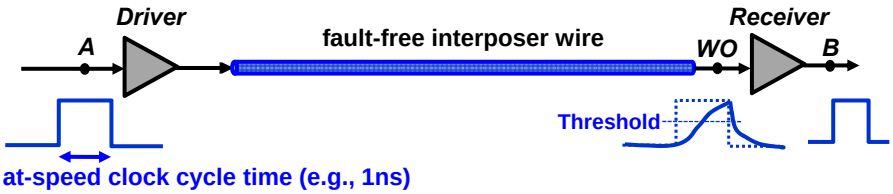
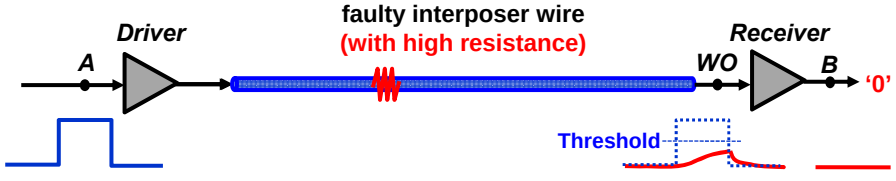
Pulse-Vanishing Test (PV-Test)

Pulse-Vanishing Test:
(1) Test Stimulus: A short-duration pulse (0-1-0)
(2) Fault Detection Criterion:
If the pulse vanishes at the receiver's output, then there is a delay fault





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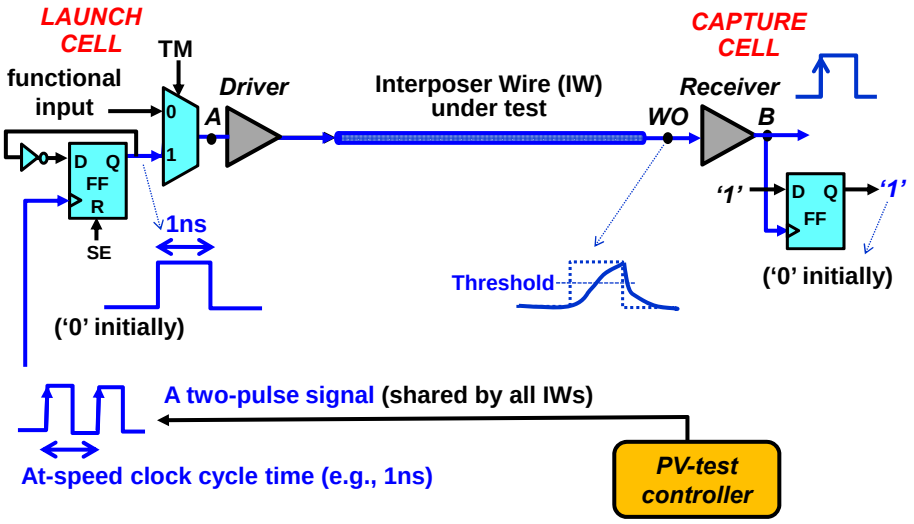
Primitive DfT Circuit (for Pulse-Vanishing Test)



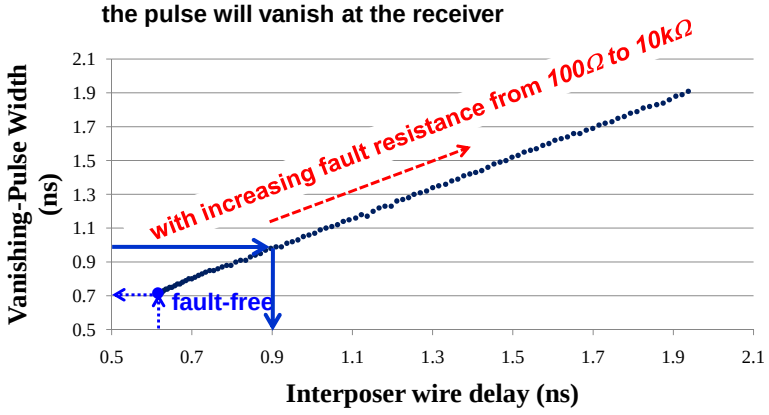
A two-pulse signal (shared by all IWs)

At-speed clock cycle time (e.g., 1ns)

PV-test controller

Vanishing Pulse Width (for 1000 μm Long Interposer Wire)

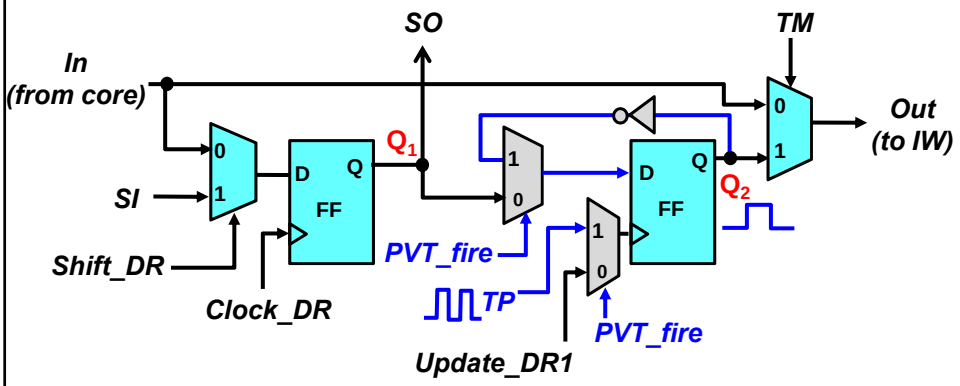
Def: Vanishing Pulse-Width (VPW)
The pulse-width of the applied test pulse above which the pulse will vanish at the receiver



Comment: A larger test pulse width implies larger delay test threshold

Boundary-Scan Compatible Launch Cell

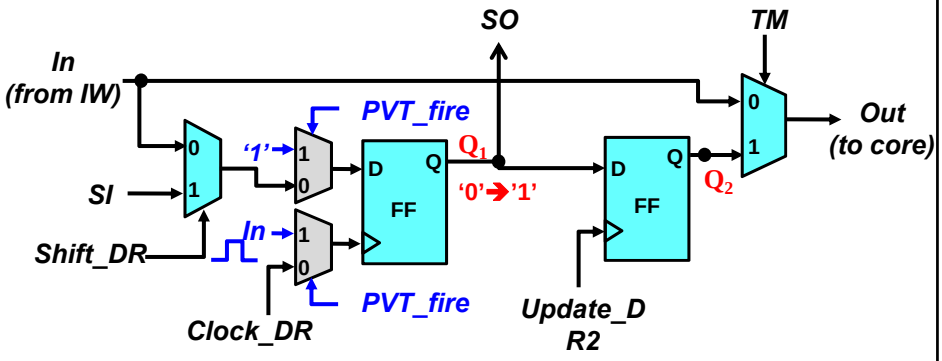
When 'PVT_fire' is '1':
(1) 2nd FF behaves like a toggle-type FF
(2) Two-Pulse signal 'TP' is applied to the clock port of 2nd FF



Note: Q2 needs to be initialized to '0' before a test session

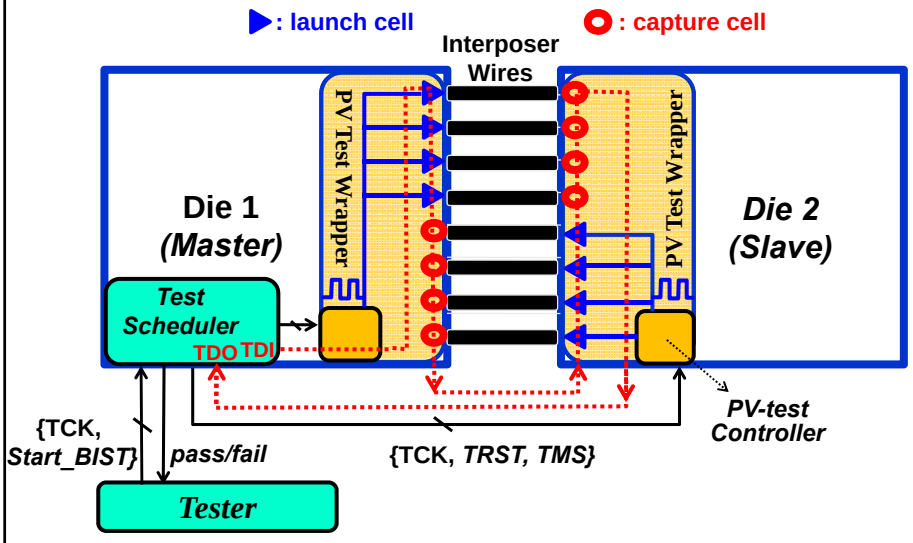
Boundary-Scan Compatible Capture Cell

When 'PVT_fire' is '1':
(1) 1st FF is set to '1' if receiving a clock pulse, otherwise stays '0'
(2) Input signal 'IN' is applied to the clock port of 1st FF



Note: Q1 needs to be initialized to '0' before a test session
The final test result is stored at Q1

Built-In Self-Test Architecture



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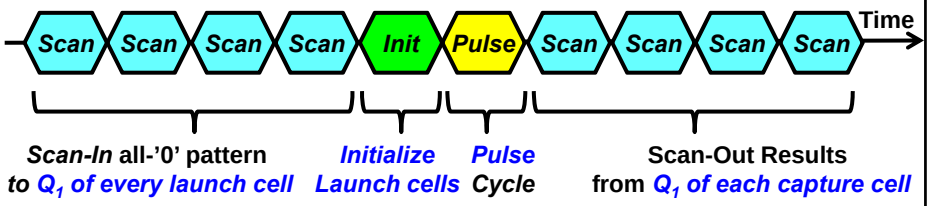
PV-Test Procedure (Scan-In, Init, Pulse, Scan-Out)



'Init': Update the value of Q_1 to Q_2 in every launch cell
'Pulse': Perform pulse-launch and pulse-capture in the same test clock cycle

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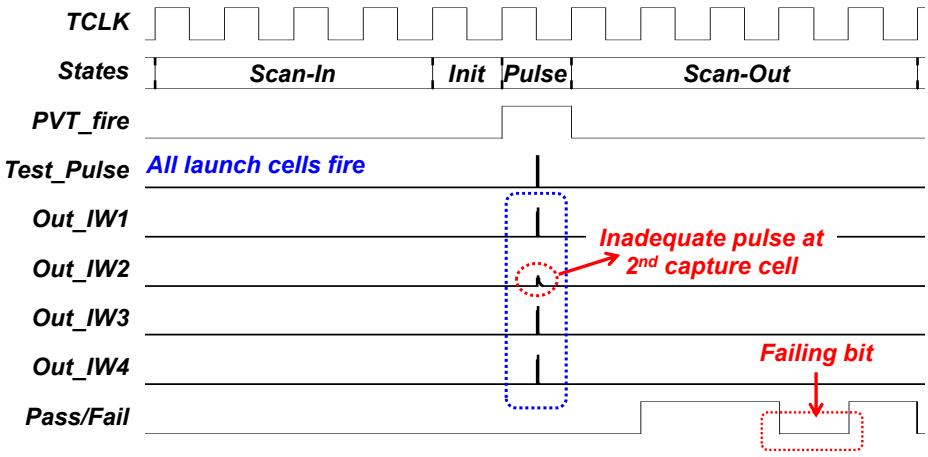
Simulation Waveforms of a PV-Test



Test Result: Interposer wire IW2 is faulty!

Test Time

- **A PV-test session using 10MHz test clock is about**
  - **0.82 ms for 1024 interposer wires**
  - **26.21 ms for 32K (32,768) interposer wires**

Area Overhead

Estimation is based on a 90nm CMOS process

Area overhead		
Type	**Cell Name**	**Layout Area (μm*μm)**
Basic Cells	**INVERTER**	**2.82**
	2-input NAND Cell	**2.94**
	MUX Cell	**8.47**
	FF Cell	**17.64**
Basic Macros	**Boundary Scan Cell**	**52.22**
	Launch Cell	**92.56**
	Capture Cell	**69.16**
	PV-test controller	**670.3**
Overhead Percentage Over 1149.1	**55.55% for 1024 interposer wires**	
	54.9% for 32,768 interposer wires	

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Summary of PV-Test

The interposer needs to be tested alone and thoroughly.
And also, when a 2.5-D IC fails,
We know if the interposer should be responsible.

- **Advantages of Pulse-Vanishing Test**
  - Simple fault detection scheme (No post-processing)
  - Delay Test without die-to-die high-speed clock synchronization
  - Boundary-Scan-Like Test Architecture (55.55% overhead)
  - On-the-spot Diagnosis (good for future self-repair)

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Outline

- Introduction
- Pulse-Vanishing Test (PV-Test)
- VOT-Based Oscillation Test
  - Characterization-based parametric fault testing

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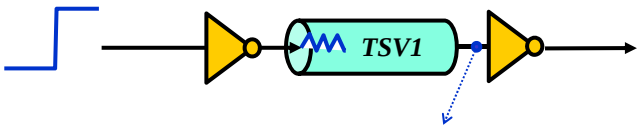
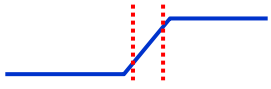
Concept 1:
It's a matter of transition time measurement!

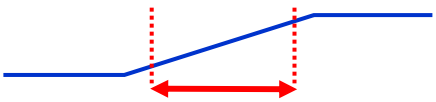
A TSV with delay fault ➔ Longer Rise/Fall Time



Observation point



Normal TSV
➔ Shorter rise time



Resistive TSV
➔ Longer rise time

To be measured…

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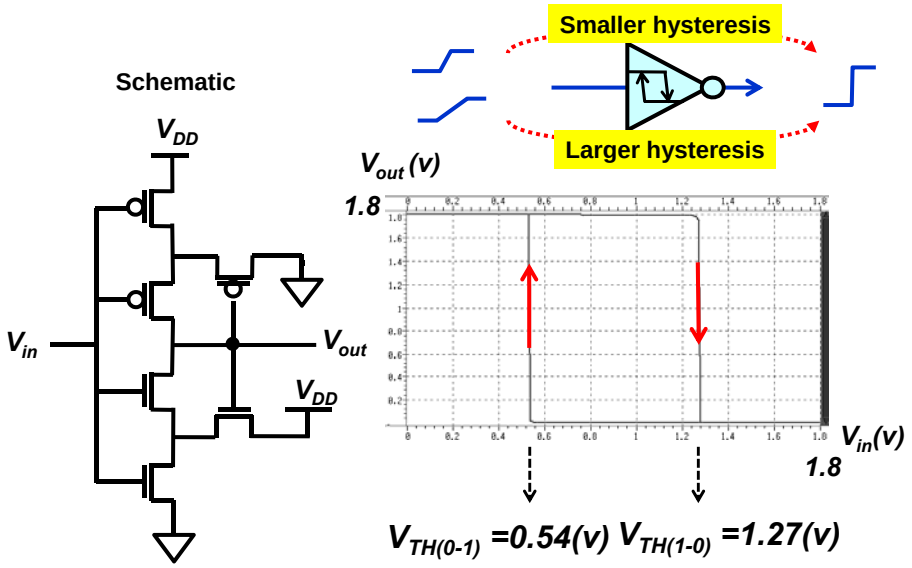
Concept 2: Use Schmitt-Trigger Inverter
- Hysteresis proportional to the input Transition time



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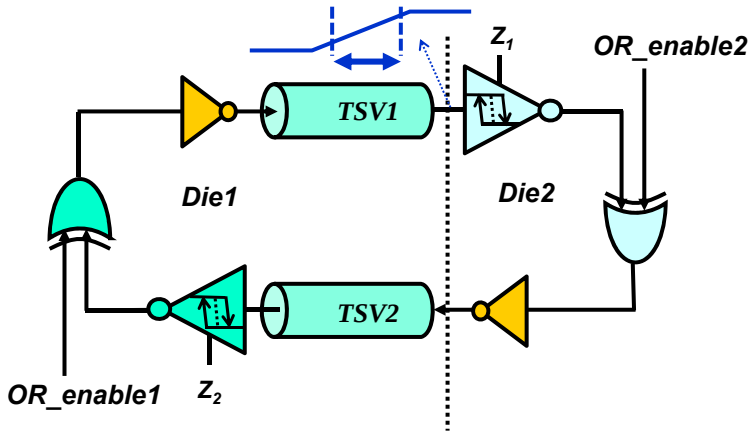
Architecture of VOT Scheme (Per TSV Pair)
(VOT: Variable Output Threshold)

Use Variable-Threshold Output Inverter for each TSV:
(1) Control signal Z = 0 → *Normal Inverter*
(2) Control signal Z = 1 → *Schmitt-Trigger Inverter (WITH HYSTERESIS)*



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Brief Summary of our Idea

TSV Delay ➔ Transition Time

Transition Time ➔ Oscillation Period Change

(from normal to Schmitt-Trigger)

(Easily Measurable)

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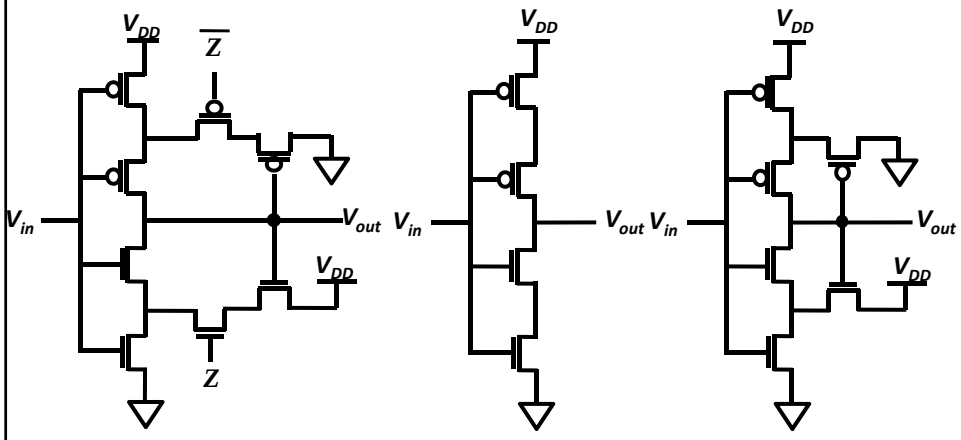
Schematic of a VOT Inverter

(a) overall schematic (b) normal inverter (Z=0) (c) ST inverter (Z=1)



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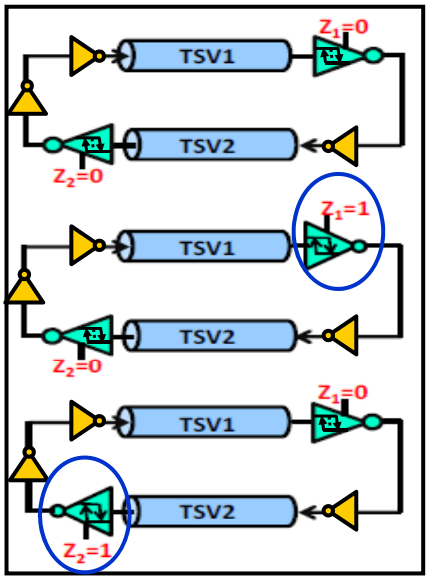
Three Oscillation Periods in VOT-Analysis



(1) Normal mode:

Oscillation period=T_{REF}

(2) TSV1-in-ST mode

Oscillation period=T_{ST1}

TSV1 delay ~ ΔT_1 (T_{ST1} – T_{REF})

(3) TSV2-in-ST mode

Oscillation period=T_{ST2}

TSV2 delay ~ ΔT_2 (T_{ST1} – T_{REF})

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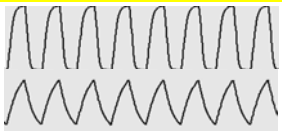
Example: Predict the Delay of Each TSV

R_{TSV1}=10 (Ω) C_{TSV1}=400 (fF) R_{TSV2} =1 (kΩ) C_{TSV2}=800 (fF)

Waveforms under the normal configuration T_{REF} = 4.42 ns

endpoint of TSV1 — *Smaller Transition times*

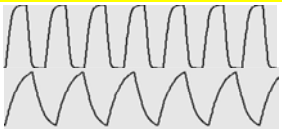
endpoint of TSV2 — *Larger Transition times*



Waveforms under the Schmitt-Trigger configuration

endpoint of TSV1 — T_{ST1} = 5.05 ns

endpoint of TSV2 — T_{ST2} = 6.49 ns



Normal Configuration: T_{REF} = 4.42 ns
TSV1-in-ST Configuration: T_{ST1} = 5.05 ns (smaller increase from T_{REF})
TSV2-in-ST Configuration: T_{ST2} = 6.49 ns (larger increase from T_{REF})
ΔT_{ST1} = 5.05 – 4.42 = 0.63 ns
ΔT_{ST2} = 6.49 – 4.42 = 2.07 ns

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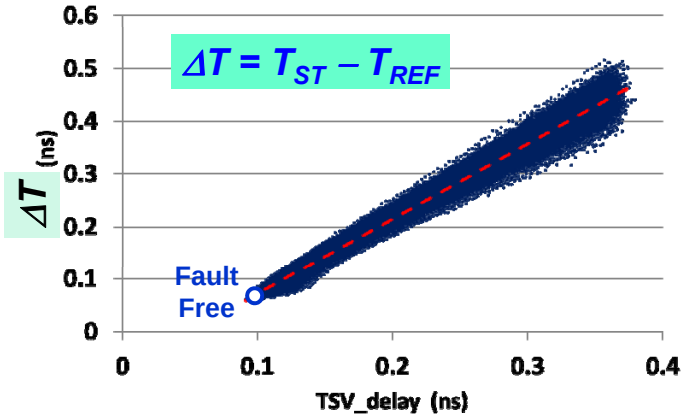
Ex: Correlation between TSV Delay and ΔT

- Fault Population: Resistive Open Faults
- An outlier in measurable ΔT is an outlier in TSV delay



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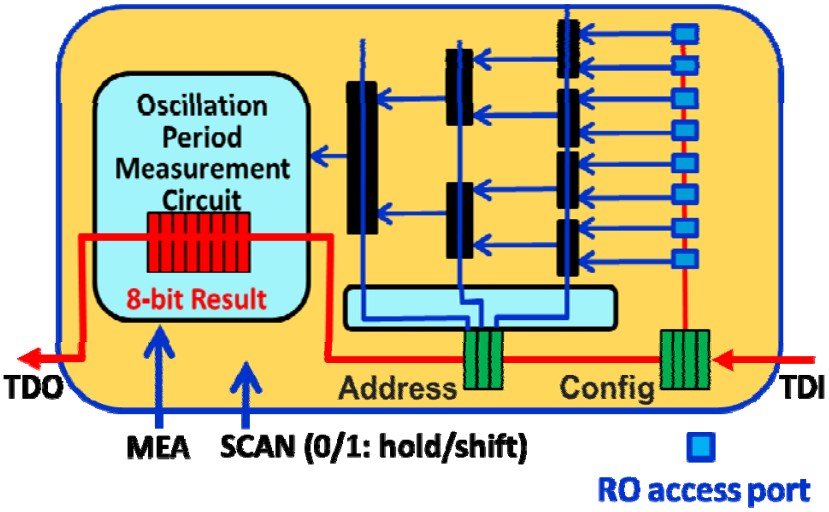
RO, MUX Tree, and Measurement Circuits



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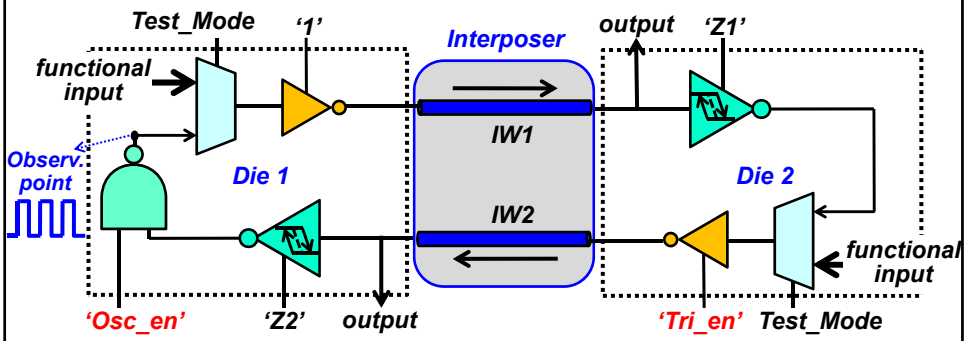
Ring Oscillator (RO) (for One Pair of Interposer Wires)

Two extra Control Signals (to support bridging fault detection):
(1) 'Osc_en': enabling signal for oscillation
(2) 'Tri_en': tri-state enabling signal for the driver of IW2



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Three Test Strategies

Principles:
(1) All ROs oscillate concurrently to detect "resistive open faults"
(2) One RO oscillates at a time to detect "inter-RO resistive bridging faults"
(3) No RO oscillates to detect "intra-RO resistive bridging faults"

	Test Strategy	RO Settings	Test Actions
Test OPEN	AO-strategy (All Oscillation)	Every RO is Active	Measure $\{T_{REF}, T_{ST1}, T_{ST2}\}$ of every RO in sequence
Test Inter-RO BRIDGING	OO-strategy (One Oscillation)	Target RO is Active (One RO at a time)	Measure $\{T_{REF}, T_{ST1}, T_{ST2}\}$ of the target RO
		The others are Grounded	NA
Test Intro-RO BRIDGING	NO-strategy (No Oscillation)	Every RO is Half-Floating	Measure $\{T_{REF}\}$ of every RO

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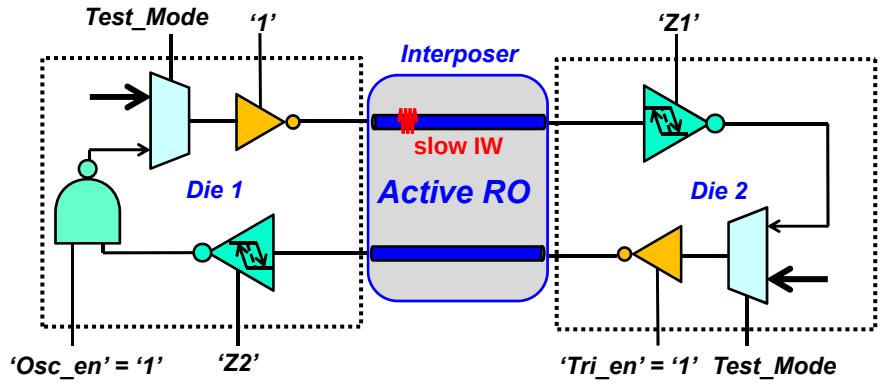
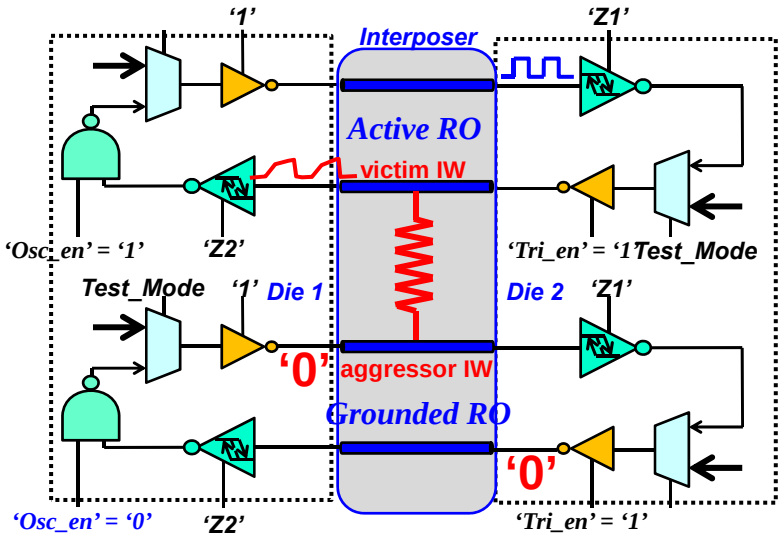
AO-strategy (All-Oscillation) (to detect an open fault)



An open fault occurring to an interposer wire.

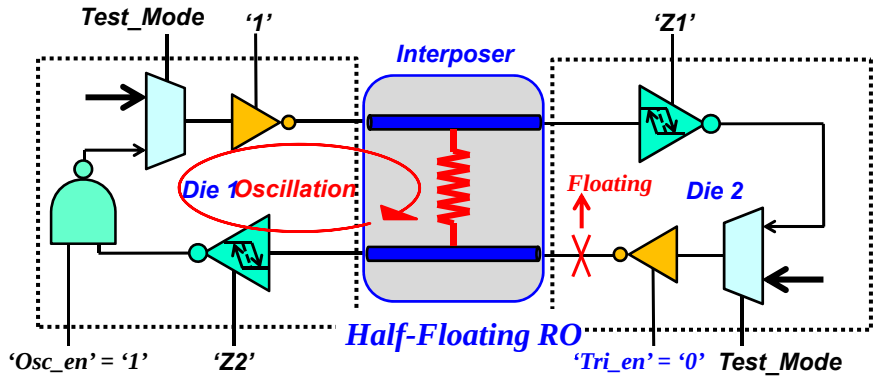
OO-strategy (One-Oscillation) (to detect an inter-RO bridging fault)

An inter-RO bridging fault will slow down the speed over a victim IW.

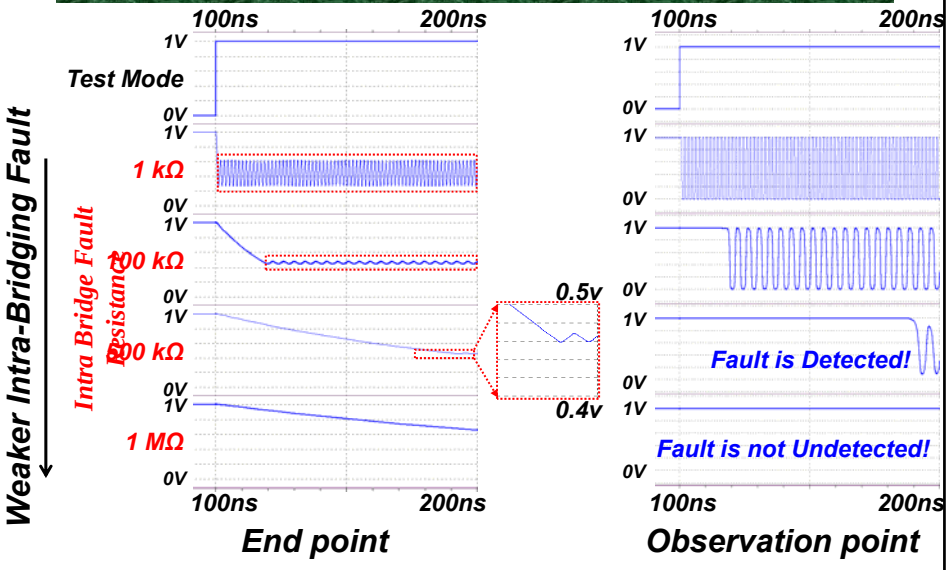


NO-strategy (No-Oscillation) (to detect an intro-RO bridging faults)

The existence of an intro-RO bridging fault will cause a half-floating RO to oscillate abnormally.

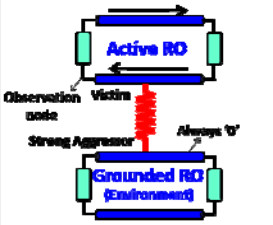


Waveform of 'End Point' and 'Observation point' in NO-strategy



Example for an Inter-Bridging Fault

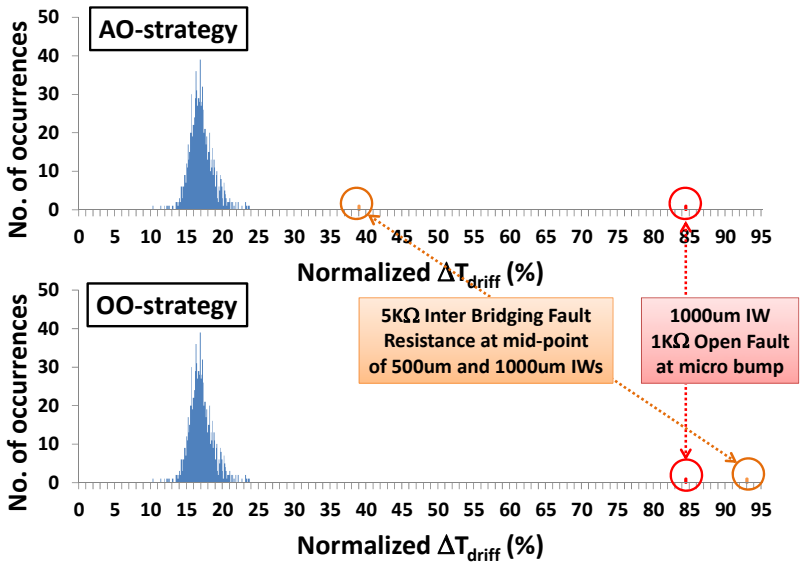
(a) AO (All-Oscillation) Strategy



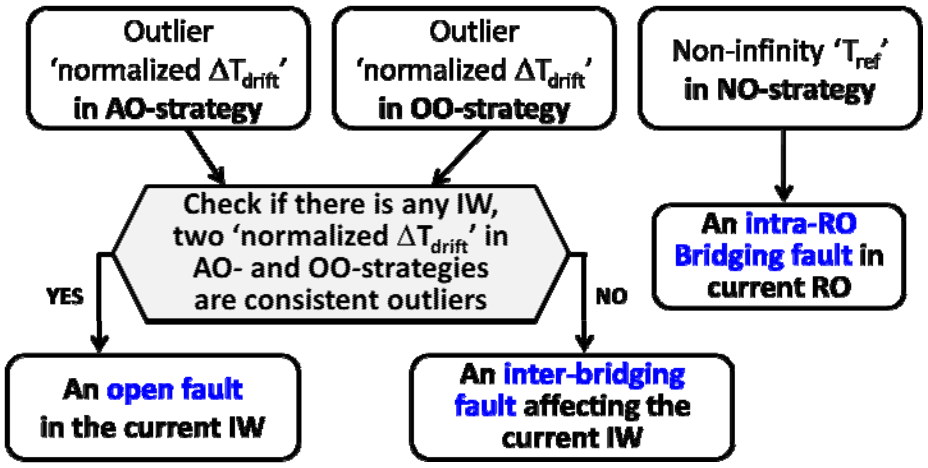
(b) OO (One-Oscillation) Strategy

	Average T_{ref}	Average T_{slow}
AO-strategy	1V, 0V, 2.49ns	1V, 0V, 2.88ns
	ΔT = 0.39, Normalized ΔT drift = 39%	
OO-strategy	1V, 0V, 2.66ns (*Consistent slower rise time*)	1V, 0V, 3.20ns
	ΔT = 0.54, Normalized ΔT drift = 93%	

Example for an Inter-Bridging Fault



Fault Type Classification



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Normalized ΔT_{drift} for Outlier Analysis

For each IW w_i, we have two versions of ΔT:

$$\Delta T_{sim}(w_i) = T_{ST\_sim}(w_i) - T_{REF\_sim}(w_i)$$
$$\Delta T_{measure}(w_i) = T_{ST\_measure}(w_i) - T_{REF\_measure}(w_i)$$

$\Delta T_{drift}(w_i)$ respresents the drifting amount of a measurement version of ΔT away from its simulation version:

$$\Delta T_{drift}(w_i) = \Delta T_{measure}(w_i) - \Delta T_{sim}(w_i)$$

To take into account of the wire-length diversity, we further normalize it:

$$(Normalized\_\Delta T_{drift}) = \left(\frac{\Delta T_{measure} - \Delta T_{sim}}{\Delta T_{sim}}\right) \cdot 100\%$$

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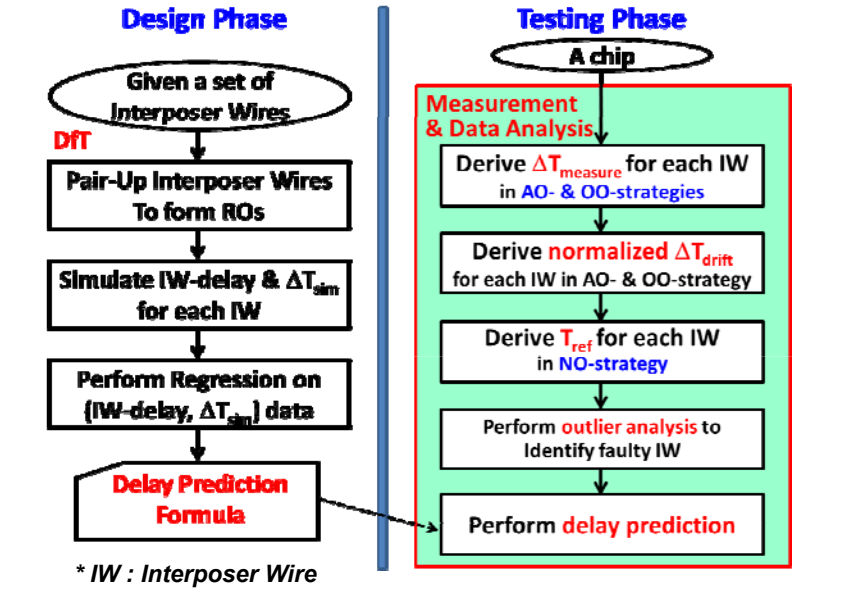
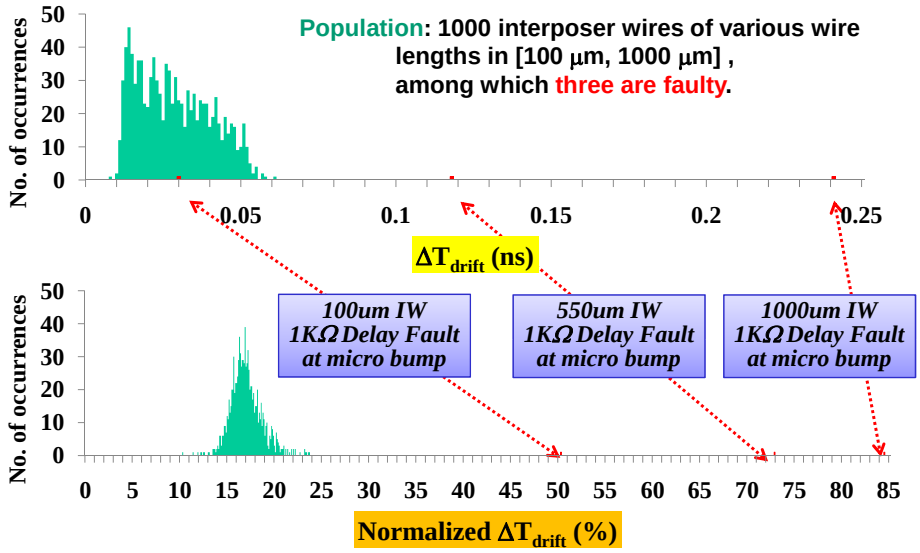
Testing and Characterization Flow



Fault Detection (Finding Outliers in Normalized ΔT_{drift})

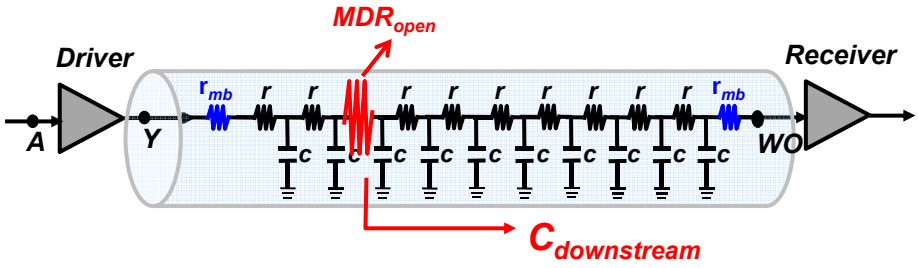


Fault Detection Capability (For Resistive Open Faults)

MDR_{open}: Minimum Detectable Open Fault Resistance 245 Ω

This metric refers to the open fault resistance value beyond which the proposed test method can detect the fault successfully based on the outlier analysis using 3σ rule.

Detectable Extra-RC: (MDR_{open}) * ($C_{downstream}$) 50.7 ps



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Resistive Open Fault Detection Capability

A resistive open fault occurring at the micro-bump of the driver side of a 1000um long interposer wire.

Pseudo Chip Conditions	MDR_{open} (Min. Detectable Open Fault Resistance)	Detectable Extra-RC
#1 (FF & -10% RC)	245 Ω	50.7 ps
#2 (FF)	76 Ω	17.5 ps
#3 (SS)	113 Ω	26.0 ps
#4 (SS & +10% RC)	78 Ω	19.7 ps
Average	145 Ω	31.4 ps

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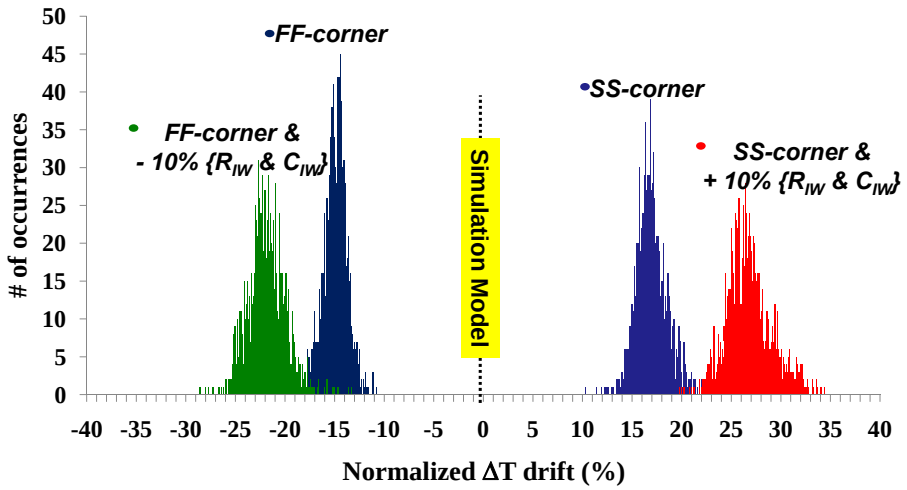
Process Drift from Simulation Model



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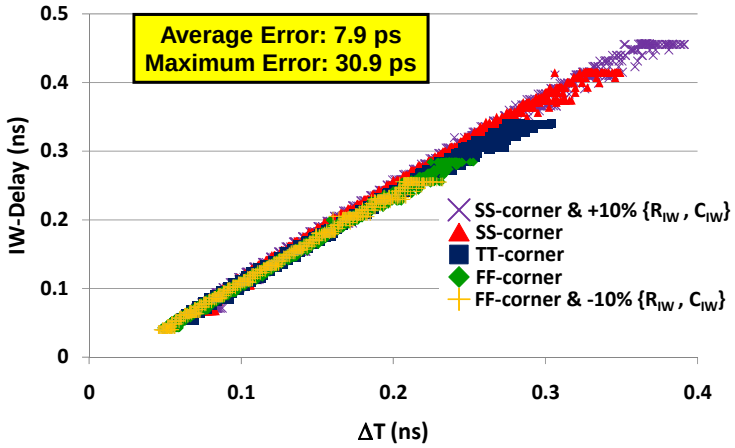
Fault-Free IW-Delays vs. ΔT for Various Pseudo Chip Conditions

Implication: Regression mode derived by TT corner Is applicable under process variations.



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Summary of VOT-Based Oscillation Test

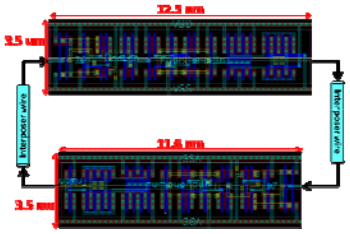
The interposer needs to be tested alone and thoroughly.
And also, when a 2.5-D IC fails,
We know if the interposer should be responsible.

Test Time

11 ms for 1024 wires
413 ms for 32K wires

Using 10MHz TCLK

Layout of an RO



~55%
Over boundary scan test

Conclusion

Criterion	PV-test	VOT-based oscillation test
Basic Concept	Check if pulse will vanish	Measure ΔT
Fault Detection Scheme	Test threshold based	Outlier analysis
Area overhead	55.5% over IEEE-1149.1	55.7% over IEEE-1149.1
Test time	0.82 ms for 1024 wires 26.21 ms for 32K wires	4.7 ms for 1024 wires 177 ms for 32K wires
Other benefits	No post-processing On-the-spot diagnosis Easier self-repair	Delay characterization Process tracking

Outlier analysis: A measurement sample that significantly deviates away from the entire population indicates a fault