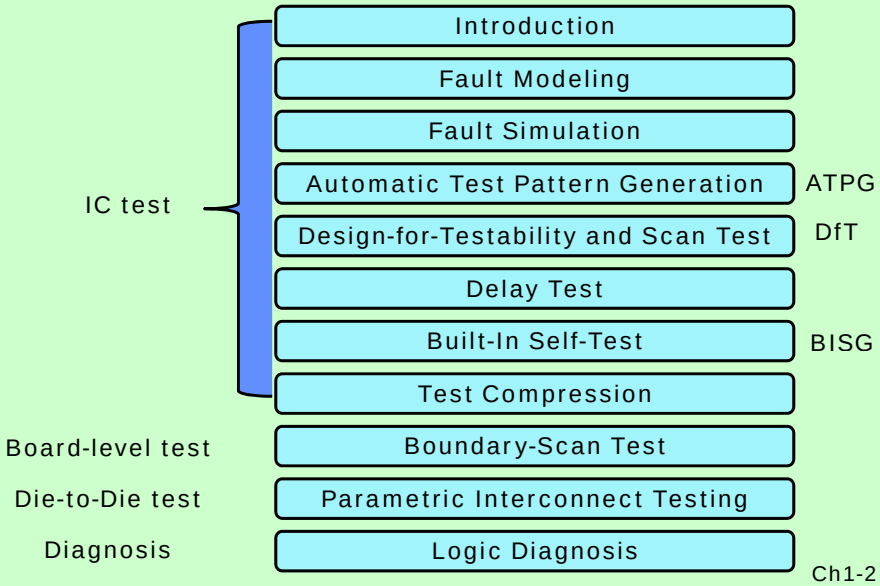
國立清華大學電機系

EE-6250
超大型積體電路測試
VLSI Testing

Chapter 1
Introduction

Course Flow



What You can Benefit from this Course?

- Values of Acquired Knowledge
  - Making ICs more testable
  - Making ICs/Boards/Systems more debuggable
  - Making ICs Faster Time-to-Market
  - Making ICs Faster Time-to-Volume
- Academic Training
  - Testing is a rich field as you will know.
  - Testing is a good topic for MS/Ph.D. theses.
- Career Development
  - IC 設計公司 (讓晶片的可測試性更高)
  - 半導體廠 (故障診斷，良率追蹤與分析與改善)
  - 測試產業 (量產測試之規劃與執行)
  - 電子系統廠 (系統故障診斷，可靠度分析與改善)

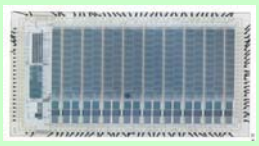
Chip Design & Manufacturing Flow

Idea

Architecture Design

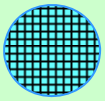
Block diagram

Circuit & Layout Design



Layout

IC Fabrication

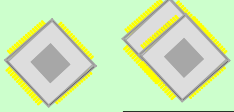


Wafer (hundreds of dies)

Sawing & Packaging

Final chips

Testing



Bad chips

Good chips

customers

Design Verification, Testing and Diagnosis

- Design Verification:
  - Ascertain the design perform its specified behavior
- Testing:
  - Exercise the system and analyze the response to ascertain whether it behaves correctly after manufacturing
- Diagnosis:
  - To locate the cause(s) of misbehavior after the incorrect behavior is detected

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Manufacturing Defects

- Material Defects
  - bulk defects (cracks, crystal imperfections)
  - surface impurities
- Processing Faults
  - missing contact windows
  - parasitic transistors
  - oxide breakdown
- Time-Dependent Failures
  - dielectric breakdown
  - electro-migration
- Packaging Failures
  - contact degradation
  - seal leaks

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Faults, Errors and Failures

- Fault:
  - A physical defect within a circuit or a system
  - May or may not cause a system failure
- Error:
  - Manifestation of a fault that results in incorrect circuit (system) outputs or states
  - Caused by faults
- Failure:
  - Deviation of a circuit or system from its specified behavior
  - Fails to do what it should do
  - Caused by an error
- Fault ---> Error ---> Failure

Reliability Test

- Temperature Related
  - Hi-Temperature Life Test
  - Low-Temperature Life Test
  - Temperature-Cycling Test
- Humidity Test
- Salt Mist Test
- UV (Ultra-Violet) Test
- ESD Test
  - ESD stands for Electro-Static Discharge
- Whole Mechanical Test

Detailed Reliability Test Items

- Temperature Related
  - Operation: 0^0C/120hr ~ 70^0C/120hr (商規)
  - Operation: -40^0C/120hr ~ 85^0C/120hr (工規)
  - Storage: -40^0C/200hr ~ 85^0C/500hr
  - Junction Temperature: Max. 95^0C
- Humidity Test
  - Operation: 25^0C/95% humidity (商規)
  - Operation: 40^0C/95% humidity (工規)
  - Storage: 85^0C/95% humidity
- Salt Mist Test
  - Salt Water Spray
- UV Test
  - UV (254nm), 15Ws/cm^2
  - X-ray exposure, 0.1Gy/1hr
- ESD Test
  - For example, For Contact Pads, ±4KV, Human Body Mode
- Whole Mechanical Test
  - Vibration (15G, 10 to 2KHz), Impact, Torque, Bending, Drop test

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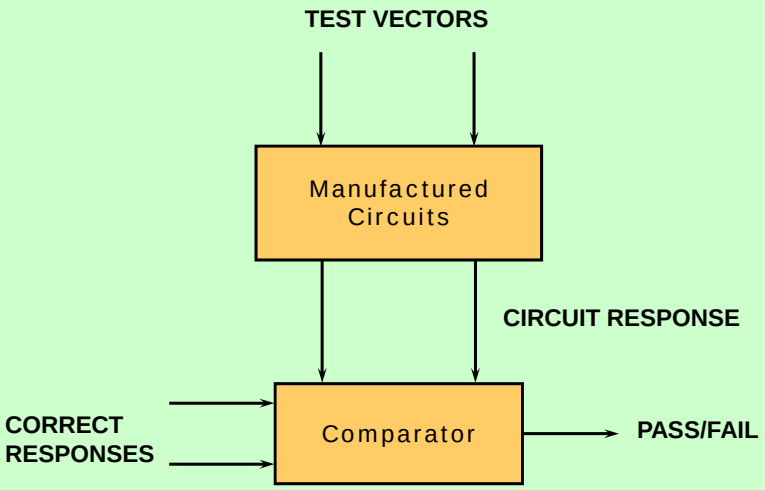
Scenario of Manufacturing Test



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Courses on Agilent 93000 at CIC

Sample Information: (What to expect from that kind of course)

上課地點	新竹CIC - 訓練教室B (新竹市科學園區研業一路26號八樓)
課程說明	本課程將介紹如何利用Agilent 93000 SoC Tester來進行數位晶片的測試，課程內容包含loadboard使用方式、測試程式開發、量測結果分析。
課程大綱	(1) Agilent 93000 SoC Tester 介紹 (2) Loadboard 使用方法 (3) Test Pattern 轉換 (4) Test flow 建立 (5) Result Analysis

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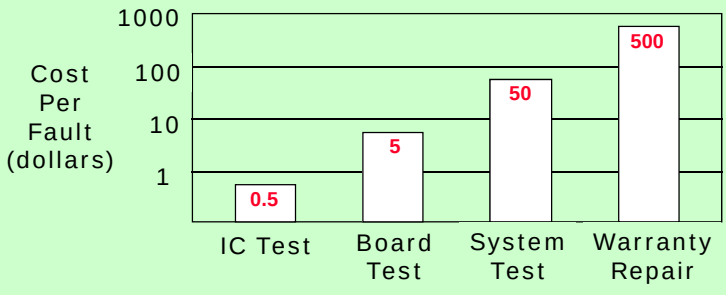
Purpose of Testing

- Verify Manufacturing of Circuit
  - Improve System Reliability
  - Diminish System Cost
- Cost of repair
  - goes up by an order of magnitude each step away from the fab. line



B. Davis, "The Economics of Automatic Testing" McGraw-Hill 1982

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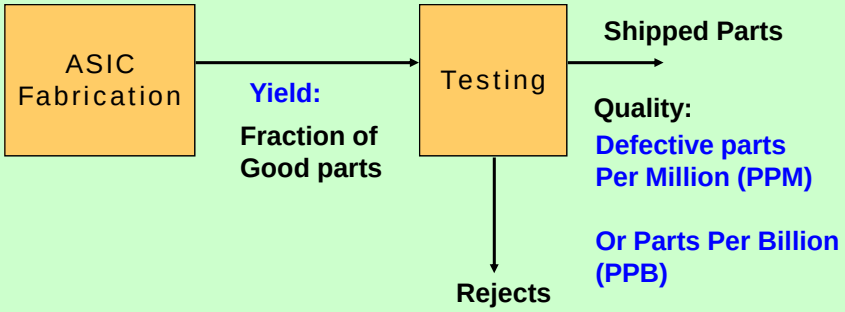
Testing and Quality



Quality of shipped part is a function of yield Y and the test (fault) coverage T.

Fault Coverage

- Fault Coverage T
  - Is the measure of the ability of a set of tests to detect a given class of faults that may occur on the device under test (DUT)

$$T = \frac{\text{No. of detected faults}}{\text{No. of all possible faults}}$$

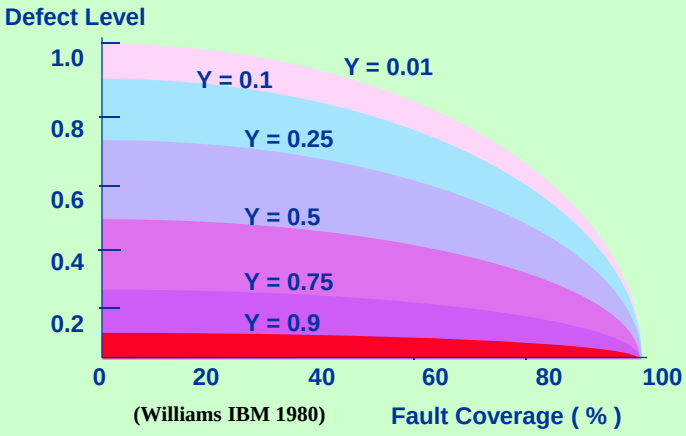
Defect Level

- Defect Level
  - Is the fraction of the shipped parts that are defective (單位 ppm or ppb)

$$DL = 1 - Y^{(1-T)}$$

Y: yield
T: fault coverage

Defect Level v.s. Fault Coverage



High fault coverage ⟶ Low defect level

DPM v.s. Yield and Coverage

Yield	Fault Coverage	Defective PPM
50%	90%	67,000
75%	90%	28,000
90%	90%	10,000
95%	90%	5,000
99%	90%	1,000
90%	90%	10,000
90%	95%	5,000
90%	99%	1,000
90%	99.9%	100

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Why Testing Is Difficult ?

- Test application time could explode for exhaustive testing of VLSI
  - For a combinational circuit with 50 inputs, we need $2^{50} = 1.126 \times 10^{15}$ test patterns.
  - Assume one test per 10^{-7}sec, it takes 1.125×10^{8}sec = 3.57yrs. to test such a circuit.
  - Test generation for sequential circuits are even more difficult due to the lack of controllability and observability at flip-flops (latches)
- Functional testing
  - may NOT be able to detect the physical faults

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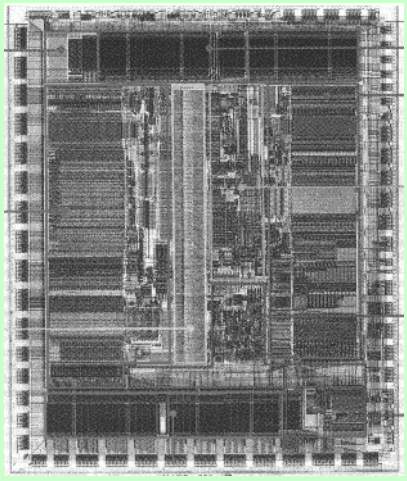
DEC Alpha Chip (1994)



- 64-bit RISC
- 200 MHz
- 400 MIPS
- 200 Mflops
- 16.8 x 13.9 mm^2 die
- 0.68 million transistors
- 431-pin package
- 3.3 V
- 30 W power consumption

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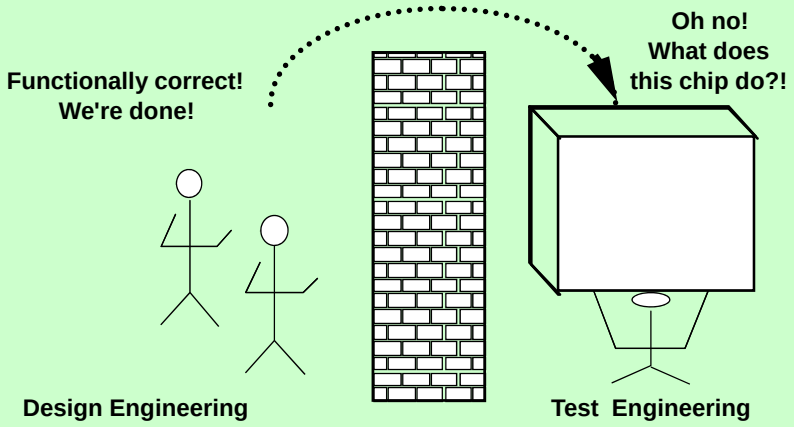
The Infamous Design/Test Wall

30 years of experience proves that test after design does not work!



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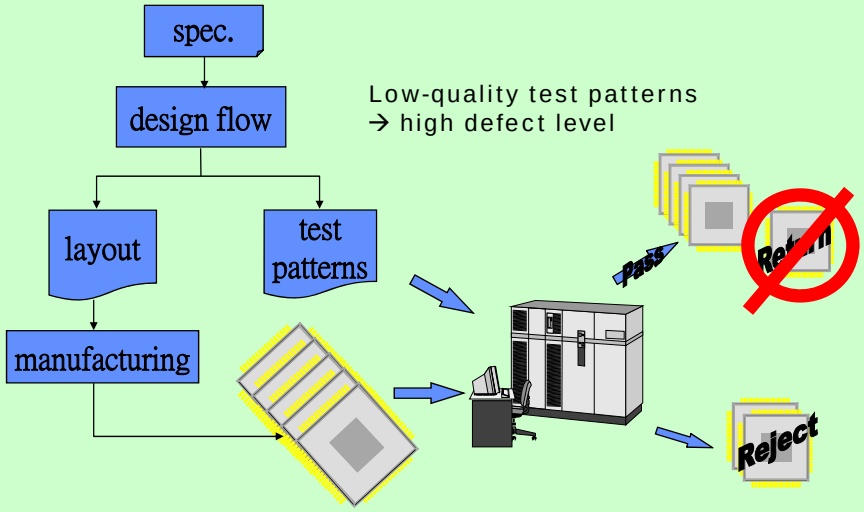
Old Design & Test Flow



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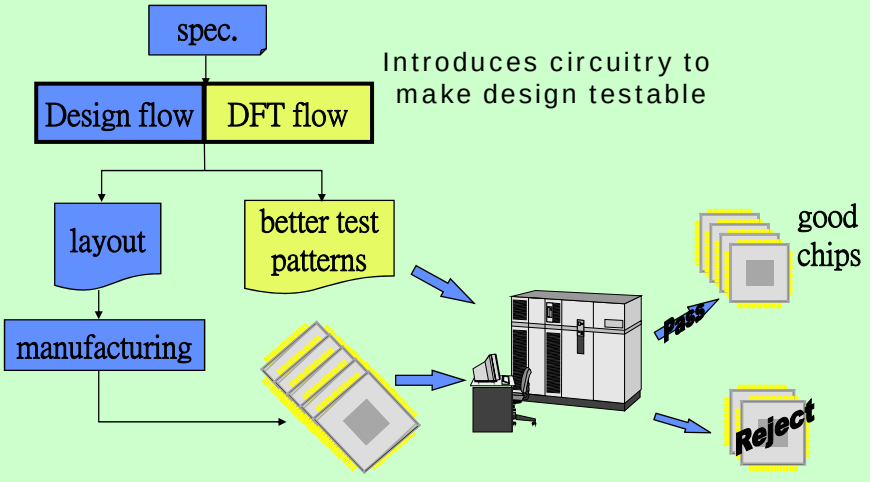
New Design and Test Flow



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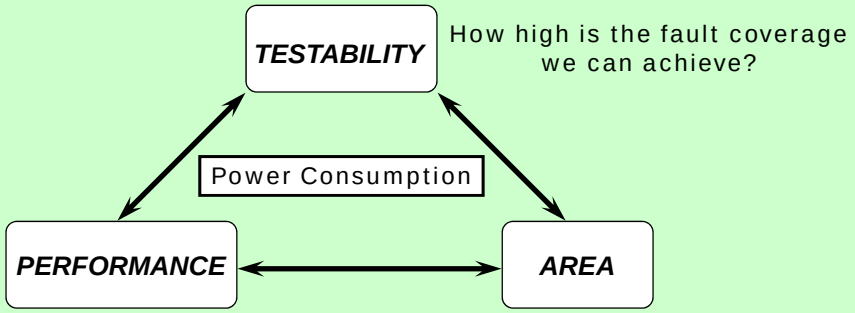
New Design Mission

- Design circuit to optimally satisfy their design constraints in terms of area, performance and testability.



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