研究經驗分享

清大電機系　黃錫瑜

Jan. 2015

Outline

- 自我介紹
- 研究經驗介紹
- 未來的展望

簡歷

- **Education**
  - **1988 BS from 台大電機系**
  - **1992 MS from 台大電機系**
  - **1997 Ph.D. from ECE Dept., UC, Santa Barbara**
    - **Title: Formal Verification and Design Debugging**
- **Working Experience**
  - **Oct. 1997 – July 1998 National Semi, Santa Clara, USA**
  - **Aug. 1998 – July 1999 世大積體電路 (後併入台積)**
  - **Aug. 1999 – now, 清華電機系**
- **Start-up Experience**
  - **兆心科技 (2007-2012)**

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Outline

- 自我介紹
- 研究經驗介紹
  - **VLSI Design, Automation, and Testing**
- 未來的展望

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曾經研究過的 IC Design 類的題目...

研究類別	研究題目	技術項目	與現有技術比較之優點
積體電路設計	(1) 高良率奈米靜態記憶體設計   SRAM compiler	X-Calibration 的技術，自動校正位元線上的漏電流	將 SRAM 可容忍之漏電流從 120uA 提昇至 300uA
		PCTT: Per-Column Timing Tracking 位元線時序追蹤方法	增加 SRAM 的穩定性與良率
		BATT: BIST-Assisted Timing Tracking 位元線時序追蹤方法	增加 SRAM 的穩定性與良率
		Self-Vdd-Tuning 自動降壓調降法	降低操作電壓節省功耗但維持指定的速度間隙以維持不受溫度變化之高可靠度
		低漏電之 285mV 10T 新 SRAM 細胞	90nm 製程下可操作在 285mV，1.5X 的雜訊容忍並減少 80%漏電流
	(2) 高精準度全數位鎖相迴路	(1) 1ps 超高準度相位比較器 (2) 1ps 精準度的頻率鎖定方法 (3) 具有頻率內差功能	可以將相位鎖定誤差從 5 ps 降至 1ps，達成超準的頻率鎖定。 相位誤差從原本的 588ps 降低為 21 ps。

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曾經研究過的 EDA 類的題目...
(Two Products TinnoTek Tried to Market)

積體電路設計自動化 (EDA)	(3) 多核心系統晶片之功率消耗評估方法 (PowerMxier)	從 Layout-Based 功耗建 到 ESL 功耗估計的完整解決方案	用於工研院兩個 PACDSP 核心的系統晶片估計 軟體功耗，誤差僅 1.43%，比邏輯階層快 2400 倍。
	(4) 全數位鎖相迴路編譯器	(1) 保證無雜訊之 cell-based 數位控制震盪器 (DCO) (2) 可適應溫度變化之頻率追蹤方式 (Smooth Code Jump (3) 自動搜尋演算法達成低面積、低功耗之目的 (4) 自動化跨製程的自我校正軟體 (約兩天即可轉移至新製程上)	全世界第一個可跨製程，低 時脈訊號產生器 自動化解決方案】

1-minute 簡介 Later…

1-minute 簡介 Later…

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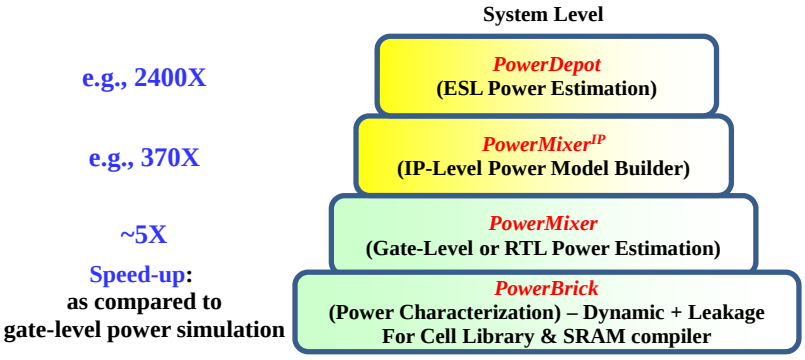
1-Minute Marketing
Our Power Estimation Tools

We can help to estimate how good your low-power scan test is…
→ To report the real test power in Watt not WSA



Note: these tools were ever supported by TinnoTek
Now a friend in Silicon Valley is trying to keep it alive…

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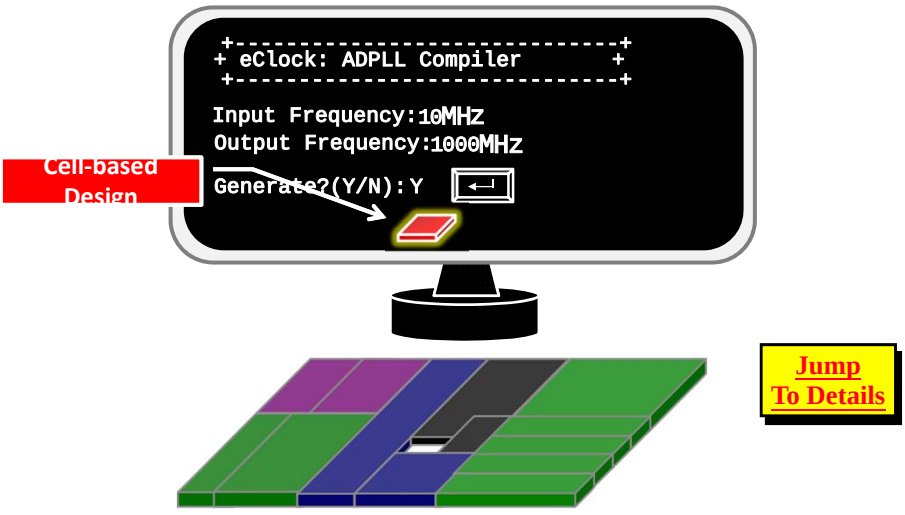
1-Minute Marketing
Our Push-Button ADPLL Compiler - eClock



Jump To Details

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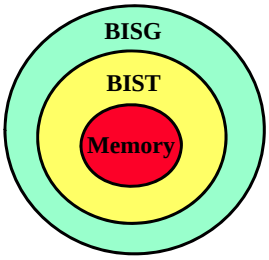
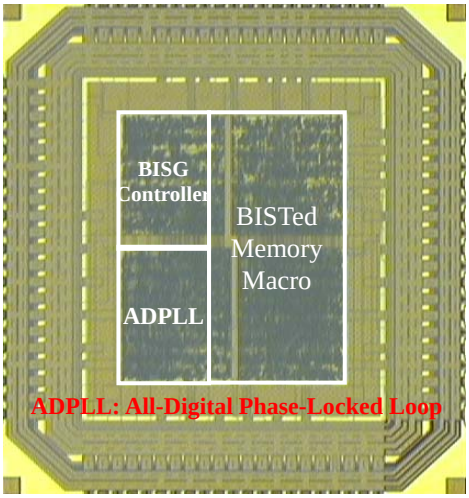
(將我的一些研究經驗融合一下…)
Built-In Speed Grading (BISG)

To gauge the maximum operating speed of a circuit via embedded ADPLL
用途: (1) Speed binning, (2) Process monitoring, (3) Performance debugging, (4) Vdd-tuning





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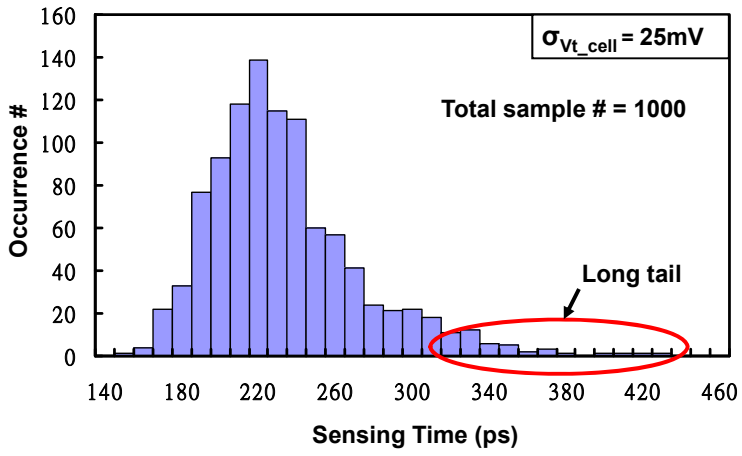
Sensing Time: The Tail Bit Effect

Based on Monte-Carlo simulation of a 32-nm 1k-bit SRAM macro
To guarantee high-yield, the timing control needs to accommodate the worst-case



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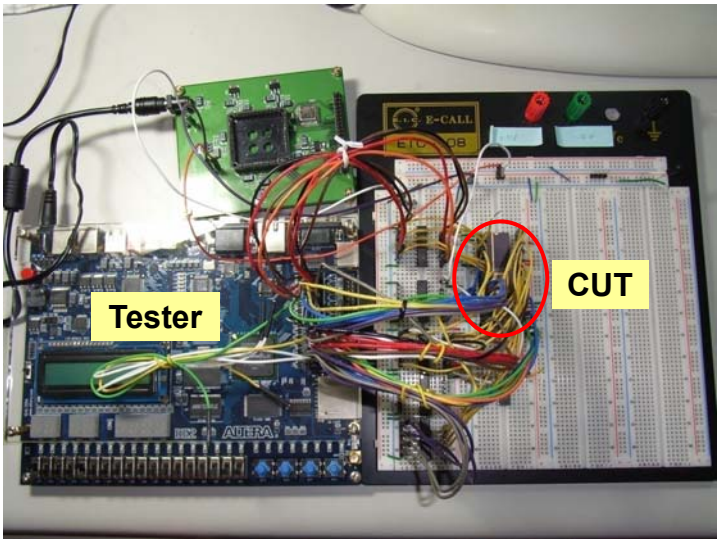
FPGA-Based Measurement Setup



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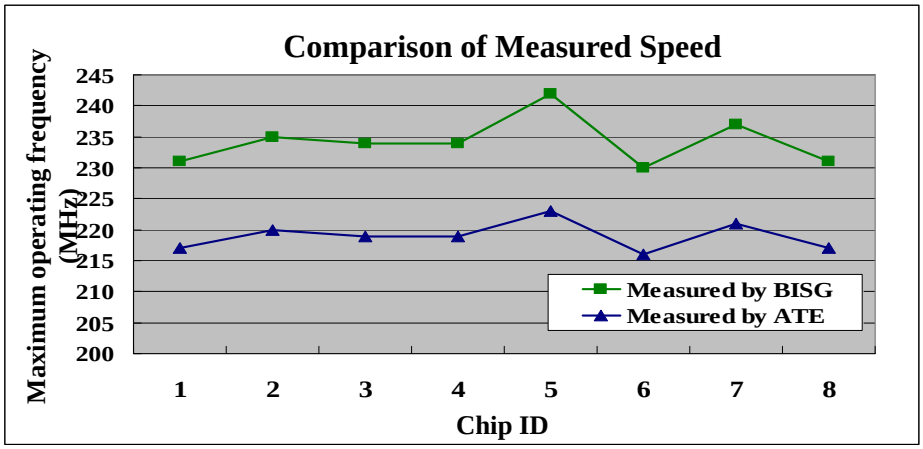
Max. Speed Profile by BISG & ATE

For 0.18um → Speed range is [230, 242] MHz for 8 test chips
(i.e., there is about 5% speed variation)



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曾經研究過的 Testing 類的題目...

積體電路測試	(5) 萬用型群體廣播式掃瞄鍊測試方法	UMC-Scan Test: 將群體廣播式掃瞄鍊測試之速度推至幾乎極限	可將測試時間的縮短倍數從 2005 年別人方法的 19 倍改善至 53 倍
	(6) 邏輯晶片診斷技術之研發	類『針炙式』故障診斷演算法	平均檢查 3.5 個訊號線即可逮住故障點
		『符號式模擬法』故障診斷法	可處理原本幾乎無法處理的『拜占庭式瑕疵』
		『訊號趨勢分析為基礎』診斷法	可處理原本無法處理的『掃瞄鍊短路瑕疵』
		(Diagnosis by Recovery) 診斷法	可處理原本幾乎無法處理的『掃瞄鍊時有時無的延遲故障』
	(7) 三維晶片裸晶間連接線之參數型瑕疵測試	Known-Good-Die (KGD) Testing	Input-Sensitivity Analysis 可以只用邏輯電路偵測到每一個 Pre-Bond 的 TSV 瑕疵所造成的等效電容變異
		漏電流瑕疵	率先對 TSV 達成了精確的【漏電流分級】的能力
		Post-Bond 後的連接線『阻抗性的斷路或短路瑕疵』	簡稱 VOT-Analysis 的方法，只要使用簡單的邏輯電路，就可以量測出每一條 Post-Bond 後連接線的大概速度
		出廠後的連接線隨時速度監控	提早偵測到【異常早衰的瑕疵】和【提早老化的瑕疵】，以提早做因應

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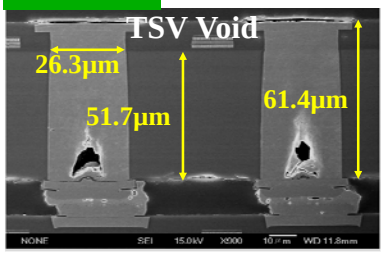
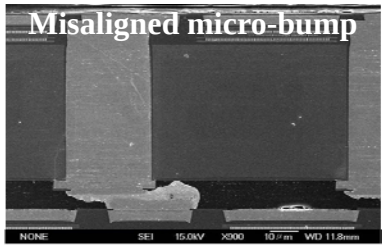
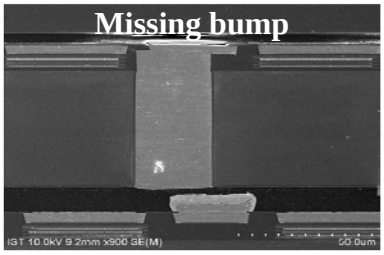
SEM Photos of TSV Defects
(0.18um Through Silicon Stacking at ITRI)

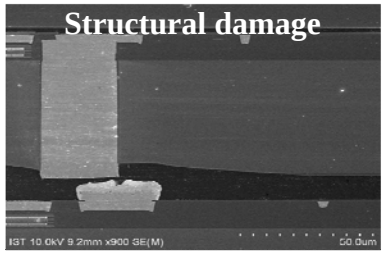
A partially faulty TSV may not operate as fast as we expect (and it could deteriorate over time…)

Source: ITRI









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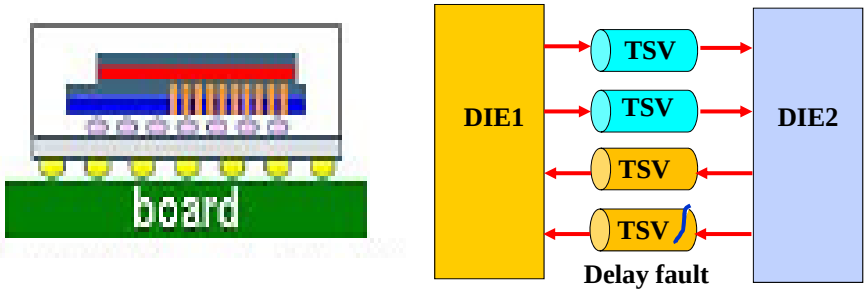
Post-Bond Die-to-Die Interconnect Testing

Problem Addressed:

To develop a low-cost method to test the delay fault associated with the TSV

也就是說，我們必須先了解每一根 Die-to-Die 連接線的速度.



3D-IC using TSVs

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Die-to-Die Interconnect Testing 相關著作

IS: Input-Sensitivity Analysis
VOT: Variable Output Threshold Based Analysis

Methods	Basic Concepts	Publications
IS-Based Pre-Bond Test	Capacitance Characterization (to support one-sided testing)	ATS'10, ATS'13 TVLSI'13, TCAD'13
VOT-Based Post-Bond Test	Delay Characterization	DAC'12, ITC'12, ITC'13, DATE'15, TCAD'13 TCAD'14
Pulse-Vanishing Test (PV-Test)	Use short-pulse as test stimulus Pulse-vanishing implies a fault	IOLTS'13, ETS'14 TCAD'14
Leakage Binning	By PLL-based timing control	ATS'12, TCAD'13, D&T'14
On-Line Delay Monitoring	By a non-intrusive transition-time binning circuit	ATS'14

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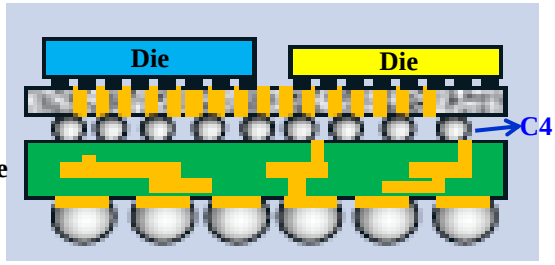
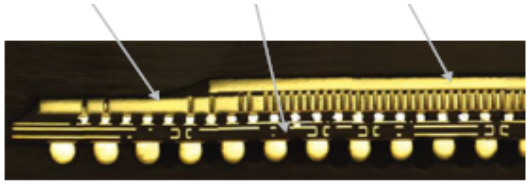
Interposer-Based 2.5D-ICs

CoWoS (Chip-on-Wafer-on-Substrate) – TSMC



Concern: How good is the power delivery network?



2.5D silicon Interposer, Cross Section
(Courtesy of ASE)

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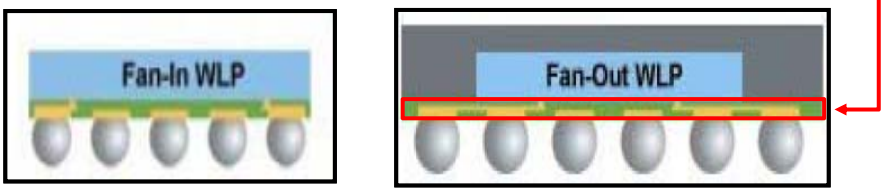
Wafer-Level Processing using RDL (Lower-Cost Die-to-Die Integration)

RDL (Re-Distribution Layer) between bare dies and solder balls



RDL: used to route the signal path from the die's IOs to desired bump locations

Concern: How good is the power delivery network?

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未來的展望

- **Almost Cell-Based Timing Circuits and Their Compiler**
  - **Delay-Locked Loop Compiler**
  - **Time-Digital Converter (TDC) Compiler**
  - **Programmable Phase-Shifter Compiler**
- **PVTA (匹夫塔效應) Monitoring Methodology**
  - **Tracking the On-Chip Process, Temperature, Voltage Drop, and Aging Effects**
- **Interconnect Testing, Repair, and Monitoring**
  - **To Identify Parametric Faults (resistive or leakage faults)**
  - **To Repair them on-the-fly**
  - **To Keep track of any over-aging phenomenon**

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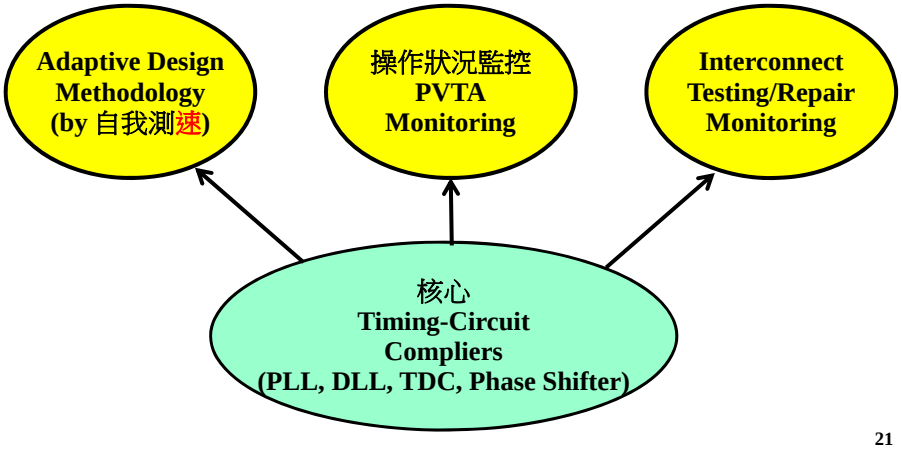
Questions to be Answered...

Question: 如何安客戶的心，讓他們相信【先進製程，多裸晶整合的晶片】是可以具有高可靠度的呢?

Perspective: 必須投資在更多的 **Design-for-X** 的技術上…



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