

Dr. 黃錫瑜 (Shi-Yu Huang) received his B.S. and M.S. degrees in Electrical Engineering from National Taiwan University in 1988 and 1992, respectively, and his Ph.D. degree in Electrical and Computer Engineering from University of California, Santa Barbara, in 1997. He joined the faculty of Electrical Engineering Department, National Tsing Hua University, Taiwan, in 1999, where he is currently Professor and serving as Director of Design Technology Center.

His research interests broadly cover VLSI design, automation, and testing, with prior experiences on formal verification, power estimation, fault diagnosis, and resilient nanometer SRAM Design. More recently, his research is concentrated on all-digital timing circuit designs, such as all-digital phase-locked loop (PLL), all-digital delay-locked loop (DLL), time-to-digital converter (TDC), and their applications to parametric fault testing and reliability enhancement for 3D-ICs. He has published more than 120 refereed technical papers.

Dr. Huang ever co-founded a company, TinnoTek Inc. (2007-2012), specializing a cell-based PLL compiler and system-level power estimation tools. He was a co-recipient of the best-presentation or best-paper award from IEEE Symposium on VLSI Design, Automation, and Test as in 2006 and 2013, respectively. Dr. Huang has actively served in the IEEE community, participating in IEEE Asian Test Symposium, as Program Co-Chair in 2004, and General Co-Chair in 2009, serving as Program Chair for IEEE International Workshop on Memory Technology, Design, and Testing in 2005 and 2006, and Program Co-Chair in 2014, and General Co-Chair in 2015 for IEEE Symposium on VLSI Design, Automation, and Test. He is now serving as an Associate Editor for IEEE Trans. on Computers.