Curriculum Vitae

Shi-Yu Huang

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1. Current Position in National Tsing Hua University:

- Professor & Director of Design Technology Center @ National Tsing Hua U., Taiwan

2. Education

- **B.S. (Sept. 1984 ~ June 1988)**
  Electrical Engineering Dept., **National Taiwan University, Taiwan**
- **M.S. (Sept. 1990 ~ June 1992)**
  Electrical Engineering Dept., **National Taiwan University, Taiwan**
- **Ph.D. (Sept. 1992 ~ Aug. 1997)**
  Electrical and Computer Engineering Dept., **U. of California, Santa Barbara, U.S.A.**

3. Working Experiences

- **Aug. 2008 ~ Now**
  Professor of **EE Department, National Tsing-Hua University, Taiwan**
- **Feb. 2002 ~ Aug. 2008**
  Associate Professor of **EE Department, National Tsing-Hua University, Taiwan**
- **Aug. 1999 ~ Feb. 2002**
  Assistant Professor of **EE Department, National Tsing-Hua University, Taiwan**
- **July 1998 ~ July 1999**
  Principle Engineer at **Worldwide Semiconductor Manufacturing Corp., Taiwan,** Working on Built-in-self-test (BIST) design for embedded DRAMs and SRAMs.
- **Oct. 1997 ~ July 1998**
  Senior Engineer at **National Semiconductor Corporation, USA** (in System-on-a-chip design methodology group).

4. Academic Services:

(IEEE Services)

- Program Co-Chair, IEEE Asian Test Symposium, 2004.
- Program Chair, IEEE Memory Technology, Design, and Testing (MTDT), 2005.
- Program Chair, IEEE Memory Technology, Design, and Testing (MTDT), 2006.
- General Co-Chair, IEEE Asian Test Symposium, 2009.
- Program Co-Chair, IEEE Int'l Symp. on VLSI Design, Automation, and Test, 2014.
- General Co-Chair, IEEE Int'l Symp. on VLSI Design, Automation, and Test, 2015.
- Program Committee Members for ATS (2005-2011, 2013-2015), VLSI-DAT (2006-2012), ASP-DAC (2009-2012), DATE (2009), CODES+ISSS (2011-2012)
- Steering Committee Member for Asian Test Symposium (2008-2015)
- Associate Editor, IEEE Transactions on Computers (2015~)

(Administrative Services @ National Tsing Hua University (NTHU), Taiwan)

- 2005 ~ 2007, Deputy Director, Design Technology Center (DTC), NTHU.
- Feb. 2007 ~ Jan. 2010, Deputy Chairman of Electrical Engineering (EE) Dept., NTHU
- Aug. 2008 ~ Jan. 2010, Director of EECS Undergraduate Program, NTHU
- Aug. 2014 ~ July 2016, Director, Design Technology Center (DTC), NTHU
- Aug. 2016 ~ Now, Director, Center of Innovative Incubator (CII), NTHU

5. Technical Expertise

- **Electronic Design Automation:**
  (1) Formal Equivalence Checking
  (2) Design Re-synthesis for ECO
  (3) Mixed-Level Power Estimation
  (4) SRAM Compiler
  (5) Phase-Locked Loop Compiler
- **IC Design:**
  (1) Process Resilient SRAM Design for Nanometer Process Technologies
  (2) Portable Cell-Based All-Digital PLL (Phase-Locked Loop) Design and its variants (e.g., long-distance clock synchronization for 3D IC, 10ps-resolution multi-phase clock generation, Deskewing duty-cycle correction circuit, etc)
- **VLSI Testing:**
  (1) Fault Diagnosis (include logical faults and scan chain faults)
  (2) Low-Power Test Compression Methodology
  (3) Built-In Speed Grading (BISG) Methodoogy for Memories and Logic Circuits
  (4) Cell-Based Timing Measurement
  (5) Parametric Fault Testing of Die-to-Die Interconnects (TSV or Interposer Wires) in 3D ICs

6. Honors

- *2006 Best Presentation Award* from IEEE Int'l Symp. of VLSI Design, Automation, and Test
  L.-Y. Ko, S.-Y. Huang, J.-J. Chiou, and H.-C. Cheng, "Modeling and Testing of Intra-Cell Bridging Defects Using Butterfly Structure," *Proc. of VLSI Design, Automation, and Testing* (VLSI-DAT), pp. 159-162, (April 2006).

- *2013 Best Paper Award* from IEEE Int'l Symp. of VLSI Design Automation, and Test.
  C.-H. Hsu, S.-Y. Huang, D.-M. Kwai, and Y.-F. Chou, "Worst-Case IR-Drop Monitoring with 1GHz Sampling Rate," *Proc. of VLSI Design, Automation, and Test* (VLSI-DAT), (April 2013).

- *2014 Best Paper Award* from IEEE Asian Test Symposium, S.-Y. Huang, H.-X. Li, Z.-F. Zeng, K.-H. Tsai, and W.-T. Cheng, "On-Line Transition-Time Monitoring for Die-to-Die Interconnects in 3D ICs", Proc. of Asian Test Symp. (ATS), pp. 162-167, (Nov. 2014).

7. Publications

Table 1: Publication Summary

Types of Publications	Number
Book	1
Book Chapter	1
Journal Publications	51 (37 IEEE journals)
Conference Papers	84

- **(Book and Book Chapter)**

1. S.-Y. Huang, and K.-T. Cheng, "Formal Equivalence Checking and Design Debugging", Kluwer Academic Publishers, (June 1998)
2. S.-Y. Huang, Chapter 7 - Logic Diagnosis of "VLSI Test Principles and Architectures - Design for Testability," Edited by L.-T. Wang, C.-W. Wu, and X. Wen, Morgan Kaufmann Publishers, pp. 397-460, (June 2006).
3. Book Chapter on " Interconnect Testing for 2.5D- and 3D-SICs", (in press).

- **(Journal Papers)**

1. S.-Y. Huang and K.-T. Cheng, "ErrorTracer: A Fault-Simulation-Based Approach to Design Error Diagnosis", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, pp. 1341-1352, (Sept. 1999).
2. S.-Y. Huang, K.-C. Chen and K.-T. Cheng, "AutoFix: A Hybrid Tool for Automatic Logic Rectification", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, pp. 1375-1384, (Sept. 1999).
3. K.-T. Cheng, S.-Y. Huang, and W.-J. Dai, "Fault Emulation: A New Methodology for Fault Grading," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, pp. 1487-1495, (Oct. 1999).
4. S.-Y. Huang, K.-T. Cheng, K.-C. Chen, C.-Y. Huang, and F. Brewer, "AQUILA: An Equivalence Checking System for Large Sequential Designs," IEEE Trans. on Computers, pp. 443-464, (May 2000).
5. S.-Y. Huang, K.-T. Cheng, K.-C. Chen, "Verifying Sequential Equivalence Using ATPG techniques," ACM Trans. on Design Automation of Electronic Systems, pp. 244-275, (April 2001).
6. S.-Y. Huang, D.-M. Kwai, and C. Huang, "A High-Speed Architecture For At-Speed DRAM Testing," Journal of The Chinese Institute of Electrical Engineering, Vol. 8, No. 4, pp. 387-394, (Nov. 2001).
7. S.-Y. Huang, "Improving the Timing of Extended Finite State Machines Via Catalyst," VLSI Design Journal, Vol. 15, No. 3, pp. 629-636, (Nov. 2002).
8. S.-Y. Huang, "A Symbolic Inject-And-Evaluate Paradigm for Byzantine Fault Diagnosis", Journal of Electronic Testing, Theory and Applications (JETTA), Vol. 19, No. 2, pp. 161-172, (April 2003).
9. H.-C. Kao, M.-F. Tsai, S.-Y. Huang, C.-W. Wu, W.-F. Chang, and S.-K. Lu, "Efficient Double Fault Diagnosis for CMOS Logic Circuits With A Specific Application To Generic Bridging Faults", Journal of Information Science and Engineering (JISE), pp.

571-586, Vol. 19, No. 4, (July 2003).

10. S.-Y. Huang and C.-J. Liu, "A Low-Power Architecture For Extended Finite State Machines Using Input Gating," IEICE Trans. on Fundamentals, pp. 3109-3115, Vol. E87-A, No. 12, (Dec. 2004).
11. Y.-J. Juang, S.-F. Chen, S.-Y. Huang, Y.-C. King, "A Low-Cost Logarithmic CMOS Image Sensor Design By Nonlinear Analog-To-Digital Conversion", IEEE Trans. on Consumer Electronics, Vol. 51, No. 4, pp. 1212-1217, (Nov. 2005).
12. K.-H. Lai, S.-Y. Huang, and P.-C. Chiang, "A Sizing Methodology for the Charge Noise Reduction of a Comparator," Int'l Journal of Electrical Engineering, Vol. 13, No. 1, pp. 1-7, (Feb. 2006).
13. C.-H. Lai, Y.-C. King, and S.-Y. Huang, "A 1.2V 0.25um Clock Output Pixel Architecture With Dynamic Range and Self-Offset Cancellation," IEEE Sensors Journal, pp. 398-405, Vol. 6, No. 2, (April 2006).
14. Y.-C. Lin and S.-Y. Huang, "Accurate Whole-Chip Diagnostic Strategy for Scan Designs with Multiple Faults," Journal of Electronic Testing: Theory and Applications (JETTA), Vol. 22, No. 2, pp. 151-159, (April 2006).
15. Y.-T. Lin and S.-Y. Huang, "Low-Power Adaptive FIR Filter Generator Using Bit-Oriented Structures," IEE Proceedings Circuits, Devices, and Systems, Vol. 153, No. 2, pp. 167-172, (April 2006).
16. H.-B. Wang, S.-Y. Huang, and J.-R. Huang, "A Modified Inject-and-Evaluate Paradigm for Diagnosing Gate-Delay Faults", Int'l Journal of Electrical Engineering, Vol. 13, No. 2, pp. 185-191, (May 2006).
17. C.-W. Tzeng and S.-Y. Huang, "Diagnosis by Image Recovery: Finding Mixed Multiple Timing Faults in a Scan Chain," IEEE Trans. on Circuits and Systems II: Express Briefs (TCAS-II), Vol. 54, No. 8, pp. 690-694, (Aug. 2007).
18. C.-F. Chen, S.-Y. Huang, and Y.-C. King, "Built-In Self-Repair for Die-to-Die Misalignment for Multi-Die Space Sensors," IEEE Sensors Journal, Vol. 7, No. 9, pp. 1354-1355, (Sept. 2007).
19. C.-W. Tzeng, J.-J. Hsu, and S.-Y. Huang, "A Robust Paradigm for Diagnosing Hold-Time Faults in Scan Chains," IET Proc. on Computers and Digital Techniques, Vol. 1, No. 6, pp. 706-715, (Nov. 2007).
20. C.-W. Tzeng, J.-S. Yang, and S.-Y. Huang, "A Versatile Paradigm for Scan Chain Diagnosis of Complex Faults Using Signal Processing Techniques," ACM Trans. on Design Automation of Electronic Systems (TODAES), Vol. 13, No. 1, pp. 9.1-9.27, (Jan. 2008).
21. C.-W. Tzeng and S.-Y. Huang, "UMC-Scan Test Methodology - Exploiting the Maximum Freedom of Multicasting", IEEE Design and Test of Computers (D&T), Vol. 25, No. 2, pp. 132-140, (March-April, 2008).
22. S.-P. Cheng and S.-Y. Huang, "A Low-Power SRAM for Viterbi Decoder in Wireless Communication," IEEE Trans. on Consumer Electronics, Vol. 54, No. 2, pp. 290-295, (May 2008).
23. Y.-C. Lai and S.-Y. Huang, "X-Calibration: A Robust Technique for Combating Excessive Bitline Leakage Current in Nanometer SRAM Designs", IEEE Journal of Solid-State Circuits (JSSC), Vol. 43, No. 9, pp. 1964-1971, (Sept. 2008).
24. Y.-C. Lai and S.-Y. Huang, "A Resilient and Power Efficient Automatic-Power-Down

Sense Amplifier for SRAM Design", IEEE Trans. on Circuits and Systems II: Express Briefs (TCAS-II), Vol. 55, No. 10, pp. 1031-1035, (Oct. 2008).

25. Y.-C. Lai and S.-Y. Huang, "Robust SRAM Design via BIST-Assisted Timing-Tracking (BATT)", IEEE Journal of Solid-State Circuits (JSSC), Vol. 44, No. 2, pp. 642-649, (Feb. 2009).
26. C.-W. Tzeng, H.-C. Cheng, and S.-Y. Huang, "Layout-Based Defect-Driven Diagnosis for Intra-Cell Bridging Defects," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Vol. 28, No. 5, pp. 764-769, (May 2009).
27. Y.-C. Lai, S.-Y. Huang, and H.-J. Hsu, "Resilient Self-VDD-Tuning Scheme with Speed Margining for Low-Power SRAM", IEEE Journal of Solid-State Circuits (JSSC), Vol. 44, No. 10, pp. 2817-2823, (Oct. 2009).
28. C.-W. Tzeng and S.-Y. Huang, "QC-Fill: Quick-and-Cool X-Filling for Multicasting-Based Scan Test," IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems (TCAD), Vol. 28, No. 11, pp. 1756-1766, (Nov. 2009).
29. H.-J. Hsu and S.-Y. Huang, "A Low-Jitter ADPLL via a Suppressive Digital Filter and an Interpolation-Based Locking Scheme," IEEE Trans. on VLSI Systems (TVLSI), Vol. 17, No. 11, pp. 165-170, (Nov. 2009).
30. C.-W. Tzeng and S.-Y. Huang, "Split-Masking: An Output Masking Scheme for Effective Compound Defect Diagnosis in Scan Architecture with Test Compression," IEEE Trans on Computer Aided Design of Integrated Circuits and Systems (TCAD), Vol. 29, No. 5, pp. 834-839, (May 2010).
31. C.-H. Lo and S.-Y. Huang, "P-P-N Based 10T SRAM Cell for Low-Leakage and Resilient Sub-Threshold Operation," IEEE Journal of Solid-State Circuits (JSSC), Vol. 46, No. 3, pp. 695-704, (March, 2011).
32. Bor-Woei Kuo, Hsun-Hao Chang, Yung-Chang Chen, and Shi-Yu Huang, "A Light-and-Fast SLAM Algorithm for Robots in Indoor Environments Using Line Segment Map," Journal of Robotics, (WEB-LINKING) Volume 2011, Article ID 257852, 12 pages, (2011).
33. S.-K. Lu, Y. Chen, S.-Y. Huang, and C.-W. Wu, "Speeding Up Emulation-Based Diagnosis Techniques for Logic Cores," IEEE Design & Test of Computers (D&T), Vol. 28, No. 4, pp. 88-97, (July-Aug. 2011).
34. F.-C. Huang, S.-Y. Huang, J.-W. Ker, and Y.-C. Chen, "High-Performance SIFT Hardware Accelerator for Real-Time Image Feature Extraction", IEEE Trans. on Circuits and System for Video Technology (TCAS-VT), Vol. 22, No. 3, pp. 340-351, (March 2012).
35. T.-Y. Li, S.-Y. Huang, H.-J. Hsu, C.-W. Tzeng, C.-T. Huang, J.-J. Liou, H.-P. Ma, P.-C. Huang, J.-C. Bor, C.-C. Tien, and M. Wang, and C.-W. Wu, "AC-Plus Scan Methodology for Small Delay Testing and Characterization," IEEE Trans. on VLSI Systems (TVLSI), Vol. 21, No. 2, pp. 329-341, (Feb. 2013).
36. J.-W. You, S.-Y. Huang, Y.-H. Lin, M.-H. Tsai, D.-M. Kwai, Y.-F. Chou, and C.-W. Wu, "In-Situ Method for TSV Delay Testing and Characterization Using Input Sensitivity Analysis," IEEE Trans. on VLSI Systems (TVLSI), Vol. 21, No. 3, pp. 443-453, (March 2013).
37. J.-W. Ke, S.-Y. Huang, C.-W. Tzeng, D.-M. Kwai, and Y.-F. Chou, "Die-to-Die Clock Synchronization for 3D IC using Dual Locking Mechanism," IEEE Trans. on Circuits and Systems - Part I, (TCAS-I), Vol. 60, No. 4, pp. 908-917, (April 2013).

38. Y.-H. Lin, S.-Y. Huang, K.-H. Tsai, W.-T. Cheng, S. Sunter, Y.-F. Chou, and D.-M. Kwai, "Parametric Delay Test of Post-Bond TSVs in 3-D ICs via VOT Analysis", IEEE Trans. on Computer-Aided Design of Electronic Circuits (TCAD), Vol. 32, No. 5, pp.-737-747, (May 2013).

39. S.-Y. Huang, Y.-H. Lin, Li-Ren Huang, K.-H. Tsai, and W.-T. Cheng, "Programmable Leakage Test and Binning for TSVs with Self-Timed Timing Control", to appear in IEEE Trans. on Computer-Aided Design of Electronic Circuits (TCAD), Vol. 32, No. 8, pp. 1265-1273, (Aug. 2013).

40. L.-R. Huang, S.-Y. Huang, S. Sunter, K.-H. Tsai, and W.-T. Cheng "Oscillation-Based Pre-Bond TSV Test," IEEE Trans. on Computer-Aided Design of Electronic Circuits (TCAD). Vol. 32, No. 9, pp. 1440-1444, (Sept. 2013).

41. R.-T. Ding, S.-Y. Huang, and C.-W. Tzeng, "Cell-Based Process Resilient Multi-Phase Clock Generation", IEEE Trans. on VLSI Systems (TVLSI), Vol. 21, No. 12, (Dec. 2013).

42. P.-Y. Chao, C.-W. Tzeng, S.-Y. Huang, C.-C. Weng, and S.-C. Fang, "Process Resilient Low-Jitter All-Digital PLL via Smooth Code Jumping", IEEE Trans. on VLSI Systems (TVLSI), Vol. 21, No. 12, (Dec. 2013).

43. L.-R. Huang, S.-Y. Huang, K.-H. (Hans) Tsai, and W.-T. Cheng, "Parametric Fault Testing and Performance Characterization of Post-Bond Interposer Wires in 2.5-D ICs", IEEE Trans. on Computer-Aided Design of Electronic Circuits (TCAD), Vol. 33, No. 3, pp. 476-488, (March 2014).

44. C.-W. Tzeng, S.-Y. Huang, P.-Y. Chao, and R.-T. Ding, "Parameterized All-Digital PLL Architecture and Its Compiler to Support Easy Process Migration," IEEE Trans. on VLSI Systems (TVLSI), Vol. 22, No. 3, pp. 621-630, (March 2014).

45. S.-Y. Huang, J.-Y. Lee, K.-H. (Hans) Tsai, and W.-T. Cheng, "Pulse-Vanishing Test for Interposers Wires in 2.5-D IC", IEEE Trans. on Computer-Aided Design of Electronic Circuits(TCAD), Vol. 33, No. 8, pp. 1258-1268, (Aug. 2014).

46. S.-Y. Huang and Li-Ren Huang, "PLL-Assisted Timing Circuit for Accurate TSV Leakage Binning," IEEE Design and Test of Computers (D&T), Vol. 31, No. 4, pp. 36-42, (2014).

47. C.-Y. Lin, C.-W. Huang, C.-B. Kuan, S.-Y. Huang, and J.-K. Lee, "The Design and Experiments of A SID-Based Power-Aware Simulator for Embedded Multi-Core Systems," ACM Trans. on Design Automation of Electronic Systems (TODAES), Vol. 20, No. 2, Article 22, (Feb. 2015).

48. S.-Y. Huang, M.-T. Tsai, Z.-F. Zeng, K.-H. (Hans) Tsai, and W.-T. Cheng, "General Timing-Aware Built-In Self-Repair for Die-to-Die Interconnects," *IEEE Trans. on Computer-Aided Design of Electronic Circuits* (TCAD), Vol. 34, No 11, pp. 1836-1846, (Nov. 2015).

49. S.-Y. Huang, M.-T. Tsai, H.-X. Li, Z.-F. Zeng, K.-H. (Hans) Tsai, and W-.T. Cheng, "Non-Intrusive On-Line Transition-Time Binning and Timing Failure Threat Detection for Die-to-Die Interconnects," *IEEE Trans. on Computer-Aided Design of Electronic Circuits* (TCAD), Vol. 34, No 12, pp. 2039-2048, (Dec. 2015).

50. S.-Y. Huang, M.-T. Tsai, K.-H. (Hans) Tsai, and W.-T. Cheng, "Delay Characterization and Testing of Arbitrary Multiple-Pin Interconnects," *IEEE Design and Test of Computers* (D&T), Vol. 33, No. 2, pp. 9-16, (April 2016).

51. S.-T. Tseng, Y.-H. Kao, C.-C. Peng, J.-Y. Liu, S.-C. Chu, G.-F. Hong, C.-H. Hsieh, K.-T.

Hsu, W.-T. Liu, Y.-H. Huang, S.-Y. Huang, and T.-S. Chu, "A 65nm CMOS Low Power Impulse Radar System for Human Respiratory Feature Extraction and Diagnosis on Respiratory Diseases", *IEEE Transactions on Microwave Theory and Techniques*, (Accepted for publication).

52. S.-Y. Huang, C.-C. Cheng, M.-T. Tsai, K.-C. Huang, K.-H. Tsai, and W.-T. Cheng, "Versatile Transition-Time Monitoring for Interconnects via Distributed TDC", *IEEE Design and Test* (D&T), Vol. 33, No. 5, (2016).

(Conference Papers)

1. K.-T. Cheng, S.-Y. Huang, and W.-J. Dai, "Fault Emulation: A Novel Approach to Fault Grading", Proc. Int'l Conf. on Computer-Aided Design, pp. 681-686, (Nov. 1995). abstract
2. S.-Y. Huang, K.-T. Cheng, and K.-C. Chen, "On Verifying the Correctness of Retimed Circuits", Proc. of Great-Lake Symposium on VLSI, pp. 277-281, (March 1996). abstract
3. S.-Y. Huang, K.-C. Chen, K.-T. Cheng, and T.-C. Lee, "Vector Generation for Accurate Power Simulation", Proc. of IEEE/ACM Design Automation Conf., pp. 161-164, (June. 1996). abstract
4. S.-Y. Huang, K.-C. Chen, and K.-T. Cheng, "Error Correction Based on Verification Techniques", Proc. of IEEE/ACM Design Automation Conf., pp. 258-261, (June. 1996). abstract
5. S.-Y. Huang, K.-T. Cheng, K.-C. Chen, and T.-C. Lee, "A Novel Methodology for Transistor-level Power Simulation", Int'l Symposium on Lower Power Electronic Design, pp. 67-72, (Aug. 1996). abstract
6. S.-Y. Huang, K.-T. Cheng and K.-C. Chen, "An ATPG-based Framework for Verifying Sequential Equivalence", Proc. Int'l Test Conf., pp. 865-874, (Oct. 1996). abstract
7. S.-Y. Huang, K.-T. Cheng and K.-C. Chen, "AQUILA: An Equivalence Verifier for Large Sequential Circuits", Proc. of Asia and South Pacific Design Automation Conf., pp. 455-460, (Jan. 1997). abstract
8. S.-Y. Huang, K.-C. Chen, and K.-T. Cheng, "Incremental Logic Rectification", Proc. of VLSI Test Symposium, pp. 134-139, (April 1997). abstract
9. S.-Y. Huang, K.-T. Cheng, K.-C. Chen, and D. I. Cheng, "ErrorTracer: A Fault Simulation Based Approach to Design Error Diagnosis", Proc. of Int'l Test Conf., pp. 974-981, (Nov. 1997).
10. Y.-M. Jiang, S.-Y. Huang, K.-T. Cheng, D. C. Wang, and C.-Y. Ho, "A Hybrid Power Model for RTL Power Estimation", Proc. of Asia and South Pacific Design Automation Conf., pp. 551-556, (Feb. 1998).
11. S.-Y. Huang, K.-T. Cheng, and K.-C. Chen, "General Design Error Diagnosis for Sequential Circuits", Proc. of IEEE/ACM Design Automatic Conf., pp. 632-637, (June 1998).
12. Yi-Min Jiang, S.-Y. Huang, K.-T. Cheng, and D.-C. Wang, C.-Y. Ho, "A Hybrid Power Model For RTL Power Estimation," Proc. of Asia and South Pacific Design Automation Conf., pp. 551-556, (Feb. 1998).
13. S.-Y. Huang and D.-M. Kwai, "A High-Speed Built-In Self-Test Design for DRAMs", Proc. of Int'l Symposium on VLSI-TSA (Technology, Systems, and Applications), pp.

50-53, (June 1999).

14. S.-Y. Huang, "On Speeding Up Finite State Machines Using Catalyst Circuitry", Proc. of Asia and South Pacific Design Automation Conf. (ASP-DAC), 583-588, (Jan. 2001).

15. S.-Y. Huang, "Towards The Logic Defect Diagnosis For Partial-Scan Designs", Proc. of Asia and South Pacific Design Automation Conf. (ASP-DAC), pp. 313-318, (Jan. 2001).

16. S.-Y. Huang, "On Improving the Accuracy of Multiple Defect Diagnosis", Proc. of VLSI Test Symposium (VTS), pp. 34-39, (April 2001).

17. C.-J. Liu and S.-Y. Huang, "Low-Power Synthesis For Extended Finite State Machines," Proc. of 12th VLSI/CAD Symposium, Taiwan, (Aug. 2001).

18. C.-C. Lu and S.-Y. Huang, "Improving the Accuracy of Mixed-Level Power Estimation for CMOS Logic Circuits With Power Management," Proc. of 12th VLSI/CAD Symposium, Taiwan, (Aug. 2001).

19. H.-C. Kao, M.-F. Tsai, S.-Y. Huang, C.-W. Wu, W.-F. Chang, and S.-K. Lu, "Efficient Double Fault Diagnosis For CMOS Logic Circuits," Proc. of 12th VLSI/CAD Symposium, Taiwan, (Aug. 2001).

20. C.-W. Wang, R.-S. Tzeng, C.-F. Wu, C.-T. Huang, C.-W. Wu, S.-Y. Huang, S.-H. Lin, and H.-P. Wang, "A Built-In Self-Test and Self-Diagnosis Scheme for Heterogeneous SRAM Clusters," Proc. of Asian Test Symposium, pp. 103-108, (Nov. 2001).

21. S.-Y. Huang, "Speeding Up The Byzantine Fault Diagnosis Using Symbolic Simulation," Proc. of VLSI Test Symposium, pp. 193-198, (April 2002).

22. Y.-C. Tsai, S.-Y. Huang, C.-P. Su, C.-T. Huang, and C.-W. Wu, "Fine-Grain Mixed-Level Power Estimation Based On Disparity Path Analysis," Proc. of 12th VLSI/CAD Symposium, Taiwan, (Aug. 2002).

23. H.-B. Wang, S.-Y. Huang, and J.-R. Huang, "Gate-Delay Fault Diagnosis Using The Inject-And-Evaluate Paradigm For Full-Scan Designs", Proc. of Int'l Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'02), (Nov. 2002).

24. S.-Y. Huang, "Diagnosis Of Byzantine Open-Segment Faults," Proc. of Asian Test Symposium, pp. 248-253, (Nov. 2002).

25. M.-L. Lee, T.-T. Hwang, and S.-Y. Huang, "Decomposition of Extended Finite State Machine For Low-Power Design," Proc. of Design Automation and Test in Europe, pp. 1152-1153, (2003).

26. S.-K Lu, J.-L. Chen, C.-W. Wu, K.-F. Chang, and S.-Y. Huang, "Combinational Circuit Fault Diagnosis Using Logic Emulation," Proc. of Int'l Symp. on Circuits and Systems, Vol. 5, pp. 549-552, May 2003.

27. S.-F. Chen, Y.-J. Juang, S.-Y. Huang, and Y.-C. King, "Logarithmic CMOS Image Sensor Through Multi-Resolution Analog-To-Digital Conversion," Proc. of Int'l Symposium on VLSI Technology, Systems, and Applications, pp. 227-230, (April 2003).

28. Y.-T. Lin and S.-Y. Huang, "Efficient Bit-Oriented Implementation of FIR Filters Using A New Compressor," Proc. of Int'l SOC Conf., pp.269-271, (Sept. 2003).

29. B.-R. Lin, S.-Y. Huang, C.-H. Lai, and Y.-C. King, "A High Dynamic Range CMOS Image Sensor Design Based On Two-Frame Composition," Proc. of Int'l SOC Conf., pp. 389-392, (Sept. 2003).

30. Y.-C. Lin and S.-Y. Huang, "Chip-Level Diagnostic Strategy For Full-Scan Designs With Multiple Faults," Proc. of Asian Test Symposium, pp. 38-44, (Nov. 2003).

31. S.-Y. Huang, "A Fading Algorithm For Sequential Fault Diagnosis," to appear in Proc. of In'l Symposium on Defect and Fault Tolerance on VLSI Systems, pp. 139-147, (Nov. 2004).

32. K.-H. Lai, S.-Y. Huang, P.-C. Chiang, "A Sizing Methodology For A Low-Noise Comparator," Proc. of Asia-Pacific Conf. on Circuits and Systems, pp. 253-256, (Dec. 2004).

33. M.-Y. Sum, S.-Y. Huang, C.-C. Weng, and K.-S. Chang, "Accurate RT-Level Power Estimation Using Up-Down Encoding," Proc. of Asia-Pacific Conf. on Circuits and Systems, pp. 69-72, (Dec. 2004).

34. Y.-F. Lee, S.-Y. Huang, S.-Y. Hsu, I.-L. Chen, C.-T. Shieh, J.-C. Lin, S.-C. Chang, "Power Estimation Strategies For A Low-Power Security Processor," Proc. of Asia-Pacific Design Automation Conf. (ASP-DAC), pp. 367-371, (Jan. 2005).

35. M.-Y. Sum, K.-S. Chang, C.-C. Weng, and S.-Y. Huang, "ToggleFinder: Accurate RTL Power Estimation For Large Designs," Int'l Symposium on VLSI Design, Automation, and Test, (VLSI-DAT), pp. 16-19, (April 2005).

36. S.-P. Cheng and S.-Y. Huang, "A Low-Power SRAM Design Using Quiet-Bitline Architecture," Proc. of IEEE Int'l Workshop on Memory Technology, Design, and Testing, (MTDT), (Aug. 2005).

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