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1. 學歷

- ◆ 台灣大學 電機系 學士 (Sept. 1984 ~ June 1988)
- ◆ 台灣大學 電機系 碩士 (Sept. 1990 ~ June 1992)
- ◆ 美國加州大學，聖塔巴巴拉分校 博士 (Sept. 1992~ June 1997)

2. 工作經歷

- ◆ Oct. 1997 ~ July 1998 National Semiconductor, USA, 資深工程師
- ◆ July 1998 ~ July 1999 世大積體電路公司(後併入台積電), 主任工程師
- ◆ Aug. 1999 ~ Feb. 2002 清華大學電機系 助理教授
- ◆ Feb. 2002 ~ Aug. 2008 清華大學電機系 副教授
- ◆ Aug. 2008 ~ Now 清華大學電機系 教授

3. 行政服務經驗

- ◆ Feb. 2005 ~ Feb. 2007 清華大學積體電路設計技術中心副主任
- ◆ Dec. 2006 ~ Feb. 2010 清華大學電機系副系主任
- ◆ Aug. 2008 ~ Feb. 2010 清華大學電資院學士班班主任
- ◆ Aug. 2014 ~ July 2016 清華大學積體電路設計技術中心主任
- ◆ Aug. 2016 ~ Now 清華大學創新育成中心主任

4. 學術服務經驗

- ◆ Jan. 2003 ~ Dec. 2004, Treasurer (財務長) of IEEE Taipei Section
- ◆ Jan. 2004 ~ Dec. 2004, 教育部 VLSI 教育改進計劃 - 『EDA 聯盟』執行秘書
- ◆ Jan. 2005 ~ Dec. 2005, 教育部 VLSI 人才培育先導型計劃 - 『SOC 總聯盟』執行秘書
- ◆ 主辦 2004 年 IEEE Asian Test Symposium 擔任共同議程主席(Program Co-Chair)。
- ◆ 主辦 2005, 2006 年 IEEE Workshop on Memory Technology, Design, and Testing (MTDT) 擔任議程主席(Program Chair)。
- ◆ 協辦 2009 年 IEEE Asian Test Symposium 擔任共同大會主席(General Co-Chair)。
- ◆ 擔任 2008, 2009, 2010, 2011, 2013, 2014, 2015, 2016 年 IEEE Asian Test Symposium 之議程委員 (PC Member)。
- ◆ 擔任 2008-2013 年 IEEE VLSI-DAT 會議之議程委員 (PC Member)。
- ◆ 擔任 2009-2012 年 IEEE ASP-DAC 之議程委員 (PC Member)。
- ◆ 擔任 2009 年 IEEE DATE 會議議程委員 (PC Member)。
- ◆ 擔任 2011-2012 年 IEEE CODES+ISSS 會議議程委員 (PC Member)。

- ◆ 擔任 2008-2016 年亞洲測試會議之指導委員會委員 (Steering Committee Member)
- ◆ 2005 ~ Now, 擔任 Associate Editor, IEEE Transactions on Computers.

5. 榮譽

- ◆ 2006 年 **Best Presentation Award** of IEEE Symposium on VLSI Design, Automation, and Testing, Paper Title: **【Modeling and Testing of Intra-Cell Bridging Defects Using Butterfly Structure】**.
- ◆ 2006 年-2009 年: 主持國科會晶片系統國家型整合型計畫**【奈米級晶片之良率與可靠度提昇方法研究】**，獲評選為**【績優計畫第三名】**。
- ◆ 2009 年-2011 年: 參與李政崑教授主持之國科會晶片系統國家型整合型計畫**【前瞻異質多核心系統開發工具研發】**，負責**【子計畫四：適用於多核心數位訊號處理系統晶片之功率消耗評估軟體工具研發】**，該整合型計畫獲評選為**【績優計畫第一名】**。
- ◆ 2013 年 IEEE Symposium on VLSI Design, Automation, and Testing 會議論文**【Worst-Case IR-Drop Monitoring with 1GHz Sampling Rate】** 獲選為 **Best Paper Award**。
- ◆ 2014 年 IEEE Asian Test Symposium 會議論文**【S.-Y. Huang, H.-X. Li, Z.-F. Zeng, K.-H. Tsai, and W.-T. Cheng, "On-Line Transition-Time Monitoring for Die-to-Die Interconnects in 3D ICs", Proc. of Asian Test Symp. (ATS), pp. 162-167, (Nov. 2014)】** 獲選為 **Best Paper Award**。

6. 著作

期刊 Journal Papers

1. S.-Y. Huang and K.-T. Cheng, "ErrorTracer: A Fault-Simulation-Based Approach to Design Error Diagnosis", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, pp. 1341-1352, (Sept. 1999).
2. S.-Y. Huang, K.-C. Chen and K.-T. Cheng, "AutoFix: A Hybrid Tool for Automatic Logic Rectification", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, pp. 1375-1384, (Sept. 1999).
3. K.-T. Cheng, S.-Y. Huang, and W.-J. Dai, "Fault Emulation: A New Methodology for Fault Grading," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, pp. 1487-1495, (Oct. 1999).
4. S.-Y. Huang, K.-T. Cheng, K.-C. Chen, C.-Y. Huang, and F. Brewer, "AQUILA: An Equivalence Checking System for Large Sequential Designs," IEEE Trans. on Computers, pp. 443-464, (May 2000).
5. S.-Y. Huang, K.-T. Cheng, K.-C. Chen, "Verifying Sequential Equivalence Using ATPG techniques," ACM Trans. on Design Automation of Electronic Systems, pp. 244-275, (April 2001).
6. S.-Y. Huang, D.-M. Kwai, and C. Huang, "A High-Speed Architecture For At-Speed DRAM Testing," Journal of The Chinese Institute of Electrical Engineering, Vol. 8, No. 4, pp. 387-394, (Nov. 2001).

7. S.-Y. Huang, "Improving the Timing of Extended Finite State Machines Via Catalyst," *VLSI Design Journal*, Vol. 15, No. 3, pp. 629-636, (Nov. 2002).
8. S.-Y. Huang, "A Symbolic Inject-And-Evaluate Paradigm for Byzantine Fault Diagnosis", *Journal of Electronic Testing, Theory and Applications (JETTA)*, Vol. 19, No. 2, pp. 161-172, (April 2003).
9. H.-C. Kao, M.-F. Tsai, S.-Y. Huang, C.-W. Wu, W.-F. Chang, and S.-K. Lu, "Efficient Double Fault Diagnosis for CMOS Logic Circuits With A Specific Application To Generic Bridging Faults", *Journal of Information Science and Engineering (JISE)*, pp. 571-586, Vol. 19, No. 4, (July 2003).
10. S.-Y. Huang and C.-J. Liu, "A Low-Power Architecture For Extended Finite State Machines Using Input Gating," *IEICE Trans. on Fundamentals*, pp. 3109-3115, Vol. E87-A, No. 12, (Dec. 2004).
11. Y.-J. Juang, S.-F. Chen, S.-Y. Huang, Y.-C. King, "A Low-Cost Logarithmic CMOS Image Sensor Design By Nonlinear Analog-To-Digital Conversion", *IEEE Trans. on Consumer Electronics*, Vol. 51, No. 4, pp. 1212-1217, (Nov. 2005).
12. K.-H. Lai, S.-Y. Huang, and P.-C. Chiang, "A Sizing Methodology for the Charge Noise Reduction of a Comparator," *Int'l Journal of Electrical Engineering*, Vol. 13, No. 1, pp. 1-7, (Feb. 2006).
13. C.-H. Lai, Y.-C. King, and S.-Y. Huang, "A 1.2V 0.25um Clock Output Pixel Architecture With Dynamic Range and Self-Offset Cancellation," *IEEE Sensors Journal*, pp. 398-405, Vol. 6, No. 2, (April 2006).
14. Y.-C. Lin and S.-Y. Huang, "Accurate Whole-Chip Diagnostic Strategy for Scan Designs with Multiple Faults," *Journal of Electronic Testing: Theory and Applications (JETTA)*, Vol. 22, No. 2, pp. 151-159, (April 2006).
15. Y.-T. Lin and S.-Y. Huang, "Low-Power Adaptive FIR Filter Generator Using Bit-Oriented Structures," *IEE Proceedings Circuits, Devices, and Systems*, Vol. 153, No. 2, pp. 167-172, (April 2006).
16. H.-B. Wang, S.-Y. Huang, and J.-R. Huang, "A Modified Inject-and-Evaluate Paradigm for Diagnosing Gate-Delay Faults", *Int'l Journal of Electrical Engineering*, Vol. 13, No. 2, pp. 185-191, (May 2006).
17. C.-W. Tzeng and S.-Y. Huang, "Diagnosis by Image Recovery: Finding Mixed Multiple Timing Faults in a Scan Chain," *IEEE Trans. on Circuits and Systems II: Express Briefs (TCAS-II)*, Vol. 54, No. 8, pp. 690-694, (Aug. 2007).
18. C.-F. Chen, S.-Y. Huang, and Y.-C. King, "Built-In Self-Repair for Die-to-Die Misalignment for Multi-Die Space Sensors," *IEEE Sensors Journal*, Vol. 7, No. 9, pp. 1354-1355, (Sept. 2007).
19. C.-W. Tzeng, J.-J. Hsu, and S.-Y. Huang, "A Robust Paradigm for Diagnosing Hold-Time Faults in Scan Chains," *IET Proc. on Computers and Digital Techniques*, Vol. 1, No. 6, pp. 706-715, (Nov. 2007).
20. C.-W. Tzeng, J.-S. Yang, and S.-Y. Huang, "A Versatile Paradigm for Scan Chain Diagnosis of Complex Faults Using Signal Processing Techniques," *ACM Trans. on Design Automation of Electronic Systems (TODAES)*, Vol. 13, No. 1, pp. 9.1-9.27, (Jan. 2008).
21. C.-W. Tzeng and S.-Y. Huang, "UMC-Scan Test Methodology - Exploiting the Maximum Freedom of Multicasting", *IEEE Design and Test of Computers (D&T)*, Vol. 25, No. 2, pp. 132-140, (March-April, 2008).

22. S.-P. Cheng and S.-Y. Huang, "A Low-Power SRAM for Viterbi Decoder in Wireless Communication," *IEEE Trans. on Consumer Electronics*, Vol. 54, No. 2, pp. 290-295, (May 2008).
23. Y.-C. Lai and S.-Y. Huang, "X-Calibration: A Robust Technique for Combating Excessive Bitline Leakage Current in Nanometer SRAM Designs", *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 43, No. 9, pp. 1964-1971, (Sept. 2008).
24. Y.-C. Lai and S.-Y. Huang, "A Resilient and Power Efficient Automatic-Power-Down Sense Amplifier for SRAM Design", *IEEE Trans. on Circuits and Systems II: Express Briefs (TCAS-II)*, Vol. 55, No. 10, pp. 1031-1035, (Oct. 2008).
25. Y.-C. Lai and S.-Y. Huang, "Robust SRAM Design via BIST-Assisted Timing-Tracking (BATT)", *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 44, No. 2, pp. 642-649, (Feb. 2009).
26. C.-W. Tzeng, H.-C. Cheng, and S.-Y. Huang, "Layout-Based Defect-Driven Diagnosis for Intra-Cell Bridging Defects," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 28, No. 5, pp. 764-769, (May 2009).
27. Y.-C. Lai, S.-Y. Huang, and H.-J. Hsu, "Resilient Self-VDD-Tuning Scheme with Speed Margining for Low-Power SRAM", *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 44, No. 10, pp. 2817-2823, (Oct. 2009).
28. C.-W. Tzeng and S.-Y. Huang, "QC-Fill: Quick-and-Cool X-Filling for Multicasting-Based Scan Test," *IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 28, No. 11, pp. 1756-1766, (Nov. 2009).
29. H.-J. Hsu and S.-Y. Huang, "A Low-Jitter ADPLL via a Suppressive Digital Filter and an Interpolation-Based Locking Scheme," *IEEE Trans. on VLSI Systems (TVLSI)*, Vol. 17, No. 11, pp. 165-170, (Nov. 2009).
30. C.-W. Tzeng and S.-Y. Huang, "Split-Masking: An Output Masking Scheme for Effective Compound Defect Diagnosis in Scan Architecture with Test Compression," *IEEE Trans on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 29, No. 5, pp. 834-839, (May 2010).
31. C.-H. Lo and S.-Y. Huang, "P-P-N Based 10T SRAM Cell for Low-Leakage and Resilient Sub-Threshold Operation," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 46, No. 3, pp. 695-704, (March, 2011).
32. Bor-Woei Kuo, Hsun-Hao Chang, Yung-Chang Chen, and Shi-Yu Huang, "A Light-and-Fast SLAM Algorithm for Robots in Indoor Environments Using Line Segment Map," *Journal of Robotics, (WEB-LINKING) Volume 2011, Article ID 257852*, 12 pages, (2011).
33. S.-K. Lu, Y. Chen, S.-Y. Huang, and C.-W. Wu, "Speeding Up Emulation-Based Diagnosis Techniques for Logic Cores," *IEEE Design & Test of Computers (D&T)*, Vol. 28, No. 4, pp. 88-97, (July-Aug. 2011).
34. F.-C. Huang, S.-Y. Huang, J.-W. Ker, and Y.-C. Chen, "High-Performance SIFT Hardware Accelerator for Real-Time Image Feature Extraction", *IEEE Trans. on Circuits and System for Video Technology (TCAS-VT)*, Vol. 22, No. 3, pp. 340-351, (March 2012).
35. T.-Y. Li, S.-Y. Huang, H.-J. Hsu, C.-W. Tzeng, C.-T. Huang, J.-J. Liou, H.-P. Ma, P.-C. Huang, J.-C. Bor, C.-C. Tien, and M. Wang, and C.-W. Wu, "AC-Plus Scan Methodology for Small Delay Testing and Characterization," *IEEE Trans. on VLSI Systems (TVLSI)*, Vol. 21, No. 2, pp. 329-341, (Feb. 2013).

36. J.-W. You, S.-Y. Huang, Y.-H. Lin, M.-H. Tsai, D.-M. Kwai, Y.-F. Chou, and C.-W. Wu, "In-Situ Method for TSV Delay Testing and Characterization Using Input Sensitivity Analysis," *IEEE Trans. on VLSI Systems (TVLSI)*, Vol. 21, No. 3, pp. 443-453, (March 2013).
37. J.-W. Ke, S.-Y. Huang, C.-W. Tzeng, D.-M. Kwai, and Y.-F. Chou, "Die-to-Die Clock Synchronization for 3D IC using Dual Locking Mechanism," *IEEE Trans. on Circuits and Systems - Part I, (TCAS-I)*, Vol. 60, No. 4, pp. 908-917, (April 2013).
38. Y.-H. Lin, S.-Y. Huang, K.-H. Tsai, W.-T. Cheng, S. Sunter, Y.-F. Chou, and D.-M. Kwai, "Parametric Delay Test of Post-Bond TSVs in 3-D ICs via VOT Analysis", *IEEE Trans. on Computer-Aided Design of Electronic Circuits (TCAD)*, Vol. 32, No. 5, pp.-737-747, (May 2013).
39. S.-Y. Huang, Y.-H. Lin, Li-Ren Huang, K.-H. Tsai, and W.-T. Cheng, "Programmable Leakage Test and Binning for TSVs with Self-Timed Timing Control", to appear in *IEEE Trans. on Computer-Aided Design of Electronic Circuits (TCAD)*, Vol. 32, No. 8, pp. 1265-1273, (Aug. 2013).
40. L.-R. Huang, S.-Y. Huang, S. Sunter, K.-H. Tsai, and W.-T. Cheng "Oscillation-Based Pre-Bond TSV Test," *IEEE Trans. on Computer-Aided Design of Electronic Circuits (TCAD)*. Vol. 32, No. 9, pp. 1440-1444, (Sept. 2013).
41. R.-T. Ding, S.-Y. Huang, and C.-W. Tzeng, "Cell-Based Process Resilient Multi-Phase Clock Generation", *IEEE Trans. on VLSI Systems (TVLSI)*, Vol. 21, No. 12, (Dec. 2013).
42. P.-Y. Chao, C.-W. Tzeng, S.-Y. Huang, C.-C. Weng, and S.-C. Fang, "Process Resilient Low-Jitter All-Digital PLL via Smooth Code Jumping", *IEEE Trans. on VLSI Systems (TVLSI)*, Vol. 21, No. 12, (Dec. 2013).
43. L.-R. Huang, S.-Y. Huang, K.-H. (Hans) Tsai, and W.-T. Cheng, "Parametric Fault Testing and Performance Characterization of Post-Bond Interposer Wires in 2.5-D ICs", *IEEE Trans. on Computer-Aided Design of Electronic Circuits (TCAD)*, Vol. 33, No. 3, pp. 476-488, (March 2014).
44. C.-W. Tzeng, S.-Y. Huang, P.-Y. Chao, and R.-T. Ding, "Parameterized All-Digital PLL Architecture and Its Compiler to Support Easy Process Migration," *IEEE Trans. on VLSI Systems (TVLSI)*, Vol. 22, No. 3, pp. 621-630, (March 2014).
45. S.-Y. Huang, J.-Y. Lee, K.-H. (Hans) Tsai, and W.-T. Cheng, "Pulse-Vanishing Test for Interposers Wires in 2.5-D IC", *IEEE Trans. on Computer-Aided Design of Electronic Circuits(TCAD)*, Vol. 33, No. 8, pp. 1258-1268, (Aug. 2014).
46. S.-Y. Huang and Li-Ren Huang, "PLL-Assisted Timing Circuit for Accurate TSV Leakage Binning," *IEEE Design and Test of Computers (D&T)*, Vol. 31, No. 4, pp. 36-42, (2014).
47. C.-Y. Lin, C.-W. Huang, C.-B. Kuan, S.-Y. Huang, and J.-K. Lee, "The Design and Experiments of A SID-Based Power-Aware Simulator for Embedded Multi-Core Systems," *ACM Trans. on Design Automation of Electronic Systems (TODAES)*, Vol. 20, No. 2, Article 22, (Feb. 2015).
48. S.-Y. Huang, M.-T. Tsai, Z.-F. Zeng, K.-H. (Hans) Tsai, and W.-T. Cheng, "General Timing-Aware Built-In Self-Repair for Die-to-Die Interconnects," *IEEE Trans. on Computer-Aided Design of Electronic Circuits (TCAD)*, Vol. 34, No 11, pp. 1836-1846, (Nov. 2015).
49. S.-Y. Huang, M.-T. Tsai, H.-X. Li, Z.-F. Zeng, K.-H. (Hans) Tsai, and W.-T. Cheng,

"Non-Intrusive On-Line Transition-Time Binning and Timing Failure Threat Detection for Die-to-Die Interconnects," *IEEE Trans. on Computer-Aided Design of Electronic Circuits (TCAD)*, Vol. 34, No 12, pp. 2039-2048, (Dec. 2015).

50. S.-Y. Huang, M.-T. Tsai, K.-H. (Hans) Tsai, and W.-T. Cheng, "Delay Characterization and Testing of Arbitrary Multiple-Pin Interconnects," *IEEE Design and Test of Computers (D&T)*, Vol. 33, No. 2, pp. 9-16, (April 2016).
51. S.-T. Tseng, Y.-H. Kao, C.-C. Peng, J.-Y. Liu, S.-C. Chu, G.-F. Hong, C.-H. Hsieh, K.-T. Hsu, W.-T. Liu, Y.-H. Huang, S.-Y. Huang, and T.-S. Chu, "A 65nm CMOS Low Power Impulse Radar System for Human Respiratory Feature Extraction and Diagnosis on Respiratory Diseases", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 64, No. 4, pp. 1029-1041, (April 2016).
52. S.-Y. Huang, C.-C. Cheng, M.-T. Tsai, K.-C. Huang, K.-H. Tsai, and W.-T. Cheng, "Versatile Transition-Time Monitoring for Interconnects via Distributed TDC", *IEEE Design and Test (D&T)*, Vol. 33, No. 5, (2016).

會議論文集 Conference Papers

1. K.-T. Cheng, S.-Y. Huang, and W.-J. Dai, "Fault Emulation: A Novel Approach to Fault Grading", Proc. Int'l Conf. on Computer-Aided Design, pp. 681-686, (Nov. 1995). abstract
2. S.-Y. Huang, K.-T. Cheng, and K.-C. Chen, "On Verifying the Correctness of Retimed Circuits", Proc. of Great-Lake Symposium on VLSI, pp. 277-281, (March 1996). abstract
3. S.-Y. Huang, K.-C. Chen, K.-T. Cheng, and T.-C. Lee, "Vector Generation for Accurate Power Simulation", Proc. of IEEE/ACM Design Automation Conf., pp. 161-164, (June. 1996). abstract
4. S.-Y. Huang, K.-C. Chen, and K.-T. Cheng, "Error Correction Based on Verification Techniques", Proc. of IEEE/ACM Design Automation Conf., pp. 258-261, (June. 1996). abstract
5. S.-Y. Huang, K.-T. Cheng, K.-C. Chen, and T.-C. Lee, "A Novel Methodology for Transistor-level Power Simulation", Int'l Symposium on Lower Power Electronic Design, pp. 67-72, (Aug. 1996). abstract
6. S.-Y. Huang, K.-T. Cheng and K.-C. Chen, "An ATPG-based Framework for Verifying Sequential Equivalence", Proc. Int'l Test Conf., pp. 865-874, (Oct. 1996). abstract
7. S.-Y. Huang, K.-T. Cheng and K.-C. Chen, "AQUILA: An Equivalence Verifier for Large Sequential Circuits", Proc. of Asia and South Pacific Design Automation Conf., pp. 455-460, (Jan. 1997). abstract
8. S.-Y. Huang, K.-C. Chen, and K.-T. Cheng, "Incremental Logic Rectification", Proc. of VLSI Test Symposium, pp. 134-139, (April 1997). abstract
9. S.-Y. Huang, K.-T. Cheng, K.-C. Chen, and D. I. Cheng, "ErrorTracer: A Fault Simulation Based Approach to Design Error Diagnosis", Proc. of Int'l Test Conf., pp. 974-981, (Nov. 1997).
10. Y.-M. Jiang, S.-Y. Huang, K.-T. Cheng, D. C. Wang, and C.-Y. Ho, "A Hybrid Power Model for RTL Power Estimation", Proc. of Asia and South Pacific Design Automation Conf., pp. 551-556, (Feb. 1998).
11. S.-Y. Huang, K.-T. Cheng, and K.-C. Chen, "General Design Error Diagnosis for

- Sequential Circuits", Proc. of IEEE/ACM Design Automatic Conf., pp. 632-637, (June 1998).
12. Yi-Min Jiang, S.-Y. Huang, K.-T. Cheng, and D.-C. Wang, C.-Y. Ho, "A Hybrid Power Model For RTL Power Estimation," Proc. of Asia and South Pacific Design Automation Conf., pp. 551-556, (Feb. 1998).
 13. S.-Y. Huang and D.-M. Kwai, "A High-Speed Built-In Self-Test Design for DRAMs", Proc. of Int'l Symposium on VLSI-TSA (Technology, Systems, and Applications), pp. 50-53, (June 1999).
 14. S.-Y. Huang, "On Speeding Up Finite State Machines Using Catalyst Circuitry", Proc. of Asia and South Pacific Design Automation Conf. (ASP-DAC), 583-588, (Jan. 2001).
 15. S.-Y. Huang, "Towards The Logic Defect Diagnosis For Partial-Scan Designs", Proc. of Asia and South Pacific Design Automation Conf. (ASP-DAC), pp. 313-318, (Jan. 2001).
 16. S.-Y. Huang, "On Improving the Accuracy of Multiple Defect Diagnosis", Proc. of VLSI Test Symposium (VTS), pp. 34-39, (April 2001).
 17. C.-J. Liu and S.-Y. Huang, "Low-Power Synthesis For Extended Finite State Machines," Proc. of 12th VLSI/CAD Symposium, Taiwan, (Aug. 2001).
 18. C.-C. Lu and S.-Y. Huang, "Improving the Accuracy of Mixed-Level Power Estimation for CMOS Logic Circuits With Power Management," Proc. of 12th VLSI/CAD Symposium, Taiwan, (Aug. 2001).
 19. H.-C. Kao, M.-F. Tsai, S.-Y. Huang, C.-W. Wu, W.-F. Chang, and S.-K. Lu, "Efficient Double Fault Diagnosis For CMOS Logic Circuits," Proc. of 12th VLSI/CAD Symposium, Taiwan, (Aug. 2001).
 20. C.-W. Wang, R.-S. Tzeng, C.-F. Wu, C.-T. Huang, C.-W. Wu, S.-Y. Huang, S.-H. Lin, and H.-P. Wang, "A Built-In Self-Test and Self-Diagnosis Scheme for Heterogeneous SRAM Clusters," Proc. of Asian Test Symposium, pp. 103-108, (Nov. 2001).
 21. S.-Y. Huang, "Speeding Up The Byzantine Fault Diagnosis Using Symbolic Simulation," Proc. of VLSI Test Symposium, pp. 193-198, (April 2002).
 22. Y.-C. Tsai, S.-Y. Huang, C.-P. Su, C.-T. Huang, and C.-W. Wu, "Fine-Grain Mixed-Level Power Estimation Based On Disparity Path Analysis," Proc. of 12th VLSI/CAD Symposium, Taiwan, (Aug. 2002).
 23. H.-B. Wang, S.-Y. Huang, and J.-R. Huang, "Gate-Delay Fault Diagnosis Using The Inject-And-Evaluate Paradigm For Full-Scan Designs", Proc. of Int'l Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'02), (Nov. 2002).
 24. S.-Y. Huang, "Diagnosis Of Byzantine Open-Segment Faults," Proc. of Asian Test Symposium, pp. 248-253, (Nov. 2002).
 25. M.-L. Lee, T.-T. Hwang, and S.-Y. Huang, "Decomposition of Extended Finite State Machine For Low-Power Design," Proc. of Design Automation and Test in Europe, pp. 1152-1153, (2003).
 26. S.-K. Lu, J.-L. Chen, C.-W. Wu, K.-F. Chang, and S.-Y. Huang, "Combinational Circuit Fault Diagnosis Using Logic Emulation," Proc. of Int'l Symp. on Circuits and Systems, Vol. 5, pp. 549-552, May 2003.
 27. S.-F. Chen, Y.-J. Juang, S.-Y. Huang, and Y.-C. King, "Logarithmic CMOS Image Sensor Through Multi-Resolution Analog-To-Digital Conversion," Proc. of Int'l Symposium on VLSI Technology, Systems, and Applications, pp. 227-230, (April

- 2003).
28. Y.-T. Lin and S.-Y. Huang, "Efficient Bit-Oriented Implementation of FIR Filters Using A New Compressor," Proc. of Int'l SOC Conf., pp.269-271, (Sept. 2003).
 29. B.-R. Lin, S.-Y. Huang, C.-H. Lai, and Y.-C. King, "A High Dynamic Range CMOS Image Sensor Design Based On Two-Frame Composition," Proc. of Int'l SOC Conf., pp. 389-392, (Sept. 2003).
 30. Y.-C. Lin and S.-Y. Huang, "Chip-Level Diagnostic Strategy For Full-Scan Designs With Multiple Faults," Proc. of Asian Test Symposium, pp. 38-44, (Nov. 2003).
 31. S.-Y. Huang, "A Fading Algorithm For Sequential Fault Diagnosis," to appear in Proc. of Int'l Symposium on Defect and Fault Tolerance on VLSI Systems, pp. 139-147, (Nov. 2004).
 32. K.-H. Lai, S.-Y. Huang, P.-C. Chiang, "A Sizing Methodology For A Low-Noise Comparator," Proc. of Asia-Pacific Conf. on Circuits and Systems, pp. 253-256, (Dec. 2004).
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