ESD-Protected K-Band Low-Noise Amplifiers Using RF Junction Varactors in 65-nm CMOS

Ming-Hsien Tsai, *Member, IEEE*, Shawn S. H. Hsu, *Member, IEEE*, Fu-Lung Hsueh, and Chewn-Pu Jou

***Abstract*—This paper presents two K-band low-noise amplifiers (LNAs) in 65-nm CMOS using the proposed RF junction varactors as the ESD protection devices. The junction varactors are customized for the RF ESD applications with accurate equivalent circuit models. The experimental results demonstrate excellent second breakdown currents (It_2) and high ratios of the ESD level to parasitic capacitances ($V_{\rm ESD}/C_{\rm ESD}$). Using the dual-diode topology, the first LNA demonstrates an over 2-kV Human-Body-Model (HBM) ESD protection level with a noise figure (NF) of 2.8 dB and a peak gain of 14.3 dB at around 24 GHz under a power consumption of only 7 mW. By incorporating an RF junction varactor as the extra gate-source capacitance at the input stage as a part of the ESD network, the second LNA presents an enhanced failure current level up to 2.6 A (corresponding to an HBM ESD level of 3.9 kV), and a Charge-Device-Model (CDM) ESD level up to 10.7 A, characterized by the Very Fast Transmission Line Pulse (VFTLP) tests. The second LNA shows a NF of 3.2 dB and a power gain of 13.7 dB, also under 7 mW.**

***Index Terms*—Charge-device-model (CDM), electrostatic discharge (ESD), junction varactor, low-noise amplifier (LNA), MOS, radio frequency (RF), transmission line pulse (TLP), very fast transmission line pulse (VFTLP).**

I. Introduction

With rapid scaling of the feature size in CMOS technology, the improved device performance allows high speed circuit operation under low power consumption. Also, the demand for increased system functionality makes the system-on-chip (SOC) design using advanced CMOS technology an inevitable trend. However, the reduced gate oxide thickness and lowered breakdown voltage poses a tremendous design challenge for the on-chip electrostatic discharge (ESD) protection, especially for the SOC design with a large chip size for RF applications [1]–[3].

The parasitic effects introduced by the ESD devices are critical to the RF front-end circuits, which could seriously degrade the input reflection coefficient, noise, and gain if not properly designed. The impact of ESD protection devices on circuit characteristics becomes more obvious as the operating frequency increases. One straightforward approach is to minimize the parasitic capacitances (the "low-C" approach), which makes the ESD devices transparent to the RF core circuits [4], [5]. However, a tradeoff in general exists between the parasitics and ESD protection robustness, and this approach becomes less effective as the frequency increases up to the tens of GHz range. Since the parasitics introduced from the ESD devices are mostly capacitive, the idea of using inductive elements to cancel the effect of the ESD devices by LC resonance was also reported [6]–[8]. This approach also results in virtually transparent ESD blocks and allows a plug-and-play ESD design for RF circuits. Nevertheless, the additional inductive elements, implemented by either transmission lines or spiral inductors, will increase the chip area and also degrade the noise figure due to the resistive parasitics.

The co-design concept of ESD/matching networks has been proposed for RF applications [4], [5]. As a part of the matching network, the impacts of the ESD parasitic effects on the core circuits could be significantly reduced. For achieving an overall good RF performance in the co-design procedure, the ESD devices should be taken into considerations at the early design stage. Therefore, it is essential that the ESD devices have accurate RF models available and also with known ESD protection levels. Different devices have been proposed for ESD protection purposes, such as the grounded-gate nMOS (GGNMOS) [1]–[3], [9], silicon-controlled rectifier (SCR) devices [1]–[3], [10], and diodes [1]–[3], [11]. However, these devices are not originally developed for RF circuits, which need to be refined for high frequency applications [12]–[15]. Also, accurate RF models of these devices are in general not available for the co-design procedure. Differing from the commonly used ESD devices in previous studies, we propose utilizing the RF junction varactors, originally developed for RF circuit applications, for the ESD protection design in this study.

In this paper, the customized RF junction varactors are co-designed with the K-band low-noise amplifiers (LNAs) for ESD protection in 65-nm CMOS technology. The K-band (18–26.5 GHz) has recently attracted significant interests to both industry and academia for the applications of short-range and high data-rate wireless communications and anticollision radars [16]–[24]. With the customized layout, accurate scalable RF models, and characterized ESD levels, the RF junction varactors are carefully included as a part of the matching network to achieve an excellent noise figure and high ESD protection level simultaneously. With an identical LNA core circuit, two ESD designs are proposed and realized in 65 nm CMOS. The first design uses the dual-diode topology with both diodes implemented by the RF junction varactors, demonstrating an over 2-kV Human-Body-Model (HBM) ESD protection level. The LNA has a noise figure of 2.8 dB and a peak gain of 14.3

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dB at around 24 GHz under a power consumption of only 7 mW. In the second design, the metal-oxide-metal (MOM) capacitor at the input stage of the first LNA for achieving power-constrained simultaneous noise and input matching (PCSNIM) [25] is replaced by an RF junction varactor. The varactor turns on during the ESD zapping to provide additional localized Charge-Device-Model (CDM) ESD protection, which is of critical importance to the SOC chips with a relatively large chip size [26]. By co-optimizing the ESD level and RF characteristics, the second LNA demonstrates a 2.6-A Transmission Line Pulse (TLP) (corresponding to a 3.9-kV HBM) and a 10.7-A Very Fast Transmission Line Pulse (VFTLP) (for CDM ESD protection level) ESD current level. Also, the LNA presents a peak power gain and NF of 13.7 dB and 3.2 dB respectively under 7 mW.

This paper is organized as follows. Section II discusses design, modeling, and characterization of the customized RF junction varactors for ESD protection. In Section III, the design details of the two proposed ESD-protected LNAs at K-band are presented. The experimental results including both RF and ESD measurements are shown in Section IV, and Section V concludes this work.

II. RF Junction Varactors for ESD Protection

Conventionally, the RF junction varactors are employed as voltage-dependent tunable capacitors [27] in voltage-controlled oscillators (VCO) or tunable matching networks for high power amplifiers [28]. In these cases, the varactors are in general operated under reverse bias conditions. In this study, we propose using the RF junction varactors for ESD protection devices. Under the reverse bias mode, the RF junction varactors are used as a RF capacitor for the matching network. In the forward bias mode, the varactors function as a diode with a small on-resistance to conduct current, providing excellent ESD protection. However, using the RF junction varactor as the ESD protection requires special design considerations, different from those of typical RF circuits.

Fig. 1(a) shows the layout view of a multi-finger RF junction varactor for ESD protection. The two most important parameters, on-resistance and failure current of the ESD protection devices, are largely determined by the device layout and metal routing. For ESD protection, the junction varactors must be able to sustain a large current during ESD zapping. It is essential to have sufficient vias and a large metal width in both anode and cathode to prevent the electron-migration issue. In the customized junction varactor design, we utilize the maximum allowed contact and via density ($\sim$10 contacts/μm in each finger). Also, all the metal layers (six layers in this technology with a total thickness of $\sim$5 μm) are employed (connected by vias) along the ESD current path to reduce the on-resistance.

Fig. 1(b) illustrates the cross section view of the finger-type junction varactor with the structure of parallel connected p-n junction in N-Well, bounded by shallow-trench-isolation (STI). Fig. 1(c) shows the corresponding equivalent circuit model. The $D_{\mathrm{P+/NW}}$ models the ESD bypass diode, mainly composed of the multi-finger p-n junctions and the fringing capacitances between the fingers. The components $R_1, R_2, L_1,$

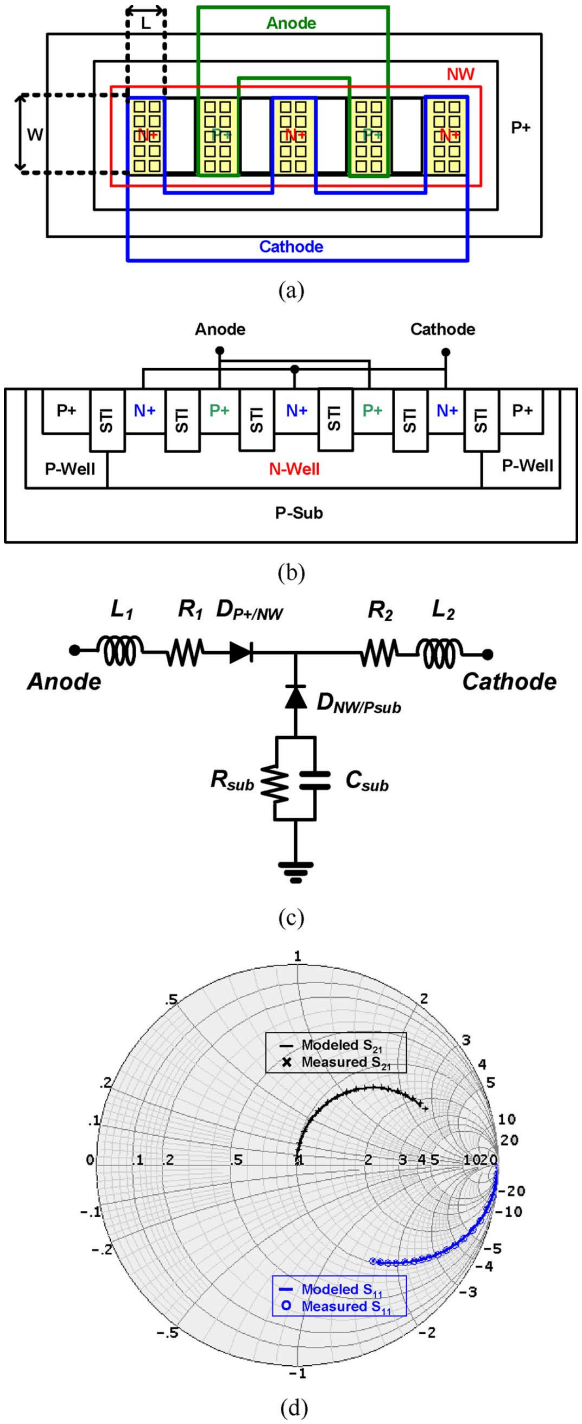

Fig. 1. Proposed RF junction varactor for ESD protection in multi-finger topology. (a) Layout view. (b) Cross section view. (c) Equivalent circuit model. (d) Measured and model S-parameters ($W = 1\ \mu$m, $L = 0.15\ \mu$m, $N = 50$).

and L_2 describe the parasitic effects of the anode and cathode; and $D_{\mathrm{NW/Psub}}, R_{\mathrm{sub}}$, and C_{sub} model the parasitics from the substrate. Compared with the single-finger layout approach for ESD design [29], [30], the multi-finger layout can reduce the parasitic resistances and inductances (R_1, R_2, L_1 and L_2) owing to the parallel connected finger and reduced length of each finger for a certain total finger width. Also, the bypass current capability is enhanced since the overall junction periphery increases under a fixed device area. Fig. 1(d) compares

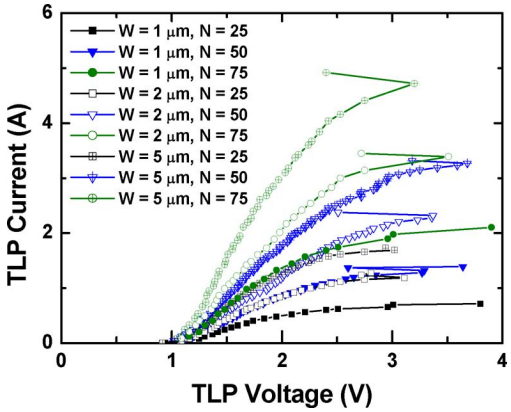

Fig. 2. Measured TLP I-V curves with different device geometries.

the measured and modeled S-parameters of an RF junction varactor ($W = 1$ μm, $L = 0.15$ μm, and $N = 50$) from 0.2 GHz to 30 GHz, which shows an excellent agreement between the measured and modeled results. It should be mentioned that the fringing effect in the multi-finger topology increases the overall parasitic capacitances compared with that in the single-finger layout. However, the parasitic capacitances become not that critical when using the co-design approach, which can be absorbed in the matching network.

A testing technique called Transmission Line Pulse (TLP) is often used to characterize the ESD robustness of the devices [31], [32]. The setup generates a pulse with a 10-ns rise time and a 100-ns width to simulate the Human-Body-Model (HBM) ESD condition. The secondary breakdown current It_2 is determined by a sudden increase of the leakage current. The relation between the TLP second breakdown current (It_2) and the HBM ESD level $(V_{\rm ESD})$ can be approximated as $V_{\rm ESD}$ (V) $\sim It_2$ (A) $\cdot R_{\rm HBM}(\Omega)$, where $R_{\rm HBM}$ (=1.5 kΩ) is the approximate equivalent resistance of the human body. The bypass ESD current capability of the junction varactors is investigated by varying the device finger width ($W = 1, 2$, and 5 μm) and finger number ($N = 25, 50$, and 75). The minimum device length of 0.15 μm, limited by the design rule, is selected for maximizing the total periphery. Fig. 2 shows the measured TLP I-V curves, and Table I summaries the corresponding ESD characteristics. For a fixed W, It_2 increases with the finger number (N) due to the increased junction periphery and reduced on-resistance; similarly, for a fixed N, It_2 increases with W. The associated parasitic capacitance $C_{\rm ESD}$ also increases with the device size. The experimental results demonstrate excellent second breakdown currents and high ratios of the ESD level to parasitic capacitances $(V_{\rm ESD}/C_{\rm ESD})$ of these customized RF junction varactors. Based on these experimental results, proper device sizes could be selected to achieve the desired ESD level with good input matching.

III. Circuit Topology

The K-band LNAs with two ESD designs were realized in 65 nm CMOS. The first LNA has a primary ESD protection by the dual-diode configuration. With an identical RF core circuit and the same primary ESD network, the second LNA also includes a secondary ESD protection using the junction varactor at the common-source input stage mainly for the CDM ESD event. In addition, an LNA without any ESD protection was implemented for reference.

TABLE I
ESD Characteristics With Different Device Sizes

	W	L	N	It_2	V_{ESD}	C_{ESD}	V_{ESD}/C_{ESD}
Unit	μm	μm	--	A	kV	fF	V / fF
W1N25	1	0.15	25	0.7	~ 1.0	13.6	73.5
W1N50	1	0.15	50	1.4	~ 2.1	25.9	81.1
W1N75	1	0.15	75	2.1	~ 3.1	38.4	80.7
W2N25	2	0.15	25	1.4	~ 2.1	25.6	82.0
W2N50	2	0.15	50	2.4	~ 3.6	51.3	70.2
W2N75	2	0.15	75	3.4	~ 5.1	75.4	67.6
W5N25	5	0.15	25	1.8	~ 2.7	61.6	43.8
W5N50	5	0.15	50	3.3	~ 4.9	123.3	40.1
W5N75	5	0.15	75	4.7	~ 7.0	186.6	37.5

* ESD levels are estimated from the TLP tests ($V_{HBM} \sim It_2 \cdot R_{HBM}$).

A. LNA With Primary ESD Protection Network

Fig. 3 shows the LNA using the proposed RF junction varactors in a dual-diode configuration as the primary ESD protection in conjunction with a power clamp to complete the ESD network. The cascode topology is employed as the core circuit with the source inductive degeneration, which has the advantages of increased gain, reduced Miller effects, and improved input/output isolation. The input matching network includes the RF junction varactors (also for ESD devices) $JV_{\rm T}$ and $JV_{\rm B}$, gate inductor $L_{\rm G}$, source inductor $L_{\rm S}$, and a MOM capacitor $C_{\rm GS}$. The gate-source capacitor $C_{\rm GS}$ is critical for achieving power-constrained simultaneous noise and input matching (PCSNIM), which helps obtain a 50-ohm real part of the input impedance while allowing a small transistor size and hence reduced power consumption. The inductor $L_{\rm D}$ works as the inductive peaking and the output matching to 50 ohm. The gate of M_2 is connected to $V_{\rm DD}$ through a large resistor $R_{\rm B}$ of $\sim$1.8 KΩ for bias. The bypass capacitor $C_{\rm B}$ of $\sim$2.4 pF provides a good ac ground for the common-gate stage. In addition, the gate-driven power clamp consists of a RC-timer circuit (resistor R and MOS capacitor $M_{\rm C}$) and an inverter ($M_{\rm P}$ and $M_{\rm N}$) to trigger the large nMOS $(M_{\rm ESD})$. Fig. 3 also indicates four different ESD current paths, corresponding to different ESD testing combinations (PD, PS, ND, and NS modes). The power clamp provides a low-impedance path from $V_{\rm DD}$ to ground, which completes the ESD paths for the PS and ND modes.

The "co-design" approach is employed for the ESD/matching circuit design. Under normal RF operation, the ESD devices (the RF junction varactors under reverse bias in this case) can be simply viewed as capacitors $C_{\rm ESD}$ and combined with the LC matching network of the LNA. Since the ESD protection level is in general proportional to $C_{\rm ESD}$ (see Table I), the circuit RF characteristics could be seriously degraded if a high ESD protection level is required using the conventional "plug and play" approach. In contrast, $C_{\rm ESD}$ is absorbed as a part of the matching network in the "co-design" approach and the tradeoff

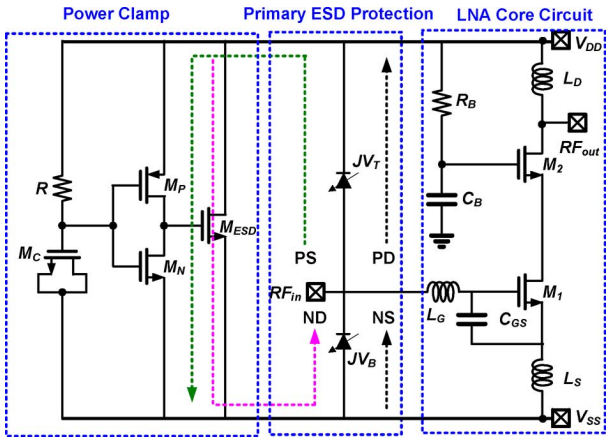

Fig. 3. Circuit schematic of the proposed LNA with the primary ESD protection network, consisting of the junction varactors ($JV_{\rm T}$ and $JV_{\rm B}$) and a power clamp.

between the RF performance and ESD level is relaxed. However, this approach requires accurate RF models of the ESD devices and more dedicated knowledge in both RF and ESD protection design.

Using the ESD and matching network co-design approach, the sizes of M_1 ($W = 36\ \mu$m) and M_2 ($W = 48\ \mu$m), and the value of g_m are determined first with the considerations of power dissipation, gain, and noise characteristics. The ESD blocks (JV_T and JV_B are both with $W = 1\ \mu$m, $L = 0.15\ \mu$m, and $N = 50$) are then designed based on the estimated protection levels and parasitic capacitances, as listed in Table I. The shunt parasitic capacitances introduced by the ESD blocks are co-designed with $L_{\rm G}$ of 0.7 nH, $L_{\rm S}$ of 0.16 nH, and $C_{\rm GS}$ of 34 fF to achieve simultaneous noise and power matching.

B. LNA With Primary and Secondary ESD Protection Networks

The charge-device-model (CDM) ESD protection has received increasing attention recently due to the trend of SOC with high integration levels and more functionality. The SOC chips are often fabricated in advanced CMOS devices with a large chip size, which could accumulate considerable amount of charges in the substrate. The CDM describes the self-discharge event of the accumulated charges in the body of ICs through a suddenly grounded pin. As the chip size increases such as in the SOC cases, the large amount of substrate charges could result in a high ESD discharge peak current during the CDM event, causing the damage of the gate oxide even before the primary ESD protection turns on. In practice, a current level up to ~10 A could be reached in a very short time period of ~1 ns [31]. Fig. 4 illustrates the most critical ESD current path from the substrate to the input pad during a CDM event. When the event occurs, the accumulated charges in the substrate need to find a discharge path with the lowest impedance. As shown in the figure, the CDM ESD current is most likely to flow through the gate oxide of M_1, which provides a low impedance path under the high frequency CDM pulse and has a short distance to the substrate. As a result, a high voltage stress is across the gate oxide which could be damaged before the primary ESD protection turns on [32], [33].

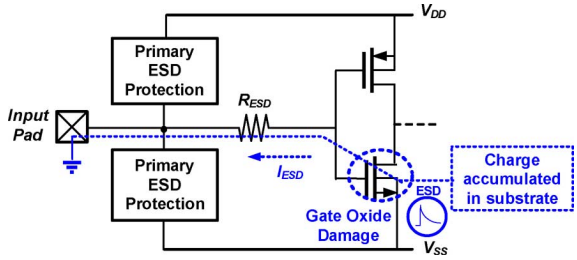

Fig. 4. Illustration of a general CDM ESD event and the most critical discharge path from the substrate to the input pad. The gate oxide could be damaged before the primary ESD protection turns on.

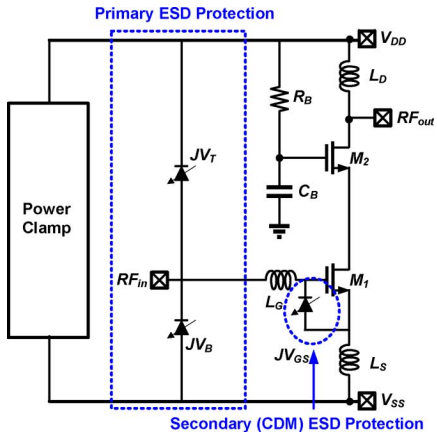

Fig. 5. Circuit schematic of the proposed LNA with the primary and secondary (CDM) ESD protection networks, consisting of the junction varactors ($JV_{\rm T}$, $JV_{\rm B}$, and $JV_{\rm GS}$) and a power clamp.

Fig. 5 shows the proposed second LNA using the RF junction varactors for the primary ESD protection, noise/matching optimization under low power, and also the secondary (CDM) ESD protection simultaneously. The MOM capacitor in the first design is replaced by an RF junction varactor. The $JV_{\rm GS}$ is not only implemented as the extra gate-source capacitance (junction varactor reverse biased at normal operation) for achieving PCSNIM, but also utilized as the secondary ESD protection (junction varactor forward biased during ESD zapping) to provide a localized ESD current path with a short distance and low impedance for the CDM protection of M_1.

Fig. 6(a) shows the flow chart of the co-design procedure, which indicates the detailed design steps of RF and ESD performance co-optimization for the proposed LNA with additional secondary ESD protection. First, the transistor size and bias could be determined by investigating the noise characteristics as a function of finger width and bias. Owing to the excellent scalability of MOS transistors, the gate bias $V_{\rm G}$ and current density $J_{\rm CH}$ for best noise performance are often with similar values in a wide variety of transistor sizes [24], which are about 0.6–0.7 V and 0.1–0.2 mA/μm in this case. Based on the selected $V_{\rm G}$ and $J_{\rm CH}$, the transistor sizes are then determined according to the $P_{\rm DC}$ and gain, which are in general a tradeoff. The selected sizes of M_1 and M_2 are $W = 36\ \mu$m and 48 μm, respectively. Second, considering the ESD protection capability, as shown in Table I, the sizes of the junction varactors ($JV_{\rm T}$, $JV_{\rm B}$, and $JV_{\rm GS}$) are determined. For simplicity, all three junction varactors are chosen with the same size of $W = 1\ \mu$m, $L = 0.15\ \mu$m, and $N = 50$. Finally, the gate inductor $L_{\rm G}$ and source inductor

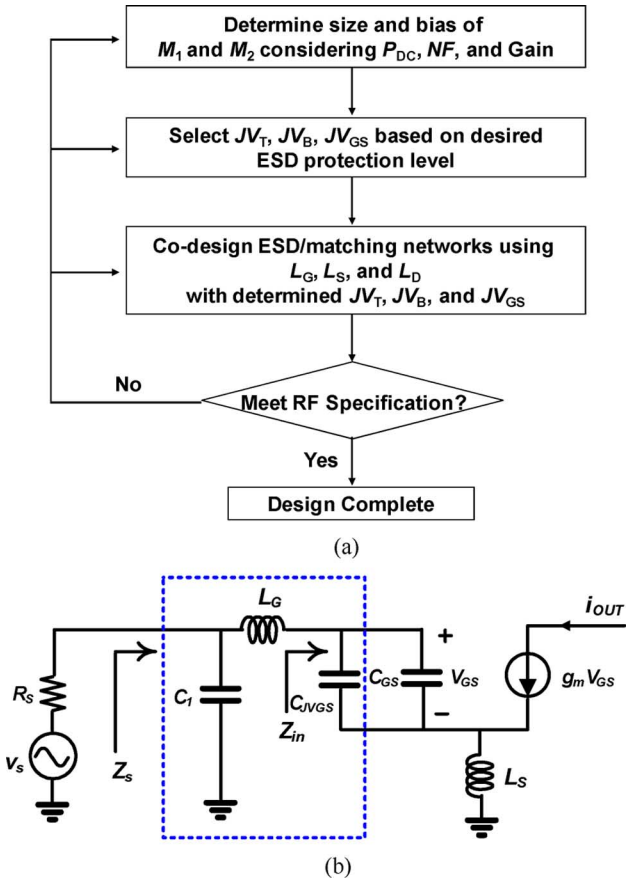

Fig. 6. (a) Co-design flow chart of ESD protection and matching network using RF junction varactors. (b) Equivalent circuit model indicates the ESD devices ($JV_{\rm T}$, $JV_{\rm B}$, $JV_{\rm GS}$) merged into the input matching network.

$L_{\rm S}$ are optimized for achieving a 50-ohm input at the operation frequency.

Fig. 6(b) shows the equivalent circuit model of the input stage with the ESD devices ($JV_{\rm T}$, $JV_{\rm B}$, and $JV_{\rm GS}$) merged into the input matching network. The input impedance can be represented by the following equations:

$$Z_{\rm in} = \frac{g_m L_S}{C_{\rm GST}} + j\left[\omega L_S - \frac{1}{\omega C_{\rm GST}}\right] \quad (1)$$

$$Z_S = \frac{1}{j\omega C_1} // (j\omega L_G + Z_{\rm in}) \quad (2)$$

where $C_{\rm GST} = C_{\rm JVGS} // C_{\rm GS}$ and $C_1 = C_{\rm JVT} // C_{\rm JVB}$. Note that $L_{\rm S}$ is determined by the equations similar with that in [24], making the real part of $Z_{\rm in}$ 50 ohm. Also, $L_{\rm G}$ is designed together with C_1 to eliminate the imaginary part of $Z_{\rm S}$.

IV. Results and Discussion

The LNAs were fabricated using a 65-nm CMOS low-power process. This process features a gate oxide thickness of ~2 nm and a minimum channel length of 60 nm for the core devices. The reference LNA and two ESD-protected LNAs are denoted as *LNA-A*, *LNA-B* (with primary ESD protection) and *LNA-C* (with both primary and secondary ESD protection), respectively. Fig. 7(a) and (b) show the chip micrographs of *LNA-B* and *LNA-C* with the same chip size of 0.22 $\rm mm^2$.

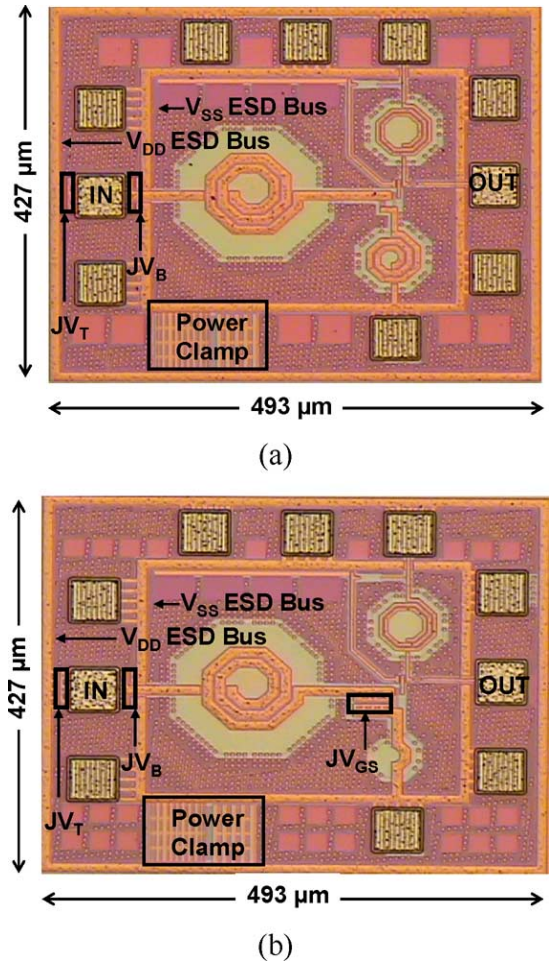

Fig. 7. Chip micrographs of the LNAs with (a) primary ESD protection (*LNA-B*), and (b) the primary and secondary (CDM) ESD protection (*LNA-C*), respectively.

A. RF Measurement Results

The RF characteristics of circuits were measured on-wafer using Cascade G-S-G microwave probes with a 100-μm pitch. The S-parameters and noise measurements were performed by the Agilent PNA network analyzer and Agilent 8975A noise figure analyzer, respectively. All three LNAs operate from a 1.2 V supply and draw a current of 5.8 mA with a dc power consumption of 7 mW. The measured $|S_{21}|$ of the LNAs are shown in Fig. 8. The peak gains are 14.3 dB at 24 GHz and 13.7 dB at 23 GHz for *LNA-B* and *LNA-C* respectively, only degraded by 0.9 and 1.5 dB compared with that of *LNA-A* (15.2 dB at 24 GHz). Fig. 9 shows the measured $|S_{11}|$ of the LNAs. The minimum input reflection coefficients are -16 and -11.5 dB at 24 GHz for *LNA-A* and *LNA-B* respectively, and -12 dB at 23 GHz for *LNA-C*. Fig. 10 shows the measured NF from 20 to 26 GHz. The minimum values are 2.8 dB and 3.2 dB for *LNA-B* and *LNA-C* respectively at 23.5 GHz, only degraded by 0.1 dB and 0.5 dB compared with that of *LNA-A* of 2.7 dB at the same frequency. In addition, the linearity of the LNA was characterized by the two-tone intermodulation distortion test. The measured *IIP3* are -5.4, -4.9, and -4.6 dBm at 24 GHz for *LNA-A*, *LNA-B*, and *LNA-C* respectively.

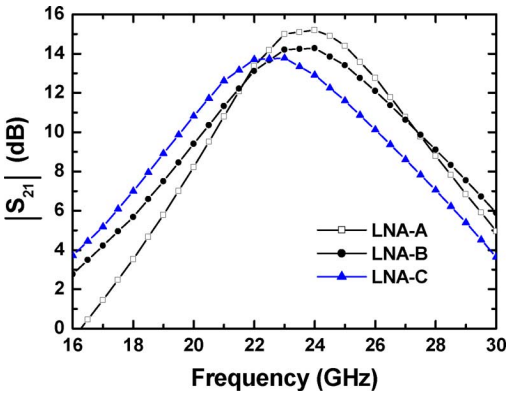

Fig. 8. Measured $|S_{21}|$ of the LNAs with/without ESD protection.

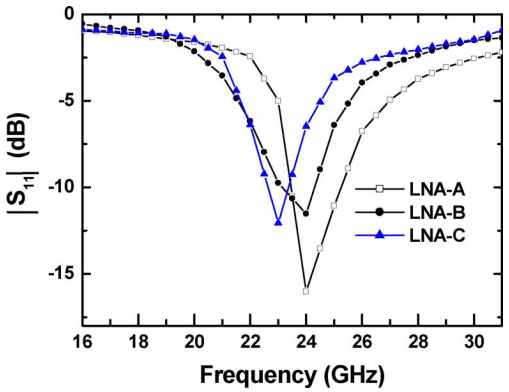

Fig. 9. Measured $|S_{11}|$ of the LNAs with/without ESD protection.

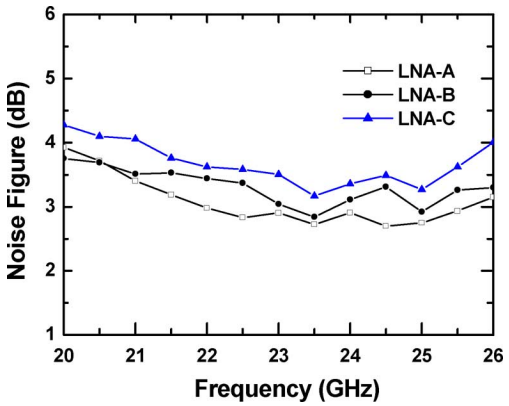

Fig. 10. Measured NFs of the LNAs with/without ESD protection.

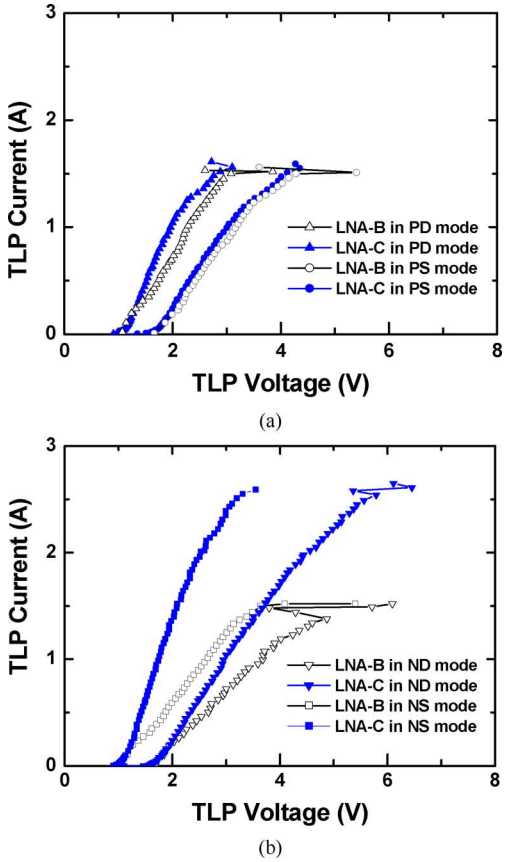

Fig. 11. Measured TLP I-V curves of the ESD-protected LNAs. (a) PD and PS modes. (b) ND and NS modes.

TABLE II
ESD PERFORMANCE COMPARISON OF DIFFERENT TESTING MODES

ESD- LNA	PS		PD		NS		ND	
	It_2 (A)	HBM (kV)	It_2 (A)	HBM (kV)	It_2 (A)	HBM (kV)	It_2 (A)	HBM (kV)
LNA-B	1.4	~ 2.1	1.4	~ 2.1	1.4	~ 2.1	1.4	~ 2.1
LNA-C	1.4	~ 2.1	1.4	~ 2.1	2.6	~ 3.9	2.6	~ 3.9

* HBM levels are estimated based on the TLP measurements.

B. ESD Testing Results

A Barth Model 4002 TLP test system, which generates a pulse with a rise time of 10 ns along with a pulsewidth of 100 ns, was used for the on-wafer TLP characterization. Fig. 11(a) and (b) show the TLP test results of *LNA-B* and *LNA-C* with different pin combinations. For both *LNA-B* and *LNA-C*, the I-V curves of the PD mode are similar as well as those of the PS mode, as shown in Fig. 11(a). In the PD mode, the ESD bypass current enters from the RF input pad, flows through $JV_{\rm T}$ to $V_{\rm DD}$; in the PS mode, the ESD current path also enters from the RF input pad, flows through $JV_{\rm T}$ to $V_{\rm DD}$, and then reaches $V_{\rm SS}$ via the power clamp. Since both paths do not touch $JV_{\rm GS}$, the TLP results of the two designs are almost identical as expected. A sudden increase of the leakage current suggests that a second breakdown current It_2 up to 1.4 A in the PD mode, mainly determined by $JV_{\rm T}$, can be achieved corresponding to an over 2-kV ESD level. In the PS mode, the TLP I-V curves show a similar on-resistance (see the slope of the curves) with the PD mode, but with an increased turn-on voltage due to the power clamp. Also, the achieved It_2 is similar with that in the PD mode. Fig. 11(b) shows the measured TLP I-V curves of *LNA-B* and *LNA-C* in the ND (from $V_{\rm DD}$ to RF pad) and NS (from $V_{\rm SS}$ to RF pad) modes. Compared with *LNA-B*, *LNA-C* shows a smaller on-resistance in both NS and ND modes, indicating an extra ESD path provided by $JV_{\rm GS}$. Moreover, compared to the PD (PS) mode with a single ESD path in both LNAs, the ND (NS) mode with multiple ESD paths in *LNA-C* can enhance the TLP failure current from 1.4 to 2.6 A, corresponding to the increase of the ESD level from 2.1 to 3.9 kV.

A HANWA HED-T5000 TLP test system was used for VFTLP characterization to investigate the CDM ESD protection capability. Compared with the typical TLP test, the

TABLE III
PERFORMANCE COMPARISON OF THE PROPOSED K-BAND LNAS WITH PRIOR ARTS

Reference	This Work			[16]	[17]	[18]	[19]	[20]	[21]	[22]	[23]
Tech. (nm)	65 CMOS			90 CMOS	130 CMOS	180 CMOS	180 CMOS	180 CMOS	180 CMOS	180 CMOS	350 SiGe
Freq. (GHz)	24			24	24	24	24	22	23.7	22	24
	LNA-A	LNA-B	LNA-C								
Power (mW)	7.0	7.0	7.0	10.6	18	8	14	24	54	7.2	41
NF (dB)	2.7	2.8	3.2	3.2	5.0	3.3	3.9	6.0	5.6	4.3	3.1
S_{21} (dB)	15.2	14.3	13.7	7.5	14.0	12.8	13.1	15.0	12.86	10.1	12.0
S_{11} (dB)	-16	-11.5	-12	-16	-7.0	-7.5	-15	-22	-11	-12	-5.4
IIP3 (dBm)	-5.4	-4.9	-4.6	--	-1.7	--	--	--	2.04	-1.0	-5.0
TLP(A) / HBM (kV)	--	1.4 / 2.1	2.6 / 3.9	--	-- / 2.5	--	--	--	--	--	-- / 1.5
VFTLP(A)	--	5.8	10.7	--	--	--	--	--	--	--	
FOM	--	13.3	20.6	--	5.2	--	--	--	--	--	1.1

*HBM ESD levels are estimated from the TLP measurements ($V_{HBM} \sim It_2 \cdot R_{HBM}$).

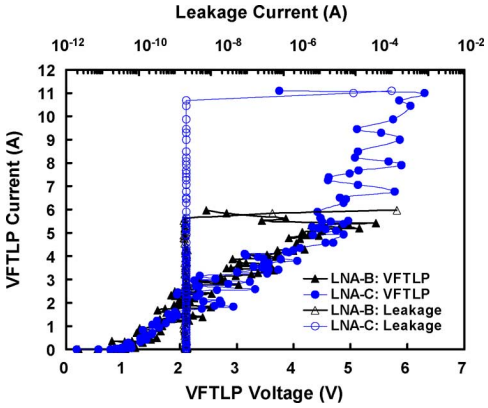

Fig. 12. Measured VFTLP I-V characteristics and the corresponding leakage current (the VFTLP failure current is determined by the significant increase of monitored leakage current).

pulsewidth of VFTLP is reduced from 100 ns to 1 ns and the rise time is shortened from 10 ns to 0.2 ns, which meet the CDM pulse specification given in the JEDEC standard [34]. Fig. 12 illustrates the measured VFTLP I-V characteristics and leakage currents of both *LNA-B* and *LNA-C*, in which 5.8 A (*LNA-B*) and 10.7 A (*LNA-C*) of the VFTLP failure currents can be achieved. The enhanced current level can be attributed to the additional localized protection provided by $JV_{\rm GS}$. Table II summarizes the ESD testing results of different testing modes. Note that with the secondary ESD protection $(JV_{\rm GS})$, the protection levels of both NS and ND modes are enhanced significantly. Table III compares this work with other published ESD-protected RF LNAs. Compared with the prior arts using less advanced technology, the relatively lower linearity is mainly due to the low power and low supply voltage design in this work by 65 nm CMOS. With low noise, high gain, low power consumption, and high ESD protection level, the proposed ESD-protected LNA achieves an excellent figure-of-merit (modified from [8])

$$\mathrm{FOM} = \frac{\mathrm{Gain[abs]} \times \mathrm{IIP3[abs]} \times f_C\mathrm{[GHz]} \times \mathrm{ESD[kV]}}{(\mathrm{NF}-1)\mathrm{[abs]} \times P_{\rm DC}\mathrm{[mW]}}. \quad (3)$$

V. CONCLUSION

In this paper, the RF junction varactors were proposed for ESD protection devices, which were characterized and modeled in details for both RF and ESD. The K-band LNAs were realized in 65-nm CMOS technology with two different ESD designs using the RF junction varactor. The first LNA using the dual-diode topology as the primary ESD network presented an over 2-kV HBM ESD level with a NF of 2.8 dB and a peak gain of 14.3 dB under 7 mW. With similar RF core circuit and primary ESD protection, the second LNA replaced the gate-source MOM capacitor by an RF junction varactor at the input stage for the secondary ESD (localized CDM) protection. The failure current level was enhanced from 1.4 up to 2.6 A, corresponding to a 3.9-kV HBM ESD protection and the CDM ESD level was increased from 5.8 A to 10.7 A. The second LNA only showed slight degradation on NF and gain of 0.4 dB and 0.6 dB, respectively under the same power consumption.

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