A 40-Gb/s Modulator Driver Using Cascade Swing Compensation in 90-nm CMOS

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Abstract—This letter presents a high-speed optical modulator driver with a large output swing in 90-nm CMOS technology. A new topology of cascade swing compensation (CSC) output stage is proposed for protecting the transistors from breakdown using dynamic gate biasing without extra RC networks. To enhance the bandwidth and gain, the active feedback with T-coil peaking and the negative capacitance with series peaking are employed in the preamplifier and main driver, respectively. Under a power consumption of 767 mW, the measured results demonstrate an operating data rate up to 40 Gb/s with a maximum differential output swing of 4.5 Vppd obtained at 32 Gb/s.

Index Terms—Cascade amplifier, CMOS, differential amplifier, modulator driver, silicon photonics.

I. INTRODUCTION

The exponential growth of data communications can be expected owing to the increasing demand for broadband services, such as multimedia applications and cloud computing. The high-speed fiber network plays an essential role to fulfill these demands. Fig. 1 shows a typical transmitter for optical communications using Mach–Zehnder modulator (MZM), where the modulator driver could be a bottleneck to limit the overall bandwidth for electrical-to-optical (E/O) signal conversion. The modulator driver should meet some important criteria such as a sufficient bandwidth, a high voltage swing, and tolerance of the voltage swing across the output stage to prevent transistors exceeding the breakdown voltage [1]–[5].

These challenges mostly have been overcome with the III–V or BiCMOS technology [4], [5]. The silicon modulators have attracted significant attention recently, which possess the benefits of low cost and low power consumption by operating at a relatively lower voltage. The reduced operating voltage makes it feasible to realize the modulator driver in CMOS technology, which is also preferred for the silicon photonics platform. However, the transistor breakdown voltage is still one of the main issues [6]–[8]. In this study, a 40-Gb/s differential modulator driver is demonstrated using the proposed new cascade swing compensation (CSC) topology in the output stage for transistor breakdown protection.

Manuscript received 2 March 2022; revised 28 March 2022; accepted 13 April 2022. Date of publication 29 April 2022; date of current version 6 September 2022. This work was supported in part by Ministry of Science and Technology (MOST) under Contract MOST 109-2221-E-007-013-MY3 and in part by Industrial Technology Research Institute (ITRI). (Corresponding author: Shawn S. H. Hsu.) The authors are with the Department of Electrical Engineering, National Tsing Hua University, Hsinchu 300, Taiwan (e-mail: shshu@ee.nthu.edu.tw).

II. CIRCUIT DESIGN AND ANALYSIS

The breakdown voltage of transistors ultimately limits the output voltage swing of a CMOS modulator driver. The conventional cascode topology is relatively simple and can increase the bandwidth effectively. With the stacked transistors, the output voltage swing could be distributed on the two devices to protect the transistors from breakdown. However, the top common-gate (CG) stage with a fixed gate bias could still suffer the gate–drain breakdown under a large output swing \(V_{\text{out}}\). An I/O device could be used for the CG stage to enhance the breakdown voltage, but the operating speed will be degraded. A widely used technique is to add the RC network at the gate of the CG transistor, which allows the gate voltage to dynamically swing with \(V_{\text{out}}\) to reduce the gate–drain voltage difference [9]. However, using the RC network still suffers from tradeoff between bandwidth and swing protection capability. In this letter, we propose a new topology of using the cascaded differential cascode configuration for the CG transistor protection without additional RC network. Compared with our previous work [1] using the DA topology, the proposed CSC technique can achieve gate dynamic bias by a cross-coupled differential topology directly, which is different from the widely used RC network bias and has not been reported. Fig. 2 shows the circuit schematic of the proposed differential modulator driver, including a preamplifier and the CSC output stage.

A. Preamplifier

The preamplifier employs second-order active feedback [10] with T-coil peaking inductors. As shown in Fig. 2, the cascaded differential common-source (CS) stages \((M_1 - M_4)\) are used as the gain stage, and the active feedback \((M_5 - M_6)\) senses the output voltage from the T-coil center nodes and returns a proportional signal to the gates of \(M_3\) and \(M_4\). The active feedback acts as negative feedback, which allows increasing the gain-bandwidth product (GBP) beyond technology \(f_T\). Note that the linearity of this topology could be limited by the \(M_5 - M_6\) stage if the output swing (T-coil center nodes) exceeds the linear operating range of the feedback stage.

The combination of active feedback \((M_5\) and \(M_6\)\) and T-coil \((L_1 - L_4)\) creates zeros and complex conjugate poles to obtain gain peaking for bandwidth extension. With well-designed parameters, bandwidth extension ration could reach
Fig. 2. Circuit topology, design parameters, and bias conditions of the proposed modulator driver with CSC topology.

Fig. 3. T-coil. (a) Layout. (b) Inductance and quality factor.

2.2 × [10]. Fig. 3(a) and (b) shows the layout of the T-coil and the electromagnetic (EM) simulated inductance and $Q$. The pattern ground shield is used to enhance the quality factor and alleviate substrate coupling. Note that the parasitic coupling capacitance in the layout is used directly as the bridge capacitor for the T-coil [11]. Also, the capacitive loading from $M_7$ to $M_8$ has been considered for the T-coil design optimization.

B. CSC Output Stage

Fig. 4 shows the proposed CSC output topology and also illustrates how the dynamic gate voltage swing can be achieved, where the reactive elements including the series peaking inductors ($L_5 - L_8$) and the negative capacitance ($C_1 - C_2$) have been removed to simplify the analysis. The topology can be viewed as two cascaded cascode stages with the signals in two different paths. As the differential signals amplified by the CS stage $M_7/M_8$ after entering nodes IN+/IN−, the output signals appear at nodes X/X′. If focusing on the half circuit, one path is connected to the gate of $M_11$ and the other is connected to the source of $M_9$. The signal propagating through the first path is then amplified again by $M_{13}$ in the cascode stage, which eventually appears at the output node OUT−. The signal in the other path coming from node $X′$ enters the source of $M_9$ and reaches node $Y$ for a dynamic gate voltage swing. As shown in Fig. 4, this gate voltage is with the same phase for the output swing at OUT−. As a result, the drain–gate voltage difference could be effectively reduced for $M_{13}$ to protect the transistor from breakdown and obtain a large output swing.

According to the desired output voltage swing and load resistance, the bias current and required swing at each node can be estimated. The dc bias (drain and gate) of the transistors can then be designed to ensure transistor operation in the saturation region. Using the minimum gate length for high-speed operation, the width of each transistor can be designed with the determined dc points and bias current. Based on the final design including all the reactive elements, Fig. 5(a) shows the simulated single-ended waveform with a Pseudo Random Binary Sequence (PRBS) input signal, which indicates that the voltage difference between node OUT− and node Y can be well controlled at around 1.3 V to avoid gate–drain breakdown of $M_{13}$. Note that the maximum supply voltage suggested by the foundry for the adopted 90-nm RF CMOS is $\sim 1.5$ V [1]. The signal at node $Y$ can also induce a voltage swing at node Z via $M_{13}$. Combining with the amplified in-phase signal from node X, the voltage swing at node Z becomes relatively large compared to a conventional cascade configuration with a fixed gate voltage. Fig. 5(b) shows the voltages at both node $Z$ and node X, which indicates that the maximum difference is
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FIG. 6. (a) Chip micrograph. (b) Comparison of measured and simulated differential S-parameters.

FIG. 7. Measured eye diagrams at (a) 20, (b) 25, (c) 32, and (d) 40 Gb/s of differential NRZ output.

FIG. 8. Simulated (a) transient gain (b) THD (at 1 GHz).

III. RESULTS AND DISCUSSION

Fig. 6(a) shows the chip micrograph of the proposed circuit in 90-nm CMOS. The differential S-parameters were measured on-wafer by the N5247A network analyzer. Fig. 6(b) shows a comparison of the measured and simulated differential S-parameters, which shows a very good agreement. Under a power consumption of 767 mW, the driver achieves a high gain of 19- and a 3-dB bandwidth of 28.5 GHz. Note that there is a considerable amount of power consumed on the 50-Ω termination in this fully integrated modulator driver, which can be reduced substantially if an external bias network is used. The large-signal measurements were performed using the MP1800A analyzer and the DSA-Z 334A real-time oscilloscope, as shown in Fig. 7. With an input signal of 500 mVppd, the measured differential eye diagrams can achieve 4.5 Vppd at 32 Gb/s, limited by the data rate of the signal source. We also performed measurement using the Anritsu G0374A for obtaining 40 Gb/s eye diagram. The achieved 4 Vppd is under a 0.4 V input swing, also limited by the equipment.

Fig. 8(a) and (b) shows the simulated transient gain and total harmonic distortion (THD) under different input voltage levels, respectively. The transient gain is obtained with a differential sinusoidal input signal, which indicates a consistent trend with $S_{11}$ even under 500 mV input. The THD simulation is performed at 1 GHz. As expected, the nonlinearity increases gradually with the input signal level. The THD is about 6.6% when $V_{in}$ is 500 mV, with a corresponding output swing $V_{ppd}$ of $\sim 4.7$ V.

IV. CONCLUSION

The proposed modulator driver in 90-nm CMOS demonstrated large bandwidth, high gain, and excellent driving capability. With the new CSC topology, the transistors in the cascode output stage can be protected from breakdown under a large voltage swing. The operating frequency is up to 40 Gb/s and the maximum output differential swing can reach 4.5 Vppd.
REFERENCES


