Constructions of Fault Tolerant Linear Compressors and Linear Decompressors

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Abstract— **The constructions of optical buffers is one of the most critically sought after optical technologies in all-optical packet-switched networks, and constructing optical buffers directly via optical Switches and fiber Delay Lines (SDL) has received a lot of attention recently in the literature. A practical and challenging issue of the constructions of optical buffers that has not been addressed before is on the fault tolerant capability of such constructions. In this paper, we focus on the constructions of fault tolerant linear compressors and linear decompressors. The basic network element for our constructions is scaled optical memory cell, which is constructed by a 2×2 optical crossbar switch and a fiber delay line. We give a multistage construction of a *self-routing* linear compressor by a concatenation of scaled optical memory cells. We also show that if the delays, say $d_1, d_2, \ldots, d_M$, of the fibers in the scaled optical memory cells satisfy a certain condition (specifically, the condition in (A2) given in Section I), then our multistage construction can be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M-F} d_i$ even after up to F of the M scaled optical memory cells fail to function properly, where $0 \leq F \leq M - 1$. Furthermore, we prove that our multistage construction with the fiber delays $d_1, d_2, \ldots, d_M$ given by the generalized Fibonacci series of order F is the best among all constructions of a linear compressor that can tolerate up to F faulty scaled optical memory cells by using M scaled optical memory cells. Similarly results are also obtained for the constructions of fault tolerant linear decompressors.**

I. INTRODUCTION

One of the key problems of optical packet switching is the lack of optical buffers as optical packets cannot be easily stopped, stored, and forwarded. To build high speed packet switches that scale with the speed of fiber optics, one needs to resolve conflicts among packets competing for the same resources. Traditionally, such conflicts are resolved by first converting optical packets into electronic packets, storing them in electronic buffers, and then converting electronic packets back into optical packets. Therefore, such an approach incurs tremendous overheads in both the O-E conversion and the E-O conversion, and hence could not fully exploit the transmission speed advantage of photons over electrons. As such, the design of optical buffers has become one of the most critically sought after optical technologies in all-optical packet-switched networks.

The only known way to "store" optical packets without converting them into other media is to direct them via a set of optical switches through a set of fiber delay lines so that the optical packets come out at the right place and at the right time. With recent advances in optical technologies, the constructions of compact and tunable optical buffers by using the so-called "slow light" technique [1]–[5] have been made feasible. As a result, the construction of an optical buffer may not be as bulky as one might expect, and the synchronization issue that is usually of practical concern may not be a critical design obstacle. As such, constructing optical buffers directly via optical Switches and fiber Delay Lines (SDL) has been recognized as one of the promising technologies for the design of optical buffers, and has received a lot of attention recently in the literature (see e.g., [6]–[23] and the references therein).

Early SDL constructions for optical buffers, including the shared-memory optical packet switch in [6] and CORD (contention resolution by delay lines) in [7][8], focused more on the feasibility of such an approach. On the other hand, recent advances in SDL constructions have shown that there exist systematic methods for constructing various types of optical buffers, including First-In-First-Out (FIFO) multiplexers in [9]–[11] and [17]–[19], buffered packet switches in [11][12], FIFO queues in [20], priority queues in [21][22], and linear compressors, non-overtaking delay lines, and flexible delay lines in [23].

A practical and challenging issue of the constructions of optical buffers that has not been addressed before is on the fault tolerant capability of such constructions. The reliability issue in the design of any network element is of great concern to a system designer and deals with the situation that some of the components of a network element may not function properly. Without taking the reliability aspect into consideration during the design process, a network element consisting of hundreds or thousands of components will be in a total breakdown even when only a single component fails to function properly. As such, the constructions of fault tolerant network elements are extremely important and challenging from a practical point of view.

In this paper, we focus on the constructions of fault tolerant linear compressors and linear decompressors. As in most works in the SDL literature, we assume that packets are of the same size. Furthermore, time is slotted and synchronized so that every packet can be transmitted within a time slot. By so doing, packets can be "stored" in a fiber delay line with the propagation delay being an integer multiple of a time slot.

We will use scaled optical memory cells as basic network elements for the constructions of fault tolerant linear compressors and linear decompressors. A scaled optical memory cell that will be described in detail in Section II is constructed by a 2×2 optical crossbar switch and a fiber delay line. In Section II, we briefly review the construction of a linear compressor in [23], and then we give a straightforward construction of a fault tolerant linear compressor. In Section III, we first show a two-stage construction of a linear compressor. Such a two-stage construction is recursively expanded to give a multistage construction of a *self-routing* linear compressor by a concatenation of scaled optical memory cells. We also derive the following condition on the delays, say $d_1, d_2, \ldots, d_M$, of the fibers in the scaled optical memory cells so that our multistage construction can be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M} d_i$:

(A1) $d_1 = 1$ and $d_{k+1} \leq \sum_{i=1}^{k} d_i + 1$ for all $k = 1, 2, \ldots, M - 1$.

For $0 \leq F \leq M - 1$, we then use (A1) to show a more general result that our multistage construction can be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M-F} d_i$ even after up to F of the M scaled optical memory cells are broken if the following condition is satisfied:

(A2) $d_i = 1$ for all $i = 1, 2, \ldots, F + 1$, and $d_{k+F-1} \leq d_{k+F} \leq \sum_{i=1}^{k-1} d_i + 1$ for all $k = 2, 3, \ldots, M - F$.

Note that (A2) is more general than (A1) as (A2) reduces to (A1) when $F = 0$. Furthermore, we show an optimality result that our multistage construction with the fiber delays $d_1, d_2, \ldots, d_M$ given by the generalized Fibonacci series of order F is the best among all constructions of a linear compressor that can tolerate up to F faulty scaled optical memory cells by using M scaled optical memory cells. Similarly results for the constructions of fault tolerant linear decompressors are given in Section IV. Finally, conclusions are made in Section V.

II. A STRAIGHTFORWARD CONSTRUCTION OF A FAULT TOLERANT LINEAR COMPRESSOR

In our previous papers [20][23], we used optical memory cells as basic network elements for the constructions of various types of optical queues. An optical memory cell (see Figure 1) is constructed by a 2×2 optical crossbar switch and a fiber delay line with one time slot (unit) of delay. To write a packet to the memory cell, set the 2×2 crossbar switch to the "cross" state so that the packet at the input link can be directed to the fiber delay line with one time slot of delay. Once the write operation is completed, the crossbar switch is then set to the "bar" state so that the packet directed into the fiber delay line

keeps circulating through the fiber delay line. To read out the information from the memory cell, set the crossbar switch to the "cross" state so that the packet in the fiber delay line can be directed to the output link.
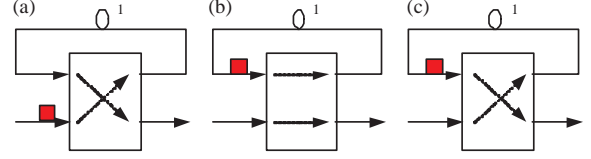

Fig. 1. An optical memory cell: (a) writing information (b) circulating information (c) reading information.

A scaled SDL element is said to be with scaling factor m if the delay of every delay line is m times of that in the original (unscaled) SDL element. One of the most important properties of SDL elements is the time interleaving property for scaled SDL elements in [17]: a scaled SDL element with scaling factor m can be operated as time interleaving of m SDL elements. For example, in Figure 2, we show a scaled optical memory cell with scaling factor 2 as the length of the delay line in Figure 2 is twice of that in the original optical memory cell in Figure 1. To operate a scaled optical memory cell with scaling factor 2 as time interleaving of two (unscaled) optical memory cells, one first partitions time into even and odd numbered time slots. For the even numbered time slots, one can set the connection patterns of the 2×2 optical crossbar switch in the scaled SDL element according to the read/write operation for one memory cell. Similarly, for the odd numbered time slots, one can set the connection patterns of the 2×2 optical crossbar switch in the scaled SDL element according to the read/write operation for the other memory cell.
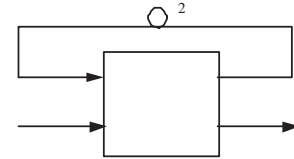

Fig. 2. An optical memory cell with scaling factor 2.

Now we review the definition and the construction of a linear compressor in [23].

Definition 1 (Linear compressors [23]) *Suppose that the departure time of a packet is known upon its arrival. Let $\tau^a(n)$ and $\tau^d(n)$ be the arrival time and the departure time, respectively, of the nth packet. A network element with a single input link and a single output link is called a* linear compressor *with the range of delay $[d_1, d_2]$ if it realizes the set of mappings that satisfy*

$$\tau^a(n) + d_1 \leq \tau^d(n) \leq \tau^a(n) + d_2 \text{ for all } n, \quad (1)$$

and the following monotone and consecutive condition: $\tau^d(n) = \tau^d(n-1) + 1$ whenever $\tau^a(n) \leq \tau^d(n-1)$. In

particular, if $d_1 = 0$, then it is called a linear compressor with maximum delay d_2.

As pointed out in [23], the name, linear compressor, originates from its counterpart for space switches (see e.g., [24][25]). The condition $\tau^a(n) \leq \tau^d(n-1)$ means that the nth packet arrives before the $(n-1)^{th}$ packet departs. If one defines a busy period of a linear compressor as the period of time that there are packets in the linear compressor, then the monotone and consecutive condition implies that the departures in a busy period are monotone and consecutive. Note that the packet that initiates a busy period can have an arbitrary delay (as long as its delay is not greater than the maximum delay).

It was shown in [23] that a linear compressor with maximum delay $2^M - 1$ can be constructed by a concatenation of M scaled optical memory cells in Figure 3. Moreover, such a construction is a self-routing linear compressor. Specifically, let $x = \tau^d(n) - \tau^a(n)$ be the delay of the nth packet, and let $b_M b_{M-1} \ldots b_2 b_1$ be the binary representation of x (from the most significant bit to the least significant bit), i.e., $x = \sum_{i=1}^{M} b_i 2^{i-1}$. Index the M scaled optical memory cells from left to right. Then the nth packet is routed to the fiber delay line with delay 2^{i-1} at the ith scaled optical memory cell only if $b_i = 1$.
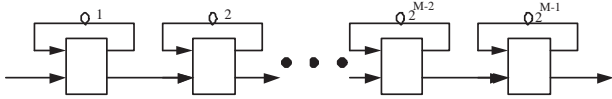

Fig. 3. A self-routing linear compressor with maximum delay $2^M - 1$.

The problem with the self-routing linear compressor in Figure 3 is its fault tolerant capability. If one of the scaled optical memory cells does not function properly, then the construction in Figure 3 no longer works. To increase the reliability of the construction via a concatenation of scaled optical memory cells, we assume that each optical memory cell has a bypass circuit. The bypass circuit sets up a direct connection between its input link and its output link once a fault within an optical memory cell is detected. Such an optical memory cell will be called a *fault/bypass* optical memory cell in this paper. Even with fault/bypass optical memory cells, the construction in Figure 3 still does not work when one of the fault/bypass optical memory cells detects a fault.

To construct a linear compressor that can tolerate a failure of a fault/bypass optical memory cell, one may simply use two scaled optical memory cells for each stage of the construction (see Figure 4). As such, one can build a linear compressor with maximum delay $2^M - 1$ that can tolerate one faulty optical memory cell by a concatenation of $2M$ scaled optical memory cells. In a similar way, one can build a linear compressor with maximum delay $2^M - 1$ that can tolerate up to F faulty optical memory cells by a concatenation of $(F+1)M$ scaled optical memory cells.

In order to compare various constructions, we introduce the efficiency ρ for a construction of a linear compressor. Suppose
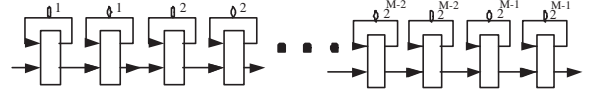

Fig. 4. A direct construction of a fault tolerant linear compressor with maximum delay $2^M - 1$ that can tolerate one faulty optical memory cell.

that a linear compressor with maximum delay d is constructed by M scaled optical memory cells. Then its efficiency ρ is defined to be the ratio of $\log_2(d+1)$ to the number of scaled optical memory cells M used in the construction, i.e.,

$$\rho = \frac{\log_2(d+1)}{M}. \qquad (2)$$

For instance, the efficiency for the construction in Figure 3 is 1 and the efficiency for the naive construction that uses $F+1$ scaled optical memory cells at each stage is only $1/(F+1)$. However, the former construction cannot tolerate any failure of scaled optical memory cells, and the latter with a much lower construction efficiency can tolerate up to F failures of scaled optical memory cells. In Section III, we will show an optimal construction of a linear compressor that can tolerate up to F faulty scaled optical memory cells and has efficiency greater than $1/(F+1)$.

III. An Optimal Construction of a Fault Tolerant Linear Compressor

A. A Two-stage Construction of a Linear Compressor

In Figure 5, we consider a two-stage construction of a network element. The first stage is a linear compressor with maximum delay d_1, and the second stage is a linear compressor with maximum delay B and scaling factor d_2. We will show that if $d_2 \leq d_1 + 1$, then such a construction can be operated as a linear compressor with maximum delay $Bd_2 + d_1$ under the following operation rule:

(R1) If $\tau^d(n) - \tau^a(n) \leq Bd_2 - 1$, then we set $\tau^c(n) = \tau^d(n) - d_2 \lfloor \frac{\tau^d(n) - \tau^a(n)}{d_2} \rfloor$. Otherwise, we set $\tau^c(n) = \tau^d(n) - Bd_2$.
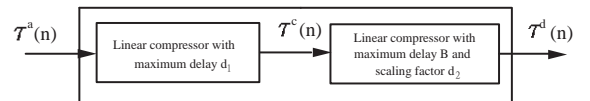

Fig. 5. A two-stage construction of a linear compressor.

Theorem 2 *Suppose that the network element in Figure 5 is started from an empty system. If $d_2 \leq d_1 + 1$, then under (R1) the two-stage construction is a linear compressor with maximum delay $Bd_2 + d_1$.*

Proof. According to Definition 1 for a linear compressor, we need to show that the network element in Figure 5 can realize

all the mappings (or sample paths) that satisfy

$$\tau^a(n) \le \tau^d(n) \le \tau^a(n) + Bd_2 + d_1, \tag{3}$$
$$\tau^d(n) = \tau^d(n-1) + 1,$$
$$\text{whenever } \tau^a(n) \le \tau^d(n-1). \tag{4}$$

In other words, if (3) and (4) hold for all n, then under the assignment rule in (R1)

$$\tau^a(n) \le \tau^c(n) \le \tau^a(n) + d_1, \tag{5}$$
$$\tau^c(n) = \tau^c(n-1) + 1,$$
$$\text{whenever } \tau^a(n) \le \tau^c(n-1). \tag{6}$$

$$\tau^c(n) \le \tau^d(n) \le \tau^c(n) + Bd_2, \tag{7}$$
$$(\tau^d(n) - \tau^c(n)) \bmod d_2 = 0, \tag{8}$$
$$\tau^d(n) = \tau^d(n^*) + d_2,$$
$$\text{whenever } \tau^a(n) \le \tau^d(n^*), \tag{9}$$

where n^* is the last packet (in the busy period containing the nth packet) that departs before the nth packet from the same time interleaved linear compressor at the second stage. In the following, we divide the proof into three parts.

(i) First, we show that (5), (7), and (8) hold for all n. We consider the following two cases:

Case 1. $0 \le \tau^d(n) - \tau^a(n) \le Bd_2 - 1$:

In this case, we see from (R1) that

$$\tau^c(n) = \tau^d(n) - d_2 \left\lfloor \frac{\tau^d(n) - \tau^a(n)}{d_2} \right\rfloor, \tag{10}$$

which implies that

$$\tau^c(n) = \tau^a(n) + ((\tau^d(n) - \tau^a(n)) \bmod d_2). \tag{11}$$

It follows from (11), $\tau^d(n) \ge \tau^a(n)$ in (3), and the assumption $d_2 \le d_1 + 1$ that

$$\tau^a(n) \le \tau^c(n) \le \tau^a(n) + d_2 - 1 \le \tau^a(n) + d_1.$$

As $0 \le \lfloor \frac{\tau^d(n) - \tau^a(n)}{d_2} \rfloor \le B - 1 \le B$ in this case, we have from (10) that

$$\tau^c(n) \le \tau^d(n) \le \tau^c(n) + Bd_2.$$

Clearly, $(\tau^d(n) - \tau^c(n)) \bmod d_2 = 0$.

Case 2. $Bd_2 \le \tau^d(n) - \tau^a(n) \le Bd_2 + d_1$:

In this case, we have from (R1) that $\tau^c(n) = \tau^d(n) - Bd_2$, and it follows that $\tau^a(n) \le \tau^c(n) \le \tau^a(n) + d_1$. Clearly, $\tau^d(n) = \tau^c(n) + Bd_2$ and $((\tau^d(n) - \tau^c(n)) \bmod d_2) = 0$.

(ii) To see (6), suppose that $\tau^a(n) \le \tau^c(n-1)$. Then we also have $\tau^a(n) \le \tau^d(n-1)$ as $\tau^c(n-1) \le \tau^d(n-1)$ in (7). It follows from (4) that

$$\tau^d(n) = \tau^d(n-1) + 1. \tag{12}$$

Now we consider the following two cases:

Case 1. $(k-1)d_2 \le \tau^d(n-1) - \tau^a(n-1) \le kd_2 - 1$, $k = 1, 2, \ldots, B$:

In this case, we see from (R1) that

$$\tau^c(n-1) = \tau^d(n-1) - d_2 \left\lfloor \frac{\tau^d(n-1) - \tau^a(n-1)}{d_2} \right\rfloor$$
$$= \tau^d(n-1) - (k-1)d_2. \tag{13}$$

Using (12), $\tau^a(n) \le \tau^c(n-1)$, and (13) yields

$$\tau^d(n) - \tau^a(n) = \tau^d(n-1) + 1 - \tau^a(n)$$
$$\ge \tau^d(n-1) + 1 - \tau^c(n-1) = (k-1)d_2 + 1.$$

As $\tau^a(n) > \tau^a(n-1)$, we also have

$$\tau^d(n) - \tau^a(n) = \tau^d(n-1) + 1 - \tau^a(n)$$
$$\le \tau^d(n-1) - \tau^a(n-1) \le kd_2 - 1.$$

It then follows from (R1) that

$$\tau^c(n) = \tau^d(n) - d_2 \left\lfloor \frac{\tau^d(n) - \tau^a(n)}{d_2} \right\rfloor$$
$$= \tau^d(n) - (k-1)d_2. \tag{14}$$

As a direct result of (14), (13), and (12), we then have

$$\tau^c(n) = \tau^d(n) + \tau^c(n-1) - \tau^d(n-1) = \tau^c(n-1) + 1.$$

Case 2. $Bd_2 \le \tau^d(n-1) - \tau^a(n-1) \le Bd_2 + d_1$:

In this case, we have from (R1) that

$$\tau^c(n-1) = \tau^d(n-1) - Bd_2. \tag{15}$$

Using (12) and $\tau^a(n) \le \tau^c(n-1)$ yields

$$\tau^d(n) = \tau^d(n-1)+1 = \tau^c(n-1)+Bd_2+1 \ge \tau^a(n)+Bd_2+1.$$

From (R1), it follows that

$$\tau^c(n) = \tau^d(n) - Bd_2. \tag{16}$$

In conjunction with (15) and (12), we then have

$$\tau^c(n) = \tau^c(n-1) + 1.$$

(iii) To prove (9), let $n_0 = \sup\{m \le n : \tau^a(m) > \tau^d(m-1)\}$ be the index of the packet that initiates the busy period containing the nth packet. From (4), it follows that for all $n_0 < m \le n$

$$\tau^d(m) = \tau^d(m-1) + 1. \tag{17}$$

Note that the d_2 time interleaved linear compressors at the second stage are connected to the output link of the linear compressor at the first stage periodically with period d_2. If $n - d_2 \ge n_0$, then we have from (17) that $n^* = n - d_2$ is the last packet (in the busy period containing the nth packet) that departs before the nth packet from the same time interleaved linear compressor at the second stage. As such, it follows from (17) that

$$\tau^d(n) = \tau^d(n - d_2) + d_2 = \tau^d(n^*) + d_2. \tag{18}$$

On the other hand, if $n - d_2 < n_0$, then the nth packet arrives at an empty linear compressor at the second stage and there is no need to check (9). ∎

We remark that Theorem 2 is a generalization of one of our previous results on the constructions of linear compressors in [23] that holds only for $d_2 = d_1 + 1$ instead of $d_2 \leq d_1 + 1$ in Theorem 2. As shown in [23], the condition $d_2 = d_1 + 1$ for the two-stage construction leads to the multistage construction of a linear compressor in Figure 3. However, as we have shown in Section II, such a construction in Figure 3 does not have the fault tolerant capability. In contrast, in Section III-B and Section III-C, we will show that the general condition $d_2 \leq d_1 + 1$ for the two-stage construction in Theorem 2 is the key to the constructions of fault tolerant linear compressors.

B. A Multistage Construction of a Linear Compressor by a Concatenation of Scaled Optical Memory Cells

As it has been shown in [23] that an optical memory cell can be used as a linear compressor with maximum delay 1, it follows that the network element in Figure 6 is a special case of that in Figure 5 with $B = 1$. As such, it can be operated as a linear compressor with maximum delay $d_1 + d_2$ if $d_2 \leq d_1 + 1$.
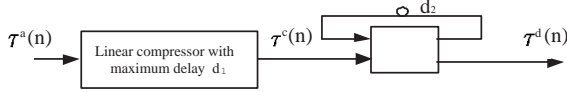

Fig. 6.   A construction of a linear compressor.

Note that if $d_1 = 1$, then the first stage in Figure 6 could be constructed by using an optical memory cell and we have a linear compressor by a concatenation of two scaled optical memory cells. On the other hand, if $d_1 > 1$ in Figure 6, then by recursively expanding the first stage, we obtain a concatenation of M scaled optical memory cells in Figure 7, where the ith scaled optical memory cell is with scaling factor d_i, $i = 1, 2, \ldots, M$, and $d_1 = 1$. Intuitively, with appropriate choice of the scaling factors $d_1, d_2, \ldots, d_M$, we expect that the network element in Figure 7 can be operated as a linear compressor with maximum delay $\sum_{i=1}^{M} d_i$.
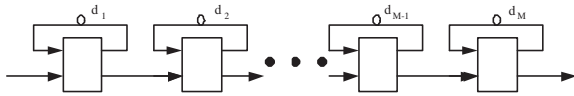

Fig. 7.   A construction of a linear compressor by a concatenation of scaled optical memory cells.

We will show that such a construction can be operated as a self-routing linear compressor if the delay lines are chosen to satisfy the condition in (A1).

To specify the routing in such a construction, let x be the delay of the nth packet, i.e., $x = \tau^d(n) - \tau^a(n)$. For x, we recursively compute the M-vector $\left(I_1(x), I_2(x), \ldots, I_M(x) \right)$ as follows:

$$I_M(x) = \begin{cases} 1, & \text{if } x \geq d_M, \\ 0, & \text{otherwise,} \end{cases} \qquad (19)$$

and for $i = M - 1, M - 2, \ldots, 1$,

$$I_i(x) = \begin{cases} 1, & \text{if } x - \sum_{k=i+1}^{M} I_k(x) \cdot d_k \geq d_i, \\ 0, & \text{otherwise.} \end{cases} \qquad (20)$$

The vector $\left(I_1(x), I_2(x), \ldots, I_M(x) \right)$ obtained this way is called the $\mathcal{C}$-transform of x in [19].

(R2)   Let $\tau_k^d(n)$ be the departure time of the nth packet from the kth stage, $k = 1, 2, \ldots, M - 1$. We set

$$\tau_k^d(n) = \tau^d(n) - \sum_{i=k+1}^{M} I_i(x) d_i \qquad (21)$$

for $k = 1, 2, \ldots, M - 1$.

It is known [19] that the $\mathcal{C}$-transform has the unique representation property for all $0 \leq x \leq \sum_{i=1}^{M} d_i$ under the condition in (A1), i.e.,

$$x = \sum_{i=1}^{M} I_i(x) d_i. \qquad (22)$$

As such, we also have from (21) that

$$\tau_k^d(n) = \tau^a(n) + \sum_{i=1}^{k} I_i(x) d_i. \qquad (23)$$

In other words, the delay line of the kth scaled optical memory cell is traversed by the nth packet if $I_k(x) = 1$.

Theorem 3 *Suppose that the network element in Figure 7 is started from an empty system. If (A1) holds, then under (R2) the construction in Figure 7 is a self-routing linear compressor with maximum delay $\sum_{i=1}^{M} d_i$.*

Proof.   We first show by induction that the network element consisting of the first k stages in Figure 7 can be operated as a linear compressor with maximum delay $\sum_{i=1}^{k} d_i$, $k = 1, 2, \ldots, M$. As $d_1 = 1$, this holds trivially for $k = 1$ as an optical memory cell can be used as a linear compressor with maximum delay 1.

Suppose as the induction hypothesis that for some $1 \leq k \leq M - 1$, the network element consisting of the first k stages in Figure 7 is a linear compressor with maximum delay $\sum_{i=1}^{k} d_i$. As the $(k+1)^{th}$ stage is a linear compressor with maximum delay 1 and scaling factor d_{k+1} and $d_{k+1} \leq \sum_{i=1}^{k} d_i + 1$, it then follows from Theorem 2 that the network element consisting of the first $k + 1$ stages in Figure 7 can be operated as a linear compressor with maximum delay $\sum_{i=1}^{k+1} d_i$. This completes the induction.

Now we show that the construction in Figure 7 is a *self-routing* linear compressor with the routing policy specified by (R2). Since the network element consisting of the first $M - 1$ stages in Figure 7 can be operated as a linear compressor with maximum delay $\sum_{i=1}^{M-1} d_i$, the construction in Figure 7 is a concatenation of a linear compressor with maximum delay $\sum_{i=1}^{M-1} d_i$ and a linear compressor with maximum delay 1 and scaling factor d_M. As such, we have from (R1) that

$\tau_{M-1}^d(n) = \tau^d(n) - I_M(x)d_M$, where x is the delay of the nth packet. Repeating the same argument yields

$$\tau_k^d(n) = \tau_{k+1}^d(n) - I_{k+1}(x)d_{k+1}$$
$$= \tau^d(n) - \sum_{i=k+1}^{M} I_i(x)d_i \qquad (24)$$

for $k = 1, 2, \ldots, M - 1$. ∎

Example 4 *(Binary representation) In particular, if we choose $d_k = 2^{k-1}$ for $k = 1, 2, \ldots, M$, then we have a self-routing linear compressor with maximum delay $2^M - 1$ as shown in Figure 3. For this particular case, the $\mathcal{C}$-transform of x is simply the binary representation of x.*

C. A General Construction of a Fault Tolerant Linear Compressor

Observe that if $K(F + 1) \leq M < (K + 1)(F + 1)$ for some $K \geq 1$, then for the straightforward construction that $d_{(k-1)(F+1)+1} = d_{(k-1)(F+1)+2} = \cdots = d_{k(F+1)} = 2^{k-1}$, $k = 1, 2, \ldots, K$, and $d_{K(F+1)+1} = d_{K(F+1)+2} = \cdots = d_M = 2^K$, the condition in (A1) is still satisfied even after up to F of the M optical memory cells are broken. As such, the network element in Figure 7 can still be operated as a linear compressor with maximum delay $\sum_{i=1}^{M-F} d_i$ even after up to F of the M optical memory cells detect faults. We can easily calculate that the maximum delay for such a direct construction is

$$\sum_{i=1}^{M-F} d_i = [M - (K-1)(F+1) + 1]2^{K-1} - F - 1. \quad (25)$$

As a result, for $F = 0$, we have $d_i = 2^{i-1}$ for $i = 1, 2, \ldots, M$, and the construction efficiency is equal to 1. For $F \geq 1$, the construction efficiency approaches $\frac{1}{F+1}$ as M tends to infinity, namely, the asymptotic construction efficiency is equal to $\frac{1}{F+1}$. Although the construction efficiency for such a straightforward construction is much smaller than 1 as F becomes large, such a direct construction guarantees that the network element in Figure 7 can still be operated as a linear compressor with maximum delay $\sum_{i=1}^{M-F} d_i$ even after up to F of the M optical memory cells are broken.

In the following theorem, we show how one constructs a linear compressor via fault/bypass optical memory cells that can tolerate up to F faulty optical memory cells and has construction efficiency greater than $\frac{1}{F+1}$.

Theorem 5 *Let $M \geq 1$ and $0 \leq F \leq M-1$. Suppose that the network element in Figure 7 is started from an empty system and all the optical memory cells in Figure 7 are fault/bypass optical memory cells. If the condition in (A2) is satisfied, then the construction in Figure 7 can still be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M-F} d_i$ even after up to F of the M optical memory cells detect faults.*

Proof. Assume that there are $\tilde{F}$ optical memory cells that detect faults, where $0 \leq \tilde{F} \leq F$. With the bypass circuit, it becomes a concatenation of $M - \tilde{F}$ scaled optical memory cells. Let $\tilde{d}_k$, $k = 1, 2, \ldots, M - \tilde{F}$, be the scaling factor of the kth optical memory cell in these $M - \tilde{F}$ optical memory cells. Clearly, $\tilde{d}_k = d_j$ for some $k \leq j \leq k + \tilde{F}$. Since we assume that $d_k \leq d_{k+1}$ for all k in (A2), it follows that

$$d_k \leq \tilde{d}_k \leq d_{k+\tilde{F}} \qquad (26)$$

for all $k = 1, 2, \ldots, M - \tilde{F}$.

Now we verify that (A1) still holds for the delays $\tilde{d}_1, \tilde{d}_2, \ldots, \tilde{d}_{M-\tilde{F}}$. As $d_i = 1$ for $i = 1, 2, \ldots, F + 1$, and $\tilde{F} \leq F$, we have

$$1 = d_1 \leq \tilde{d}_1 \leq d_{\tilde{F}+1} = 1,$$

implying that $\tilde{d}_1 = 1$. For $0 \leq k \leq F - \tilde{F}$, we have from (26) and $d_i = 1$, $i = 1, 2, \ldots, F + 1$, that

$$\tilde{d}_{k+1} \leq d_{k+1+\tilde{F}} = 1 \leq \sum_{i=1}^{k} \tilde{d}_i + 1.$$

Similarly, for $F - \tilde{F} + 1 \leq k \leq M - \tilde{F} - 1$, we have from (26), (A2), and $\tilde{F} \leq F$ that

$$\tilde{d}_{k+1} \leq d_{k+1+\tilde{F}} \leq \sum_{i=1}^{k+\tilde{F}-F} d_i + 1 \leq \sum_{i=1}^{k} d_i + 1 \leq \sum_{i=1}^{k} \tilde{d}_i + 1.$$

From Theorem 3, the concatenation of the remaining $M - \tilde{F}$ scaled optical memory cells can be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M-\tilde{F}} \tilde{d}_i$. Since $\tilde{F} \leq F$ and $d_k \leq \tilde{d}_k$ for all k in (26), it is also a self-routing linear compressor with maximum delay $\sum_{i=1}^{M-F} d_i$. ∎

Example 6 *(Generalized Fibonacci series) Let $M \geq 1$ and $0 \leq F \leq M - 1$. Consider the series of fiber delay lines with $d_i = 1$ for all $i = 1, 2, \ldots, F + 1$, and $d_{k+F} = d_{k+F-1} + d_{k-1}$ for all $k = 2, 3, \ldots, M - F$. We call such a series the generalized Fibonacci series of order F. Note that when $F = 0$, the generalized Fibonacci series reduces to the series of powers of 2, i.e., $d_k = 2^{k-1}$, $k = 1, 2, \ldots, M$. Also note that the well-known Fibonacci series is a special case of the generalized Fibonacci series with $F = 1$.*

We show that such a series of delays satisfy the condition in (A2). Clearly, we have $d_k \leq d_{k+1}$ for all $k = 1, 2, \ldots, M-1$. Now we argue by induction that

$$d_{k+F} = \sum_{i=1}^{k-1} d_i + 1 \qquad (27)$$

for all $k = 2, 3, \ldots, M - F$. For $k = 2$, we have $d_{F+2} = d_{F+1} + d_1 = d_1 + 1$. Suppose that (27) holds for some $2 \leq k \leq M - F - 1$. Then we have

$$d_{k+1+F} = d_{k+F} + d_k = \sum_{i=1}^{k-1} d_i + 1 + d_k = \sum_{i=1}^{k} d_i + 1. \quad (28)$$

Since the Fibonacci series grows exponentially at the rate of the golden ratio $(\sqrt{5} + 1)/2$, the efficiency for the construction that uses the Fibonacci series as the delays of

F	0	1	2	3	4
$\frac{1}{F+1}$	1	0.5	0.333333	0.25	0.2
ρ_F	1	0.694242	0.551463	0.464958	0.405685
F	5	6	7	8	9
$\frac{1}{F+1}$	0.166667	0.142857	0.125	0.111111	0.1
ρ_F	0.361992	0.328173	0.301066	0.278758	0.260015
F	10	11	12	13	14
$\frac{1}{F+1}$	0.909091	0.083333	0.076923	0.071429	0.066667
ρ_F	0.244006	0.230142	0.218000	0.207260	0.197682
F	15	16	17	18	19
$\frac{1}{F+1}$	0.0625	0.058824	0.055556	0.052632	0.05
ρ_F	0.189077	0.181297	0.174222	0.167757	0.161822

TABLE I

ASYMPTOTIC CONSTRUCTION EFFICIENCY ρ_F BY USING THE
GENERALIZED FIBONACCI SERIES OF ORDER F FOR $0 \leq F \leq 19$

the fiber delay lines approaches $\log_2(\frac{\sqrt{5}+1}{2}) = 0.694242$ as M tends to infinity. This is much better than the naive construction that uses two scaled optical memory cells at each stage. In general, the generalized Fibonacci series of order F grows exponentially at the rate of r_F, where r_F is the root of the equation $r^{F+1} - r^F - 1 = 0$ with the largest magnitude. It follows that its construction efficiency $\rho_{M,F} = \log(\sum_{i=1}^{M-F} d_i + 1)/M = \log(d_{M+1})/M$ approaches the asymptotic construction efficiency $\rho_F = \log_2(r_F)$ as M tends to infinity. As can be seen from Table I, for $F \geq 1$ this is much better than the asymptotic construction efficiency $1/(F+1)$ of the naive construction that uses $(F+1)$ scaled optical memory cells at each stage.

D. An Optimal Construction of a Fault Tolerant Linear Compressor

In this section, we show that the construction by the generalized Fibonacci series of order F in Example 6 is the optimal construction that maximizes the construction efficiency among all the constructions that can tolerate up to F faulty optical memory cells by using M scaled optical memory cells.

Let $d_i^* = 1$ for all $i = 1, \ldots, F+1$, and let

$$d_{k+F}^* = \sum_{i=1}^{k-1} d_i^* + 1 \tag{29}$$

for all $k = 2, 3, \ldots, M-F$. Let

$$D_{M,F}^* = \sum_{k=1}^{M-F} d_k^*. \tag{30}$$

Theorem 7 Let $M \geq 1$ and $0 \leq F \leq M-1$. Consider a linear compressor that is constructed by using M scaled optical memory cells. Suppose that it can still be operated as a linear compressor with maximum delay d after up to F of the M optical memory cells detect faults. Then $d \leq D_{M,F}^*$, where $D_{M,F}^*$ is defined in (30).

Proof. Suppose that there are F optical memory cells that detect faults. Let $\tilde{d}_1, \tilde{d}_2, \ldots, \tilde{d}_{M-F}$ be the ordered scaling

factors (from the smallest to the largest) of the remaining $M - F$ scaled optical memory cells so that $\tilde{d}_k \leq \tilde{d}_{k+1}$ for all $k = 1, 2, \ldots, M-F-1$.

As the remaining scaled optical memory cells can be operated as a linear compressor with maximum delay d, we have $\tilde{d}_1 = 1$. Otherwise, a packet with delay equal to 1 can not depart at its departure time as this packet must be stored in one of the fibers and the delay of every fiber delay line is greater than 1 in this case.

Let j be the smallest positive integer less than $M - F$ such that $\tilde{d}_{j+1} > \sum_{i=1}^{j} \tilde{d}_i + 1$. If there does not exist such a positive integer, let $j = M - F$. We claim that

$$d \leq \sum_{i=1}^{j} \tilde{d}_i. \tag{31}$$

We prove this claim by contradiction. Suppose that j is the smallest positive integer less than $M - F$ such that $\tilde{d}_{j+1} > \sum_{i=1}^{j} \tilde{d}_i + 1$. Consider the sample path that a packet initiates a busy period at time t and with delay equal to $\sum_{i=1}^{j} \tilde{d}_i + 1$, and there is a packet in every time slot $t+1, t+2, \ldots$. From the monotone and consecutive condition of a linear compressor, we see that the delays for all the packets after time t are also equal to $\sum_{i=1}^{j} \tilde{d}_i + 1$. Therefore, at time $t_1 = t + \sum_{i=1}^{j} \tilde{d}_i$, there are $\sum_{i=1}^{j} \tilde{d}_i + 1$ packets with delays equal to $\sum_{i=1}^{j} \tilde{d}_i + 1$ stored in the fiber delay lines with delays $\tilde{d}_k$, $k = 1, 2, \ldots, M-F$. As at each time instance the fiber delay lines with delays $\tilde{d}_i$, $i = 1, 2, \ldots, j$, can only accommodate a maximum of $\sum_{i=1}^{j} \tilde{d}_i$ packets, at least one of the $\sum_{i=1}^{j} \tilde{d}_i + 1$ packets at time t_1 must be stored in a fiber delay line with delay $\tilde{d}_k$ for some $k \geq j+1$, and that packet can not depart at the right time since it has a packet delay $\sum_{i=1}^{j} \tilde{d}_i + 1$ which is smaller than $\tilde{d}_k$, $k \geq j+1$. As such, the maximum delay d of the linear compressor is at most $\sum_{i=1}^{j} \tilde{d}_i$. On the other hand, if $\tilde{d}_{k+1} \leq \sum_{i=1}^{k} \tilde{d}_i + 1$ for all $k = 1, 2, \ldots, M-F-1$, then $j = M - F$ and we can prove that $d \leq \sum_{i=1}^{M-F} \tilde{d}_i$ by a similar argument.

Note that from the definition of j, we have $\tilde{d}_1 = 1$ and $\tilde{d}_{k+1} \leq \sum_{i=1}^{k} \tilde{d}_i + 1$ for all $k = 1, 2, \ldots, j-1$. Let $d_{(i)}$, $i = 1, 2, \ldots, M$, be the ith smallest element in $\{d_1, d_2, \ldots, d_M\}$. Clearly, for all $k = 1, 2, \ldots, M-F$, we have $\tilde{d}_k = d_{(i)}$ for some $k \leq i \leq k+F$. As $\tilde{d}_1 = 1$, we must have $d_{(i)} = \tilde{d}_1 = 1$, $i = 1, 2, \ldots, F+1$. For a fixed $1 \leq k \leq j-1$, consider the special case that $\tilde{d}_i = d_{(i)}$, $i = 1, \ldots, k$, and $\tilde{d}_{k+1} = d_{(k+1+F)}$, then we have

$$d_{(k+1+F)} \leq \sum_{i=1}^{k} d_{(i)} + 1 \tag{32}$$

We are now in a position to show that

$$d_{(i)} \leq d_i^*, \quad i = 1, 2, \ldots, j+F. \tag{33}$$

We will prove (33) by induction. We already have $d_{(i)} = 1 = d_i^*$, $i = 1, 2, \ldots, F+1$. Assume for some $1 \leq k \leq j-1$ that (33) holds for all $i = 1, 2, \ldots, k+F$ as the induction hypothesis. It then follows from (32), the induction hypothesis,

and (29) that

$$d_{(k+1+F)} \leq \sum_{i=1}^{k} d_{(i)} + 1 \leq \sum_{i=1}^{k} d_i^* + 1 = d_{k+1+F}^*.$$

Finally, for the special case that $\tilde{d}_i = d_{(i)}$, $i = 1, 2, \ldots, M - F$, we have from (31), (33), $j \leq M - F$, and (30) that

$$d \leq \sum_{i=1}^{j} \tilde{d}_i = \sum_{i=1}^{j} d_{(i)} \leq \sum_{i=1}^{j} d_i^* \leq \sum_{i=1}^{M-F} d_i^* = D_{M,F}^*.$$

The proof is completed. ■

The following corollary follows directly from Theorem 7 and Example 6.

Corollary 8 *The asymptotic construction efficiency for a linear compressor that can tolerate up to F faulty optical memory cells by using M scaled optical memory cells is bounded above by $\rho_F = \log_2(r_F)$, where r_F is the root of the equation $r^{F+1} - r^F - 1 = 0$ with the largest magnitude.*

IV. AN OPTIMAL CONSTRUCTION OF A FAULT TOLERANT LINEAR DECOMPRESSOR

The mirror image of an SDL element is an SDL element that reverses the direction of every link in the original SDL element. By so doing, the inputs (resp. outputs) of the original SDL element become the outputs (resp. inputs) of its mirror image. It is obvious that if a sample path can be realized by an SDL element, then its time reversed sample path can also be realized by the mirror image of the SDL element

The mirror image of a linear compressor is called a linear decompressor in [23] as defined below:

Definition 9 (Linear decompressors [23]) *Suppose that the departure time of a packet is known upon its arrival. Let $\tau^a(n)$ and $\tau^d(n)$ be the arrival time and the departure time, respectively, of the nth packet. A network element with a single input link and a single output link is called a* linear decompressor *with the range of delay $[d_1, d_2]$ if it realizes the set of mappings that satisfy (1), the FIFO condition: $\tau^d(n - 1) < \tau^d(n)$ for all n, and the following* inverse monotone and consecutive condition: $\tau^a(n) = \tau^a(n - 1) + 1$ whenever $\tau^a(n) \leq \tau^d(n - 1)$. In particular, if $d_1 = 0$, then it is called a linear decompressor with maximum delay d_2.

Suppose a linear decompressor with maximum delay d is constructed by using M scaled optical memory cells. As for a linear compressor, its efficiency ρ is defined as

$$\rho = \frac{\log_2(d + 1)}{M}. \tag{34}$$

As a linear decompressor is the mirror image of a linear compressor, the construction in Figure 7 can be operated as a linear decompressor and the optimal construction efficiency is achieved by the generalized Fiboncacci series as stated in the following theorem and its corollary.

Theorem 10 *Let $M \geq 1$ and $0 \leq F \leq M - 1$. Suppose that the network element in Figure 7 is started from an empty system and all the optical memory cells in Figure 7 are fault/bypass optical memory cells. Let $d_i' = d_{M+1-i}$, $i = 1, 2, \ldots, M$. If $d_i' = 1$ for all $i = 1, 2, \ldots, F + 1$, and*

$$d_{k+F-1}' \leq d_{k+F}' \leq \sum_{i=1}^{k-1} d_i' + 1 \tag{35}$$

for all $k = 2, 3, \ldots, M - F$, then the construction in Figure 7 can still be operated as a self-routing linear decompressor with maximum delay $\sum_{i=1}^{M-F} d_i'$ even after up to F of the M optical memory cells detect faults.

Conversely, consider a linear decompressor that is constructed by using M scaled optical memory cells. Suppose that it can still be operated as a linear decompressor with maximum delay d after up to F of the M optical memory cells detect faults. Then $d \leq D_{M,F}^*$, where $D_{M,F}^*$ is defined in (30).

Corollary 11 *The asymptotic construction efficiency for a linear decompressor that can tolerate up to F faulty optical memory cells by using M scaled optical memory cells is bounded above by $\rho_F = \log_2(r_F)$, where r_F is the root of the equation $r^{F+1} - r^F - 1 = 0$ with the largest magnitude.*

V. CONCLUSIONS

In this paper, have considered SDL constructions of fault tolerant linear compressors and linear decompressors. The basic network element for our constructions is scaled optical memory cell, which is constructed by a 2×2 optical crossbar switch and a fiber delay line. Such consideration of fault tolerant capability is extremely important and challenging from a practical point of view as otherwise the linear compressors and linear decompressors may fail to function properly even when a single scaled optical memory cell is broken.

We first provided a two-stage construction of a linear compressor. Such a two-stage construction was recursively expanded to give a multistage construction of a self-routing linear compressor by a concatenation of scaled optical memory cells. We have shown that if the delays $d_1, d_2, \ldots, d_M$ satisfy the condition in (A1), then our multistage construction can be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M} d_i$. We have also shown a more general result that if the delays $d_1, d_2, \ldots, d_M$ satisfy the condition in (A2), then our multistage construction can be operated as a self-routing linear compressor with maximum delay $\sum_{i=1}^{M-F} d_i$ even after up to F of the M scaled optical memory cells are broken. Furthermore, we have proved that our multistage construction with the delays $d_1, d_2, \ldots, d_M$ given by the generalized Fibonacci series of order F is the best among all constructions of a linear compressor that can tolerate up to F faulty scaled optical memory cells by using M scaled optical memory cells. Similarly results were also obtained for the constructions of fault tolerant linear decompressors.

One of our on going research problems is on the constructions of fault tolerant optical 2-to-1 FIFO multiplexers. For

this, we have considered the feedback system in our previous work [19]. In that paper, we have obtained a necessary and sufficient condition on the delays of the fiber delay lines in the feedback system so that it can be operated as an optical 2-to-1 FIFO multiplexer. Our preliminary investigation shows that under a more general condition on the delays of the fiber delay lines, the feedback system can be operated as an optical 2-to-1 FIFO multiplexer when some of the fibers are broken. Results along this line will be reported separately.

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