A 10-Gb/s CML I/O Circuit for Backplane Interconnection in 0.18-μm CMOS Technology

Min-Sheng Kao, Jen-Ming Wu, *Member, IEEE*, Chih-Hsing Lin, Fan-Ta Chen, Ching-Te Chiu, *Member, IEEE*, and Shawn S. H. Hsu, *Member, IEEE*

***Abstract*—A 10-Gb/s current mode logic (CML) input/output (I/O) circuit for backplane interconnect is fabricated in 0.18-μm 1P6M CMOS process. Comparing with conventional I/O circuit, this work consists of input equalizer, limiting amplifier with active-load inductive peaking, duty cycle correction and CML output buffer. To enhance circuit bandwidth for 10-GB/s operation, several techniques include active load inductive peaking and active feedback with current buffer in Cherry–Hooper topology. With these techniques, it reduces 30%–65% of the chip area comparing with on-chip inductor peaking method. This design also passes the interoperability test with switch fabric successfully. It provides 600-$\mathrm{mV_{pp}}$ differential voltage swing in driving 50-Ω output loads, 40-dB input dynamic range, 40-dB voltage gain, and 8-mV input sensitivity. The total power consumption is only 85 mW in 1.8-V supply and the chip feature die size is 700 μm$\times$ 400μm.**

***Index Terms*—Cherry–Hooper topology, current-mode logic, inductive peaking, limiting amplifier.**

I. Introduction

With the access network including digital subscriber line (DSL), passive optical network (PON), IEEE 802.11/5/6 and 3/3.5 G phone service being widely deployed in past few years, the data traffic is easily up to 1-Gb/s. Central office equipments operated at speed of OC48 (2.5-Gb/s) to OC192 (10-Gb/s) and the backplane need to support high speed serial link of data to replace parallel bus in many applications [1].

A typical switch fabric system is shown in Fig. 1, which contains line cards, switch fabric core and backplane with connectors which route to each line cards. The switch fabric also integrates multi-channel Serializer/De-Serializer (SerDes) with current mode logic (CML) input/output (I/O) interface. To overcome parallel buses crosstalk and EMI, etc., issues, the design trends are using SerDes with CML I/O for high speed operation.

Manuscript received August 07, 2007; revised October 25, 2007. Current version published April 22, 2009. This work was supported by the National Science Council, Taiwan, R.O.C., under the Program for Promoting Academic Excellence of Universities (Phase II) (NSC 96-2752-E-007-002-PAE).

M.-S. Kao is with the Institute of Communications Engineering, National Tsing Hua University, Hsinchu 300, Taiwan, and also with Mindspeed Technologies Inc., Taipei 110, Taiwan (e-mail: kaom0711@gmail.com).

J.-M. Wu, C.-H. Lin, and F.-T. Chen are with the Institute of Communications Engineering, Department of Electrical Engineering, National Tsing Hua University, Hsinchu 300, Taiwan (e-mail: jmwu@ee.nthu.edu.tw; d915607@oz.nthu.edu.tw; fanta524cf@yahoo.com.tw).

C.-T. Chiu is with the Institute of Communications Engineering, and the Department of Computer Science, National Tsing Hua University, Hsinchu 300, Taiwan (e-mail: ctchiu@cs.nthu.edu.tw).

S. S. H. Hsu is with the Department of Electrical Engineering, National Tsing Hua University, Hsinchu 300, Taiwan (e-mail: shhsu@ee.nthu.edu.tw).

Digital Object Identifier 10.1109/TVLSI.2009.2016726

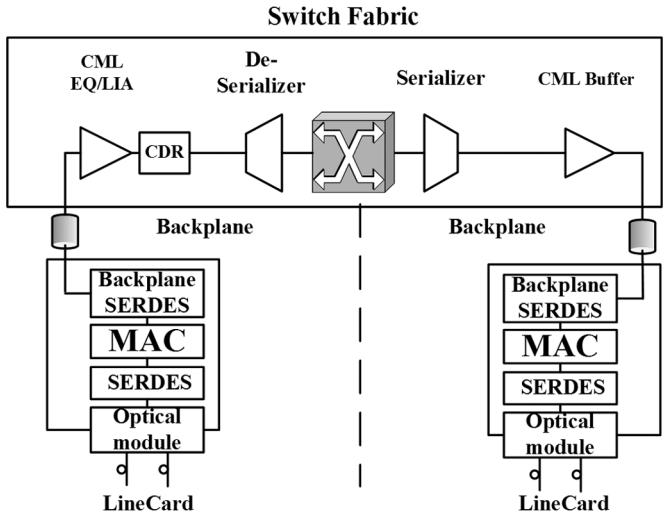

Fig. 1. Block diagram of a typical switch fabric systems.

CML is suitable for backplane interconnection due to its low swing and pure differential architecture. Most of the prior arts [2]–[6] use inductor peaking to enhance bandwidth but it occupies chip area and not suitable for highly integrated system-on-chip (SOC) like multi-channel switch fabric. On the other hand, this proposed CML I/O circuit has been under the interoperability test with a novel load balanced Birkhoff-von Neumann switch in the mean time [7]–[10]. This paper presents the CML I/O circuits include input (EQ/LIA) and output (CML buffer) interfaces and is organized as the following. Section II describes the architecture of the CML I/O interface. The EQ, LIA, and CML output buffer are codesigned to examine the performance together, and the design techniques and circuit structures are discussed in Section III. To achieve wide-band and high-gain design goals, inductive peaking is adopted by using PMOS active load and active feedback in Cherry–Hooper topology [11]. Section IV describes the experimental results. Conclusions are presented in Section V.

II. CML I/O Architecture

The block diagram of the CML I/O interface is shown in Fig. 2.

CML input interface consists of an equalizer and a limiting amplifier which includes dc-offset canceling function. CML output interface simply designs with CML output buffer.

The equalizer input stage is self-biased with 100-Ω differential impedance and a modified Cherry–Hooper topology including capacitive source degeneration architecture is adopted. The limiting amplifier has five inductive peaking gain-stages

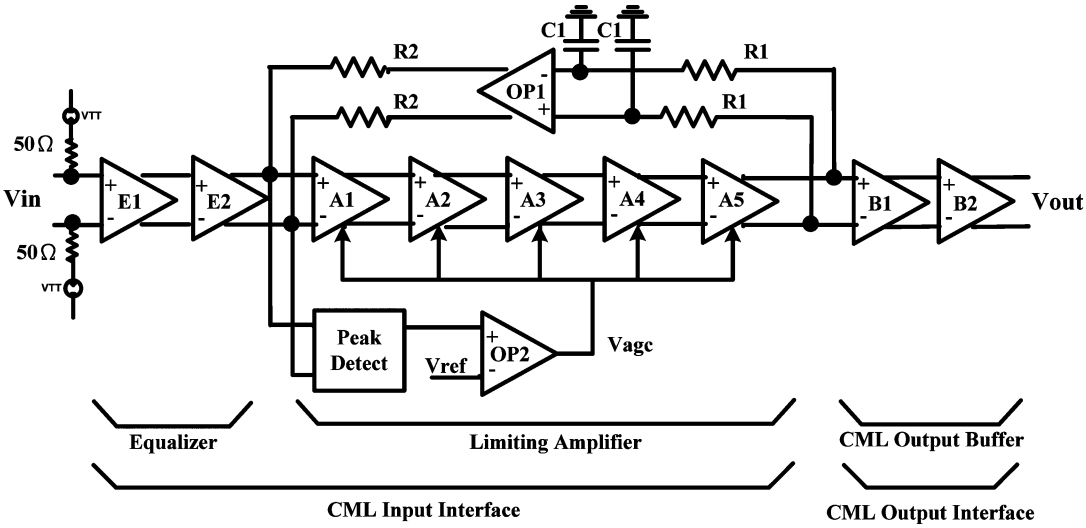

Fig. 2. Block diagram of CML I/O architecture.

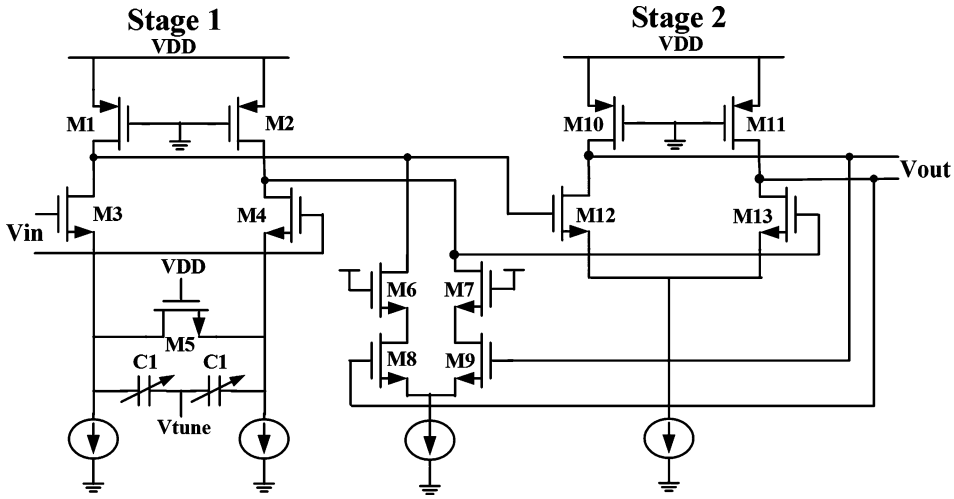

Fig. 3. Block diagram of equalizer.

$(A1, A2, \ldots,$ and $A5)$ with active feedback to increase bandwidth and auto gain control (AGC) to extend dynamic range and improve jitter performance. At the same time, differential dc-offset error signal from gain stage A5 feeds back to gain stage A1 with low-pass filter (C1 and R1) and differential operation amplifier (OP1) to keep output waveform in 50% duty cycle. Following the limiting amplifier are CML output buffer stages (B1 and B2), which uses the same inductive peaking and active feedback techniques to increase circuit bandwidth for enhancing the operation speed to 10-Gb/s.

Moreover, this CML output buffer is designed to drive 50-Ω resistive load and output swing is over 600-$\mathrm{mV_{pp}}$.

III. CML I/O Circuit Blocks

A. Equalizer

Fig. 3 shows the equalizer circuit that employs the modified Cherry–Hooper amplifier topology which consists of two stage amplifier with active feedback [11], [12]. The main advantage of Cherry–Hooper topology is it can maintain the high gain and high bandwidth at the same time. Furthermore, this design includes M6 and M7 that act as the ideal current buffers to reinforce Cherry–Hooper performance by getting better active feedback properties. The equalizer also includes tunable source degeneration function (C1 and M5) and the high-frequency signal amplitude can be changed by tuning varactor C1. Comparing prior art [13], this architecture can simply maintain input voltage swing and only compensate high-frequency signal loss. The equalizer is a two-stage design. Stage 1 is a trans-conductance amplifier; Stage 2 is a trans-impedance amplifier and active feedback circuitry which increases the overall bandwidth and also keeps the high voltage gain.

Assuming each gain cell is approximated by a two-pole amplifier then its conversion gain can be described by $A(s)$ in (1) [2]. Source denegation effect is temporarily neglected here and it will be discussed separately in the following:

$$A(s) = \frac{A\nu \times \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{1}$$

$$A\nu = \frac{G_{M3}G_{M12}R_{M1}R_{M10}}{1 + G_{M8}G_{M12}R_{M1}R_{M10}} \tag{2}$$

$$A\nu = \frac{1 + G_{M8}G_{M12}R_{M1}R_{M10}}{R_{M1}R_{M10}C_{M3}C_{M12}} \tag{3}$$

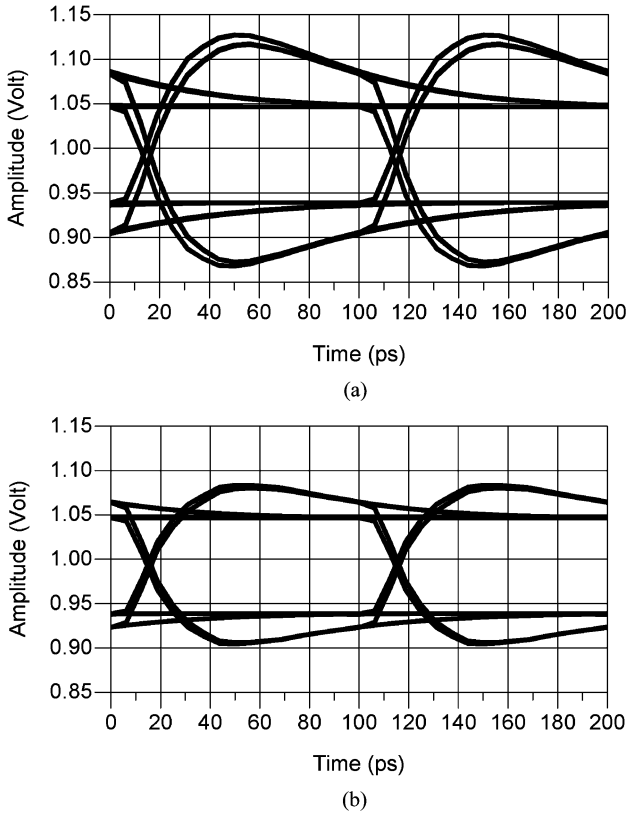

Fig. 4. EQ simulated output eye diagram: (a) $\mathrm{Vtune} = 0$ V; (b) $\mathrm{Vtune} = 1.8$ V.

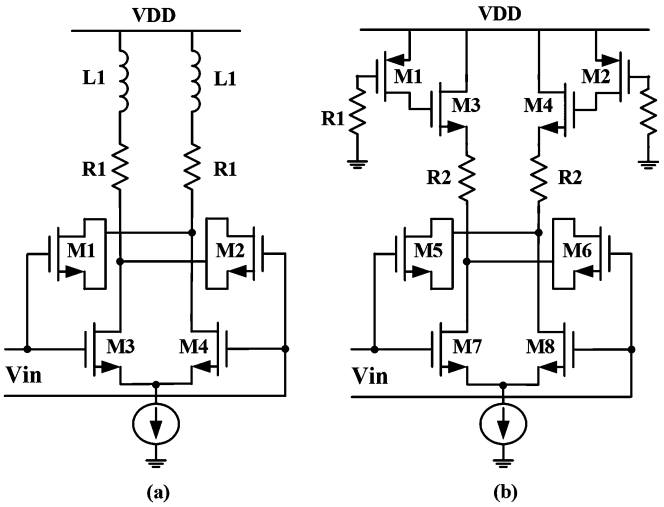

Fig. 5. Basic CML Gain stage: (a) passive inductive peaking; (b) active inductive peaking.

$$\xi = \frac{1}{2}\frac{R_{M1}C_{M3}+R_{M10}C_{M12}}{\sqrt{R_{M1}C_{M3}R_{M10}C_{M12}(1+G_{M8}G_{M12}R_{M1}R_{M10})}}. \tag{4}$$

C_{M3} and C_{M12} represent the parasitic capacitance at the drain node of M3 and M12 and R_{M12} and R_{M1} represent the equivalent resistive load of M1 and M10, respectively. G_{M12} and G_{M10} denote the transconductance of the differential pair (M3–M4) and (M12–M13) and G_{M8} is the transconductance

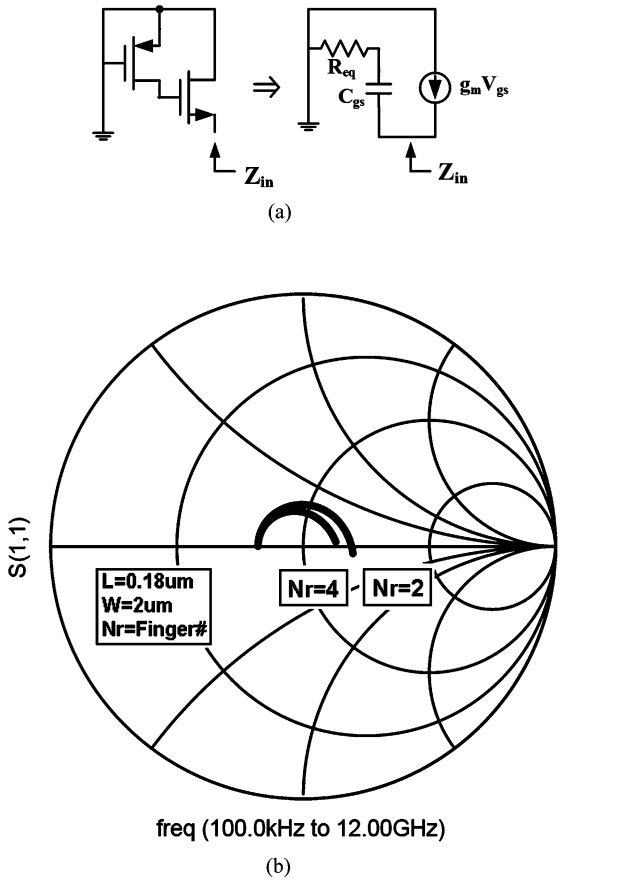

Fig. 6. Active inductive peaking circuit illustration: (a) circuit modeling; (b) smith chart.

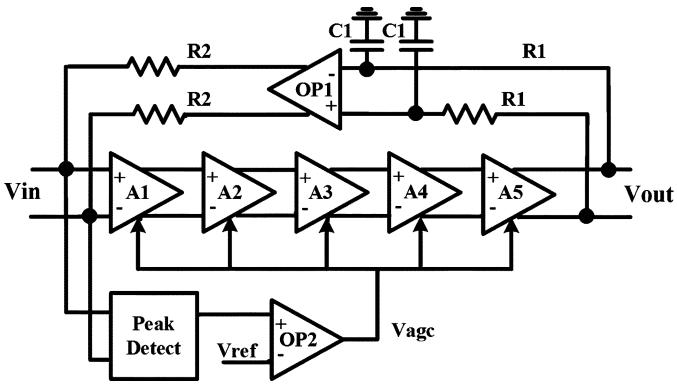

Fig. 7. LIA architectures.

of the active feedback stage (M8–M9). M6 and M7 effect is combined into active feedback stage and it will increase the low-frequency voltage gain but does not affect the overall bandwidth.

To achieve tunable high-frequency compensation capability, source degeneration technique is applied and transconductance of (M3–M4) can be derived as G_{M3SD} by half-circuit analysis method. In another word, G_{M3} can be represented with G_{M3SD}. By substituting into (1), we obtain complete transfer function as in (5)

$$G_{M3SD} = \frac{1}{2}\left[\frac{G_{M3}(1+sR_{M5}C_1)}{G_{M3}R_{M5}+2(1+sR_{M5}C_1)}\right]. \tag{5}$$

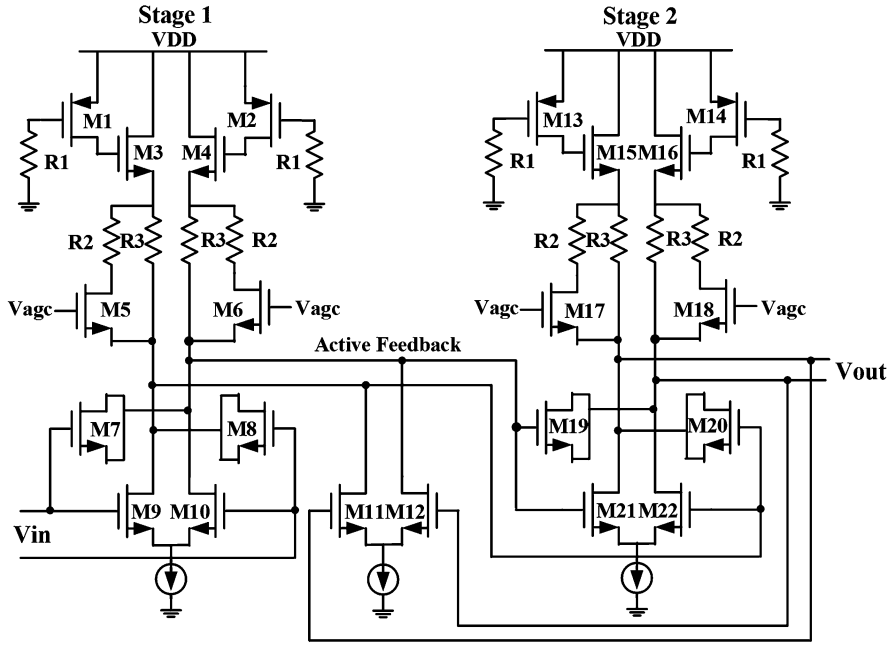

Fig. 8. LIA gain stage.

R_{M5} denotes the equivalent resistive load of the M5 and $2C_1$ equals the capacitance of C1. From (5), G_{M3SD} contains a zero at $(R_{M5}C_1)^{-1}$ and if the zero cancels the pole at drain of M3 then bandwidth will increase by a factor of $[1+1/2(G_{M3}R_{M5})]$. By the way, the zero of equalizer can be adjusted by the capacitance of C1 varactor which is controlled by Vtune and Fig. 4 shows the simulated output waveform for $\mathrm{Vtune} = 0$ and 1.8 V. High-frequency gain varies with C1 capacitance and it reveals rising edge peaking in time domain waveform.

B. Limiting Amplifier

Fig. 5 shows the basic CML gain stage circuit diagram with conventional passive inductive peaking and with proposed active inductive peaking. By using active inductive peaking, the chip area can shrink dramatically and phase shift is minimized.

The equivalent small signal model of active inductive circuit and a plot of its simulated S11 are shown in Fig. 6(a) and (b), respectively.

The input impedance of active inductive circuit can be described as

$$Z_{\mathrm{in}} = \frac{V_x}{I_x} = \frac{1 + sR_{\mathrm{eq}}C_{gs}}{g_m + sC_{gs}}. \tag{6}$$

$R\mathrm{eq}$ denotes the equivalent resistive load of the M1 and Cgs equals the M3 gate-source parasitic capacitance. The input impedance $Z11$ increases with frequency and behaves as the series L-R network. Based on the simulated Smith Chart, the active inductor self-resonant frequency is approximately 12 GHz and then becomes capacitive. The equivalent inductor also varies with the width of M1 which is expressed as R_{eq} in (6). Fig. 7 shows the complete LIA architecture includes automatic gain control function, dc-offset cancelling (DCC) network and consecutive gain stages to provide about 40 dB conversion gain. DC-offset cancelling network is composed of a differential operation amplifier (OP1) and low-pass filter (C1 and R1). To compensate for an input-referred offset voltage of roughly 20 mV, R2 needs to be around 1 k-Ω.

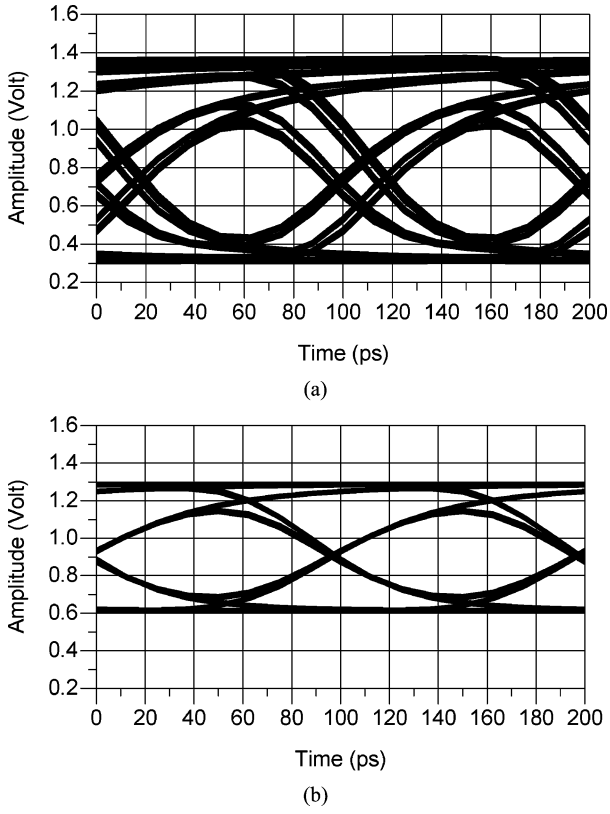

Fig. 9. LIA simulated output eye diagram: (a) AGC-off; (b) AGC-on.

On the other hand, due to the high conversion gain, the gain stage will saturate when input voltage is increasing and output eye diagram is getting distorted and induce more jitter. To enlarge the input dynamic range and improve the jitter perfor-

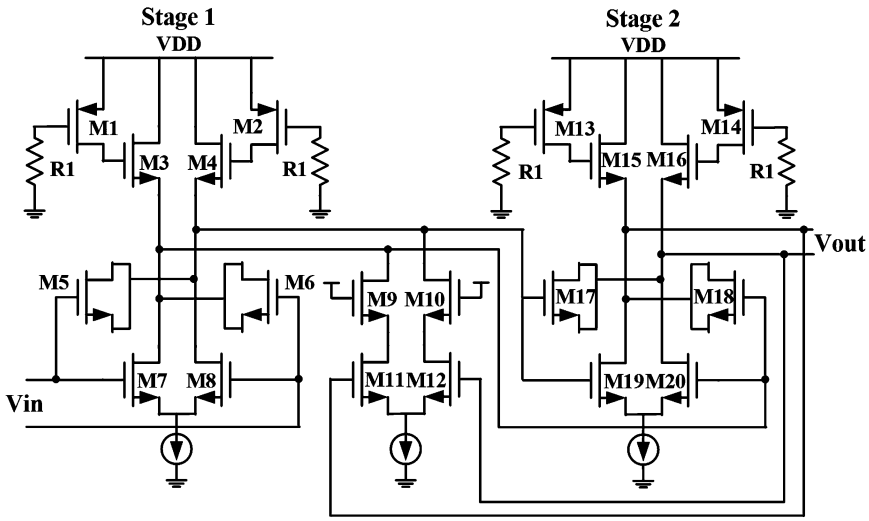

Fig. 10. Block diagram of CML output buffer.

mance, AGC is presented in this design. The function of AGC is based on input swing peak detection and AGC kick-in voltage (Vref) which is presented in Fig. 7. Operation amplifier (OP2) acts like a comparator and output AGC control voltage to the gain stages $(A1, A2, \ldots,$ and $A5)$ by comparing the Vref. The typical AGC kick-in point is around input swing over 30 $\mathrm{mV_{pp}}$.

Fig. 8 shows block diagram of limiting amplifier gain stage. This gain stage design still adopts Cherry–Hopper architecture with active feedback, active inductive peaking and tunable resistive load. Tunable load is achieved by (R2, M5, M6, M17, and M18) and the R2/R3 ratio will determine the gain factor in AGC region. To compromise between the conversion gain and jitter performance over full input swing range, the rule of thumb R2/R3 ratio is roughly equal to $1/\sqrt{2}$. At the same time, negative miller capacitance also helps in mending eye-opening margin by cancelling the parasitic effect of the current switch differential (M9–M10) and (M21–M22). Similar AGC concept is presented [14]. It needs complicated multiple peak-detector circuit and using closed-loop architecture which increases design complexity.

Fig. 9 compared simulated output waveform with AGC-on and AGC-off. The output swing is reduced in AGC region but jitter, eye diagram opening and rise/fall time of the wave form are obviously improved. Especially, it eliminates the double edge of eye pattern and enhances the signal integrity.

C. CML Buffer

The proposed CML output buffer which presents in Fig. 10 is simply based on modified Cherry–Hopper architecture which mentioned in previous equalizer design section but using active inductive load instead of PMOS. The second stage of CML buffer is designed to provide over 8 mA driving current and over 300 $\mathrm{mV_{pp}}$ voltage swing with 50-Ω output load [11], [15]–[17].

Fig. 11 presents the simulated S21 plot and output eye diagram which bases on PMOS (M1 and M2) parameters value ($L = 0.18$ μm, $W = 2$ μm and $\mathrm{Nr} = 4$). By changing the M1 and M2 finger numbers (equivalent width), the bandwidth of the

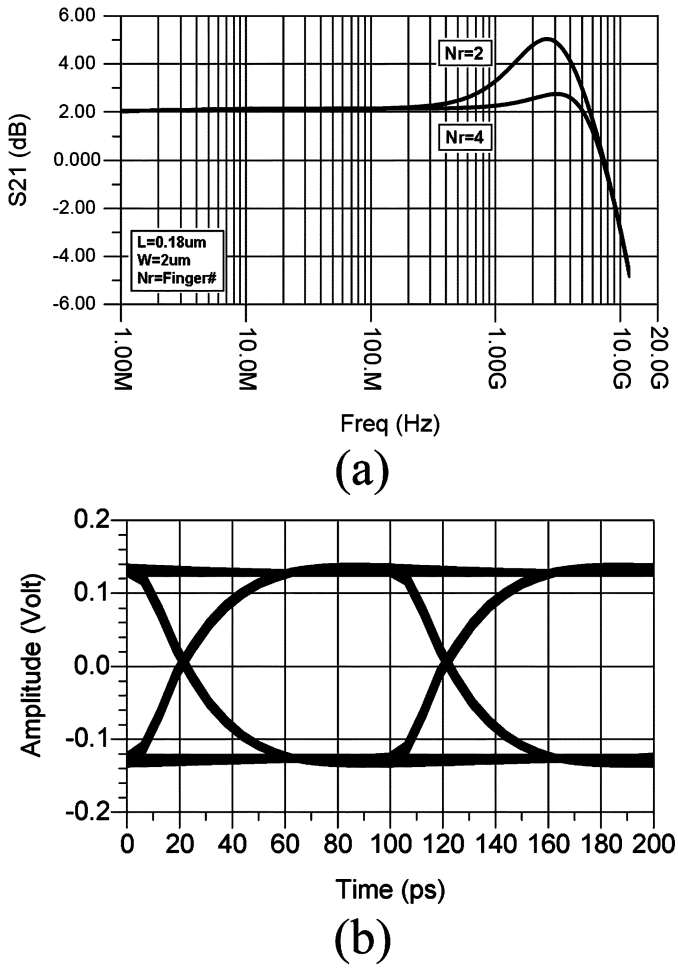

Fig. 11. CML buffer simulated output diagram: (a) S21 plot; (b) Eye waveform (50-Ω output load).

CML buffer can be adjusted and it decreases with pMOS device size. The drawback of the increasing peaking at high frequency region is the penalty of signal distortion and eye quality needs to be optimized by design.

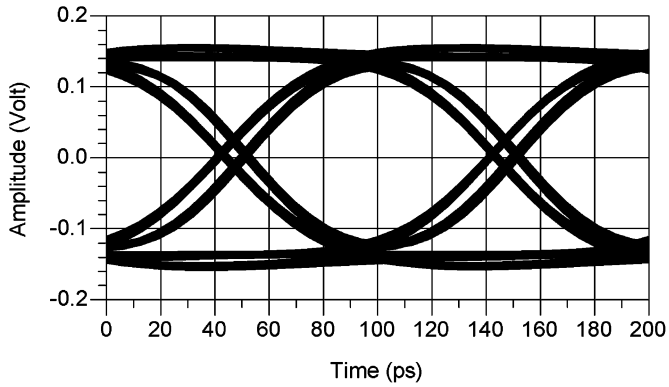

Fig. 12. Overall CML I/O structure simulated output eye diagram (50-Ω output load).

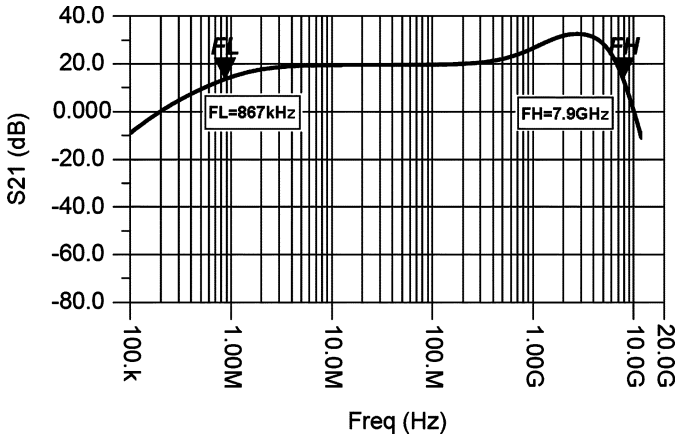

Fig. 13. Overall CML I/O structure simulated S21 plot.

D. Overall CML I/O Structure Simulation Result

The simulated output eye diagram and S21 plot of overall CML I/O structure is presented in Figs. 12 and 13, respectively. The bandwidth of CML I/O structure is 7.9 GHz and lower cutoff frequency is 867 KHz. The simulated eye diagram is very close to measurement result in Fig. 15 except the jitter is slightly larger than expectation. The simulation conditions are PRBS $2^{23}-1$ NRZ data, 8 mV ac-coupled input swing and ac-coupled driving external 50-Ω load.

To verify EQ performance with overall circuitry, a 15 cm FR4 traces is included into simulation environment prior to overall CML I/O structure (SMA connector and bonding wire effect are neglected) and the simulated result is shown in Fig. 14.

The inter symbol interference induced by FR4 PCB trace is removed after equalizer circuit block and obtains an adequate eye opening with 600 $\mathrm{mV_{pp}}$ output swing. The simulation conditions are PRBS $2^{23}-1$ NRZ data, dc-coupled 100 mV input swing, setting $\mathrm{Vtune}=0$ V at EQ stage and ac-coupled driving 50-Ω load directly.

IV. Experimental Result

For complete performance measurement, the CML I/O IC was tested by mounting on FR4 print circuit board and on-wafer probing. The test equipments include pattern generator (Anritsu MP-1763B) and digital communication analyzer (Agilent DCA 86100A).

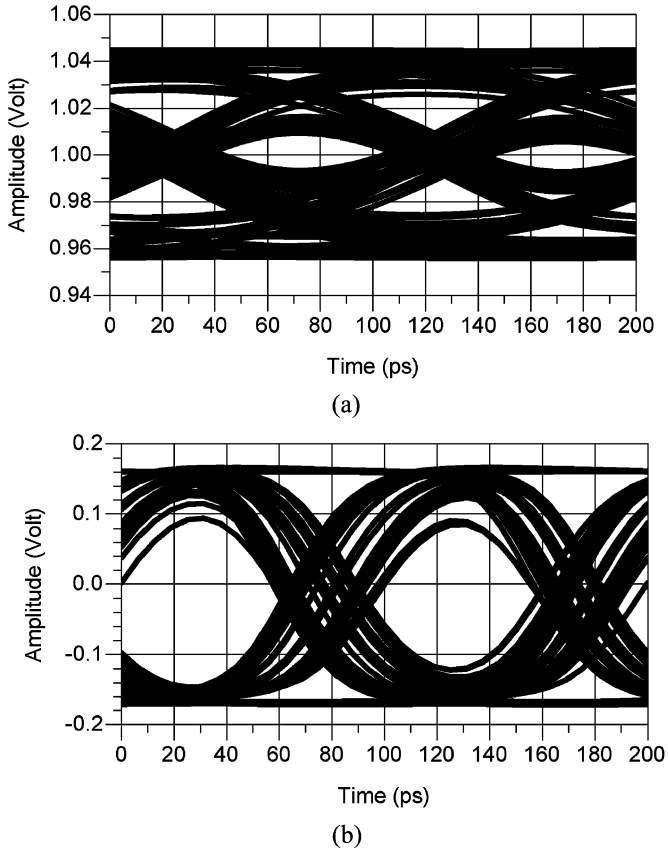

Fig. 14. Overall CML I/O structure simulated output diagram: (a) input data (after 15 cm FR4 PCB trace); (b) eye waveform after equalization (50-Ω output load).

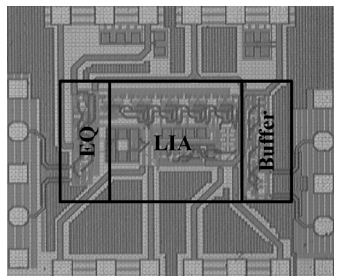

Fig. 15. Chip photo graph.

Fig. 15 illustrates the chip photo. Fabricated in a 1.8-V 0.18-μm 1P6M CMOS technology, the die area is 700 μm$\times$ 400 μm.

A. Test Result of Die Bonding Evaluation Board

Fig. 16 shows the FR4 evaluation board for die bonding.

This work was measured with different data rates from 2, 3, 4, to 5 Gb/s. The test conditions are PRBS $2^{23}-1$ NRZ data, 8 mV AC-coupled input swing and data output connects to 50-Ω load DCA electrical channel. The eye diagrams are shown in Fig. 17. The evaluation board measurement result revealed limitation of operation frequency due to the die wedge bonding, FR4 PCB material attenuation and proposed CML output buffer does not include pre-emphasis. The jitter of the output eye diagram at 5 Gb/s is up to 60 $\mathrm{ps_{pp}}$ and the output differential voltage swing is over 400 $\mathrm{mV_{pp}}$. On the other hand, the input overload also supports up to 1 V_{pp} to meet backplane data communication requirement [18].

TABLE I
PREFORMANCE BENCHMARK

	This work	[2]	[3]	[4]	[6]
Function	EQ+LA	LA	LA	LA	TIA+LA
DCC & AGC	Both	DCC	DCC	DCC	DCC (LA)
Inductor counts	0	24	10	8	6 (LA)
Process	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS
Supply voltage	1.8V	1.8V	2.4V	1.8V	1.8V
Power consumption	85mW	150mW	120mW	135mW	199mW
$Jitter_{pp}$	~25ps	~10ps	~30ps	N/A	~36ps
Bandwidth	7.9GHz	9.4GHz	6.5GHz	4GHz	7.8GHz
DC gain	40dB	50dB	30dB	32dB	40dB
Chip area	~0.28mm^2	~0.75 mm^2	~0.39mm^2	~0.5 mm^2	~0.8mm^2(LA)

Fig. 16. Photo of FR4 PCB evaluation board.

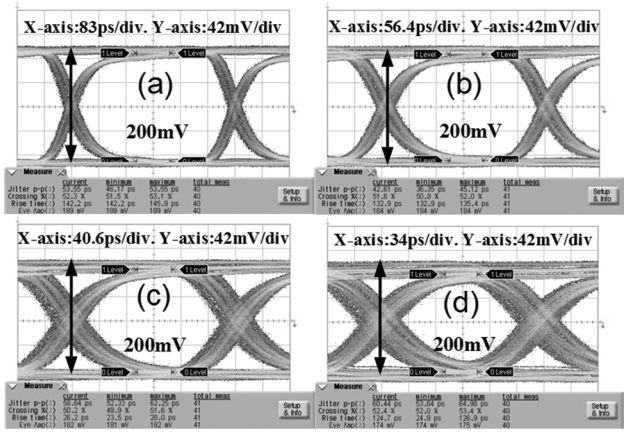

Fig. 17. FR4 PCB evaluation result: (a) 2 Gb/s; (b) 3 Gb/s; (c) 4 Gb/s; (d) 5 Gb/s.

B. On Wafer Test Result

At the same time, this circuit also tested by on-wafer probing method and the test conditions are the same as chip-on-board measurement. The test conditions are PRBS $2^{23}-1$ NRZ data, 8 mV AC-coupled input swing and data output connects to DCA scope directly. The Vtune of equalizer stage is 1.5 V under 10 Gb/s eye measurements for slightly compensating connector, cable loss.

The 8, 9, and 10 Gb/s eye diagrams are shown in Fig. 18, respectively. The performance is much better than printed circuit board because of the less parasitic effect and without FR4 material attenuation. The measured peak-to-peak jitter at 10 Gb/s

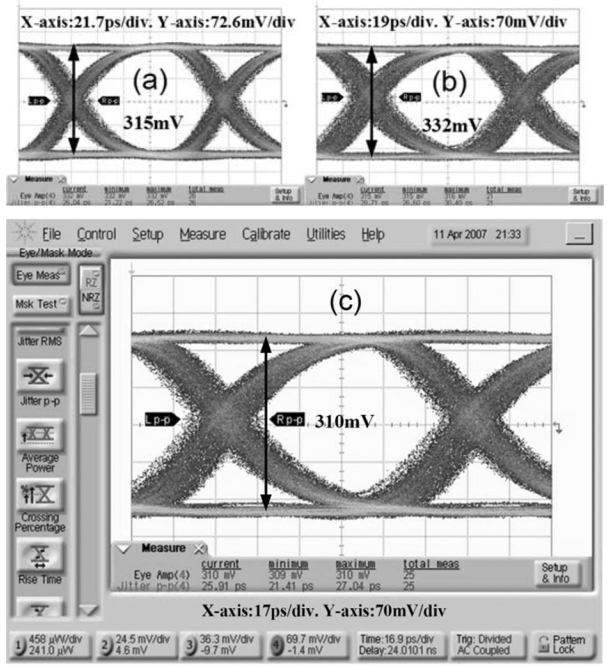

Fig. 18. On wafer test result: (a) 8 Gb/s; (b) 9 Gb/s; (c) 10 Gb/s.

is around 25 ps and output differential voltage swing can reach 600 m$V_{\rm pp}$ which verifies the circuit simulation result.

V. CONCLUSION

This paper describes a low power consumption and area efficient wide-band current-mode logic I/O interface for high speed backplane multi-channel interconnection in TSMC 0.18-μm 1P6M CMOS technology.

This CML I/O interface integrates the equalizer, limiting amplifier and output buffer. It can provide 40 dB voltage conversion gain, 40 dB input swing dynamic range and operation data rate up to 10 Gb/s. In this design, a modified Cherry–Hopper wide-band high-gain circuit architecture is applied to several circuit blocks and it is fully verified by chip level measurement result. The proposed design is suitable for SOC design because of its: 1) small chip area includes EQ/LIA; 2) low power consumption; 3) LIA circuit block contains AGC/DCC functionality; 4) high-speed CML buffer includes active inductive load along with active feedback structure.

Table I summarizes the circuit performance and compare with other recently published works. It shows that proposed design can save 30–65% of die area, consume less than 30%–40% power including both dc-offset cancelling function and AGC function. Equalizer and CML output buffer circuit blocks are also included. Based on previous advantages, this design is specially optimized for high speed backplane multi-channels data communications.

ACKNOWLEDGMENT

The authors would like to thank Taiwan Semiconductor Manufacturing Company (TSMC) and National Chip Implementation Center (CIC) for their comments and fabrication support.

REFERENCES

[1] Altera Corp., San Jose, CA, "The evolution of high-speed transceiver technology," Nov. 2002.

[2] S. Galal and B. Razavi, "10 Gb/s limiting amplifier and laser/modulator driver in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2138–2146, Dec. 2003.

[3] R. Tao and M. Berroth, "10 Gb/s limiting amplifier for optical links," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Sep. 2003, pp. 285–287.

[4] P. Muller and Y. Leblebici, "Limiting amplifier for next-generation multi-channel optical I/O interface in SoC," in *Proc. IEEE SoC Conf.*, Sep. 2005, pp. 193–196.

[5] W. Z. Chen, Y. L. Cheng, and D. S. Lin, "A 1.8 V, 10 Gbps fully integrated CMOS optical receiver analog front end," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1388–1396, Jun. 2005.

[6] W. Z. Chen and C. H. Lu, "A 90-dBO 10-Gb/s optical receiver analog front-end in a 0.18-μm CMOS technology," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 3, pp. 358–365, Mar. 2007.

[7] C. S. Chang, D. S. Lee, and Y. S. Jou, "Load balanced Birkhoff-von Neumann switches, part I: One-stage buffering," *Comput. Commun.*, vol. 25, pp. 611–622, 2002.

[8] C. S. Chang, D. S. Lee, and C. M. Lien, "Load balanced Birkhoff-von Neumann switch, part II: Multi-stage buffering," *Comput. Commun.*, vol. 25, pp. 623–634, 2002.

[9] C. S. Chang, D. S. Lee, and C. Y. Yue, "Providing guaranteed rate services in the load balanced Birkhoff-von Neumann switches," in *Proc. IEEE INFOCOM*, San Francisco, CA, 2003, pp. 1622–1632.

[10] C. S. Chang, D. S. Lee, and Y. J. Shih, "Mailbox switch: A scalable two-stage switch architecture for conflict resolution of ordered packets," in *Proc. IEEE INFOCOM*, Hong Kong, 2004, pp. 1995–2006.

[11] E. M. Cherry and D. E. Hooper, "The design of wide-band transistor feedback amplifier," *Proc. Inst. Elec. Eng.*, vol. 110, no. 2, pp. 375–389, Feb. 1963.

[12] H. Tamura, M. Kibune, H. Yamaguchi, K. Kanda, K. Gotoh, and J. Ogawa, "Circuits for CMOS high-speed I/O in sub-100 nm technologies," *IEICE Trans. Electron.*, vol. E89-C, no. 3, pp. 300–313, Mar. 2006.

[13] Y. Tomita, M. Kibune, J. Ogawa, and W. W. Walker, "A 10 Gb/s receiver with equalizer and on-chip ISI monitor in 11 μm CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2004, pp. 202–205.

[14] E. A. Crainl and M. H. Perrott, "A 3.125 Gb/s limit amplifier in CMOS with 42 dB gain and 1 us offset compensation," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 443–451, Feb. 2006.

[15] M. I. Elmasry and P. M. Thompson, "Analysis of load structures for current-mode logic," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 2, pp. 72–75, Feb. 1975.

[16] R. L. Treadway, "DC analysis of current mode logic," *IEEE Circuits Devices Mag.*, vol. 5, no. 2, pp. 21–35, Mar. 1989.

[17] Payam and Heydari, "Design issues in low-voltage high-speed current-mode logic buffers," in *Proc. ACM Great Lakes Symp. VLSI*, Apr. 2003, pp. 28–29.

[18] N. Krishnapura, M. B. Pour, Q. Chaudhry, J. Khoury, and A. Aggarwal, "A 5 Gb/s NRZ transceiver with adaptive equalization for backplane transmission," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2005, pp. 60–62.

Min-Sheng Kao received the B.S. degree in electrical engineering from National Taiwan Ocean University, Taiwan, R.O.C., in 1997, the M.S. degree in electrical engineering from National Taiwan University of Science and Technology, Taiwan, R.O.C., in 1999. He is currently pursuing the Ph.D. degree in communications engineering from National Tsing Hua University.

He joined Industrial Technology Research Institute (ITRI) optical communication and optical display division from 2000 to 2004. He is currently a staff marketing and product application engineer with Mindspeed Technologies. He holds 7 U.S. patents. His research interests include high-speed analog and RF circuit design.

Jen-Ming Wu (S'88–M'98) received the B.S. degree from National Taiwan University, Taipei, Taiwan, in 1988, and the Ph.D. degree from University of Southern California, Los Angeles, CA, in 1998, all in electrical engineering.

From 1998–2003, he has been with Sun Microsystems, Inc. in Silicon Valley as a Senior Member of technical staff. Since 2003, he has been with the Institute of Communications Engineering, Department of Electrical Engineering, National Tsing Hua University as an Assistant Professor. He has worked on various fields of electrical engineering including high speed chip-to-chip interconnections, I/O interface for optical transceivers, digital signal processing, wireless communication transceiver design, and microprocessor architecture. Currently, his research works focus on high speed interconnections, wireless baseband communication technologies, embedded SoC design for multimedia communications.

Chih-Hsing Lin was born in I-Lan, Taiwan, R.O.C., in 1977. He received the B.S. degree in electric engineering from Ming-Hsin of Science and Technology University, Hsin Chu, Taiwan, R.O.C., in 2000, and the M.S. degree in electric engineering from Chung Yuan Christian University, Chung Li, Taiwan, R.O.C., in 2002. He is currently pursuing the Ph.D. degree in communication engineering from the National Tsing Hua University, Hsin Chu, Taiwan, R.O.C.

His research interests include delay-locked loops, frequency synthesizers, and low power design.

Fanta Chen was born in Hsin Chu, Taiwan, R.O.C., in 1983. He received the B.S. degree from Yuan Ze University, Taiwan, R.O.C., in 2005 and the M.S. degree from the National Tsing Hua University, Hsin Chu, Taiwan, R.O.C., in 2007, where he is currently pursuing the Ph.D. degree in communication engineering.

His research interests include phased locked loops and clock and data recovery for high speed switch fabric design.

Ching-Te Chiu received the B.S. and M.S. degree from National Taiwan University, Taipei, Taiwan, in 1986 and 1988, respectively, and the Ph.D. degree from University of Maryland, College Park, in 1992, all in electrical engineering.

She was an Associate Professor with National Chung Cheng University, Chia-Yi, Taiwan, from 1993 to 1994. From 1994 to 1996, she was a member of the technical staff with AT&T, Murray Hill, NJ, and Lucent Technologies, Murray Hill, NJ, from 1996 to 2000, and with Agere Systems, Santa Clara, CA, from 2000 to 2003. Since 2004, she has joined the Computer Science Department, National Tsing Hua University, Hsinchu, Taiwan. Her research interests include video and communication integrated circuit design. She has been working on High Dynamic Range tone mapping processor chip design, high speed switch fabric IC design and SERDES interface design. Her previous chip designs include high definition television video decoder, the standard television demodulation, the SONET/SDH mapper and framer, the ATM core/edge switch, 10 Gb/s I/P router traffic management, and FEC decoder.

Shawn S. H. Hsu (M'04) was born in Tainan, Taiwan, R.O.C. He received the B.S. degree in electrical engineering from National Tsing Hua University, Taiwan, R.O.C., in 1992, the M.S. degree in electrical engineering and computer science, and the Ph.D. degree from The University of Michigan, Ann Arbor, in 1997 and 2003, respectively.

From 1992 to 1994, he served as a Lieutenant with the R.O.C. Army. From 1994 to 1995, he was a Research Assistant with National Chiao Tung University, Taiwan, R.O.C. In 1997, he joined the III–V Integrated Devices and Circuits Group, The University of Michigan at Ann Arbor. He is currently an Associate Professor with the Department of Electrical Engineering, National Tsing Hua University. His current research interests include the analytical and empirical large-signal and noise modeling of Si/III–V-based devices for RFIC/MMIC design applications, and the implementation and development of various measurement techniques to extract parameters for equivalent circuit models. He is also involved with the design of MMICs and RFICs using Si/III–V-based devices for low-noise, high-linearity, and high-efficiency system-on-chip (SOC) applications.