A Miniature 300-MHz Resonant DC–DC Converter With GaN and CMOS Integrated in IPD Technology

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***Abstract*—A 300-MHz class-E dc–dc converter using the resonant gate driving technique is proposed. The gate driver utilizes the harmonic shaping network and *RC* feedback to enhance the output swing voltage, and the class-E power converter can minimize the voltage–current overlap to improve efficiency. With the 0.25-μm GaN high-electron-mobility transistor and 0.18-μm CMOS for the switching power device and the gate driver, respectively, a complete dc–dc converter operating at 300 MHz is demonstrated including all the passive components microfabricated by integrated passive device (IPD) technology on the high-resistivity silicon substrate. The overall chip area is smaller than 1 cm $\times$ 1 cm and the volume is only 0.115 cm^3. The measured results show a maximum output power of 4.16 W with 47.3% efficiency. An excellent power density of 36.2 W/cm^3 can be achieved. The flip-chip assembled converter on the IPD substrate demonstrates the potential of heterogeneous integration for high-frequency power conversion applications.**

***Index Terms*—Class E, CMOS, GaN high-electron-mobility transistor (HEMT), high frequency, power converter, power supply-in-package (PSiP), resonant power converter.**

I. Introduction

IN RECENT years, the research and development of power converters at high switching frequencies [1]–[19] has attracted significant attention from both academia and industry. Power converters with a small size and high power density are favorable for modern electronic products, especially for the portable applications [1], [5], [13], [15]. Also, the miniaturized power converter is critical to the next-generation technology such as insect-sized microrobots that can provide surveillance and reconnaissance in hostile or other hard-to-reach environments [2]. In many cases, the size and weight of a power converter are determined by the passive components, which are the essential parts of the system. To achieve a converter with a compact size, smaller passive components are favorable, which usually means higher operating frequencies. In addition to the size reduction, power converters with a high switching frequency are required for the advanced modulation schemes necessary to achieve high power-added-efficiency such as envelope tracking and envelope elimination and restoration (EER) transmitter systems [1], [13]. Different approaches and techniques have been proposed for high switching frequency power converters with reduced sizes. For example, a copper air-core microinductor with a 30-μm thick electroplated copper [2] and the packaging inductors including bond wires and lead frames were utilized [7] to enhance circuit performance by the inductor with a high quality factor. The idea of a self-oscillating gate driver was reported to achieve soft gating with improved efficiency compared with hard switching [3], [4], [9], and the resonant gate driver can reduce the gate losses at high switching frequencies [11], [17]–[19]. Also, some previous publications emphasized using the standard CMOS process for fully integrated power converters [8], [17], whereas some reported works employed the GaAs Pseudomorphic High-Electron -Mobility Transistor (pHEMT) [15], [16] or GaN HEMT technology [9] to take advantage of low on-resistance and high switching speed of the transistors for high-efficiency power conversion. The concept of system-in-package (SiP) was also incorporated to achieve a compact circuit size by stacking the chips [6], [16].

There are some obstacles to be overcome in order to achieve high-frequency operation while maintaining a good efficiency in power conversion systems, including increased switching loss and driver power consumption, limitation of the switching frequency by the nature of power devices, realization of high-Q passive components, and parasitic effects due to package and circuit layout. Many efforts have been made to reduce the power consumption of switching and the gate driver with an increased operating speed of power converters. One approach to minimize the switching loss is referred to as "zero-voltage switching" (ZVS) [3], [4], [10]–[14], [20], which can be attained by class-E or some other resonant converter topologies. Compared with hard switching power converters, the ZVS design can mitigate the overlap of voltage and current waveforms in the power device to minimize the switching loss. Another challenge is the considerable power consumption of the driving circuit due to the large input capacitance of power devices at high-frequency switching. Resonant gate drive techniques have been proposed to reduce the power consumption of the driving circuits [17]–[19], [21]–[24]. The basic concept of using the interaction of a capacitor with a series-connected inductor and a switching element for resonant gate drive was illustrated in [22]. The resonant gate driver allows energy recovery using the inductive components, and an enhanced efficiency is expected [24]. A combined low-side and high-side resonant-type gate driver with partially shared inductor was proposed in [17]. The resonant gate driver was also employed in the low-side switch for a 100-MHz

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GaAs dc–dc converter to reduce the loss under light load conditions, and a 5% efficiency improvement can be achieved [18]. A 200-MHz fully integrated dc–dc converter with a resonant gate driver using an on-chip air-core inductor was realized in 0.25-μm BiCMOS technology [19]. A multistage gate driver was proposed in [23], which employed a hard-switched inverter as the first stage, and the resonant second-harmonic class E inverter was used as the following stage to drive the power device.

The switching frequency is also limited by the power devices, where tradeoffs exist among the on-resistance, breakdown voltage, and switching speed. Power devices based on relatively new wide bandgap semiconductors such as SiC and GaN have been proposed in recent years to take advantage of superior material properties [25]–[31]. The performance of wide bandgap power devices was improved by different approaches such as the hybrid drain structure [25], [27], ohmic/Schottky contact engineering [26], [30], and square gate geometry [28]. The advantages of using SiC-based devices for high-power and high-frequency applications were discussed [31]. In addition, the loss of inductive components becomes a serious issue as the operating frequency increases due to the eddy current and hysteresis loss [2]. Different approaches were reported to improve the high-frequency performance of magnetic materials for inductors and transformers [32]–[40]. Multiple layers of magnetic materials such as Co–Zr–O [32], [40], permalloy ($Ni_{80}Fe_{20}$) [34], and FeCoB [39] were employed to increase the flux density. The distributed air-gap structure was proposed using low-temperature cofired ceramic technology to achieve a very compact inductor [38]. The loss characteristics of RF magnetic materials for power conversion applications were investigated in details [33], and the challenges and considerations of integrating magnetics for on-chip power supply were discussed and reviewed [35], [37].

One effective solution for achieving a compact power converter with high operating frequencies is to increase the integration level of the system, which means using more microfabricated elements with an advanced semiconductor process to replace the discrete components for system integration and circuit size reduction. However, most of the high-frequency power converters reported to date are still realized at the board level using discrete active and passive components with relatively large sizes [3]–[5], [10]–[14]. In this work, a class-E dc–dc converter with a resonant gate driver is proposed. With integrated passive devices (IPDs) technology on a high-resistivity silicon substrate, a complete power converter is heterogeneously flip-chip integrated, including the resonant gate driver in standard 0.18-μm CMOS, the power device in 0.25-μm GaN HEMT technology, and the planar inductors and metal–insulator–metal (MIM) capacitors microfabricated directly on the IPD substrate, as illustrated in Fig. 1. The overall chip area of the converter is smaller than 1 cm $\times$ 1 cm with a volume of only $\sim$0.1157 cm^3.

The focus of this work is to demonstrate a high-frequency power converter with the novel SiP technology together with CMOS and GaN devices. The goal is to achieve high power density with more design and integration flexibility. We present the results in a relatively wide input voltage range from 4 to 12 V, which could potentially be used for applications such as lithium battery of about 4 V [2], and the boost converters of a 12-V car battery input and a 20-V output [9]. Also, the converter can supply LEDs used for LCD backlight [3]. Moreover, the proposed power converter can be possibly employed to drive the low-power dc motor [41]. This paper is organized as follows. Section II introduces the principle of class-E circuit topology and analysis of the ZVS class-E power converter. Section III presents the detailed design of the proposed dc–dc converter with different technologies employed. Section IV presents the experimental results and discussion, and Section V concludes this work.

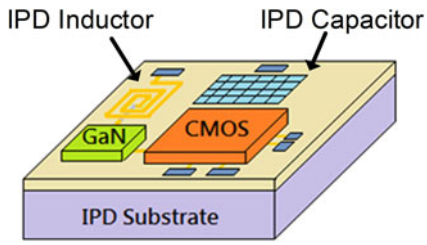

Fig. 1. Conceptual plot of the proposed class-E power converter using both GaN and CMOS devices/circuits integrated in the IPD technology.

II. Class-E Circuit Topology

Both the hard switching and resonant topologies are theoretically capable of achieving 100% efficiency for power converters. Compared with the hard switching design, the main advantage of resonant converters is the reduced switching loss for high-frequency operation by achieving ZVS or "zero-current switching (ZCS)" conditions [42]. In addition, the resonant topology provides an effective approach to resolve the issues caused by the parasitics for high-frequency power conversion. The parasitic effects such as the output capacitance of the switching transistor and the stray inductances and parasitic capacitances introduced from the circuit layout and package can degrade the circuit performance, which becomes more severe at high frequencies in the conventional hard switching power converters. In contrast, the resonant-type designs can absorb the parasitics as a part of the circuit for achieving the ZVS/ZCS condition [3], [4], [10]–[14]. In this study, we focus on the resonant-type class-E power converter operating in the UHF range.

A. Operating Principle of Class-E Topology

Operation of the power converter at high frequencies introduces a significant switching loss, which makes the circuit topology critical for improving the conversion efficiency. One of the ZVS techniques employed is the class-E topology, first introduced by Sokal and Sokal in 1975 [43], [44] for RF power amplifiers. Fig. 2(a) shows the circuit topology of a typical class-E amplifier, where the transistor S_1 acts as a switch, L_1 functions as an RF choke, and C_2 and part of L_2 form a series resonator (open circuit at the harmonics) to transfer power to the load at the fundamental frequency. Part of L_2 and the shunt capacitor C_1 function together to achieve the ZVS condition of the class-E power amplifier [45]. Although different configurations can also achieve the ZVS condition for power converters and switching amplifiers [20], [46]–[48], the class-E topology possesses some distinct advantages owing to its load network design. First, the

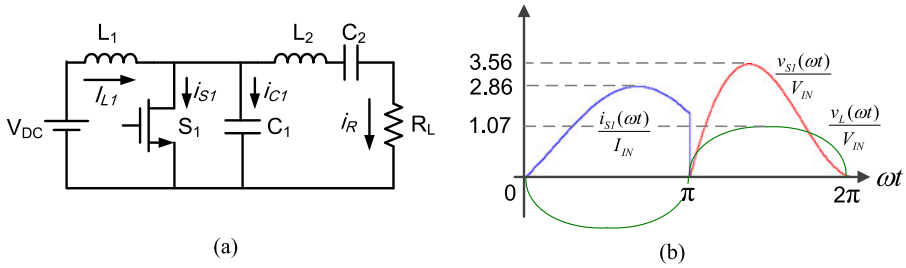

Fig. 2. (a) Class-E circuit topology, and (b) current and voltage waveforms.

transient response of the load network (C_1, L_2, C_2, and R_L; L_1 is sufficiently large acting as a constant current source) allows a delay of voltage increase at switch turn OFF, which makes sure that high voltage does not exist across the switch as the current flowing through it is nonzero [43]. In addition, the class-E topology can reach an approximate zero voltage slope ($dv/dt \approx 0$) at switch ON with a properly designed load network, which permits a time interval during turn ON to still meet the condition of $v = 0$. The conditions of both zero voltage and zero voltage slopes together also imply that the switch current starts from zero gradually. As a result, the moderate turn ON of switch can effectively reduce the power dissipation during transistor turn ON. This also allows slightly mistuning of the circuit without severe loss of efficiency [43]. More detailed analysis of the class-E topology is described as follows based on the assumptions of ideal switching characteristics [47]. Also, the choke inductor is large enough so that the input current is a pure dc current, and the loaded quality factor of the resonant tank is very high to ensure pure sinusoidal current.

Assume the current of load i_R is

$$i_R(\omega t) = I_R \sin(\omega t + \phi) \tag{1}$$

where I_R is the amplitude and ϕ is the initial phase. The currents in the ideal switching transistor S_1 and the shunt capacitor C_1 for each half-cycle (assuming 50% duty cycle) can be expressed as (2) and (3), respectively. Assume that S_1 is ON during the first half-cycle ($i_{C1} = 0$) and OFF in the second half-cycle ($i_{S1} = 0$)

$$i_{S1}(\omega t) = I_{L1} - I_R \sin(\omega t + \phi) \quad 0 < \omega t \le \pi \tag{2}$$

$$i_{C1}(\omega t) = I_{L1} - I_R \sin(\omega t + \phi) \quad \pi < \omega t \le 2\pi \tag{3}$$

where $I_{L1} = I_{\rm IN}$ is the total current at the input. As a result, the voltage v_{S1} across C_1 can be obtained from

$$v_{S1}(\omega t) = \frac{1}{\omega C_1}\int_{\pi}^{2\pi} i_{C1}(\omega t)d(\omega t) = \begin{cases} 0 & 0 < \omega t \le \pi \\ \frac{1}{\omega t}\left[I_L(\omega t - \pi) + I_R(\cos(\omega t + \phi) - \cos(\pi + \phi)\right] & \pi < \omega t \le 2\pi \end{cases}. \tag{4}$$

To achieve the goals of ZVS and zero derivative switching (ZDS), the conditions $V_{\rm SI}(\omega t)|_{\omega t = 2\pi} = 0$ and $\frac{\partial v_{\rm SI}(\omega t)}{\partial(\omega t)}|_{\omega t = 2\pi} = 0$ must both be satisfied. These two requirements at the end of the OFF state indicate that the switch current at the beginning of the ON state will be zero, and also the current only increases gradually from zero. This feature is desirable to reduce the power dissipation during the turn ON transient [43]. Based on these constrains, we can obtain the following equations:

$$I_R = I_{L1}\frac{\pi}{\cos(\pi + \phi) - \cos(\phi)} \tag{5}$$

$$i_{S1}(\omega t) = I_{L1}\left[1 - \frac{\pi \sin(\omega t + \phi)}{\cos(\pi + \phi) - \cos\phi}\right] \quad 0 < \omega t \le \pi \tag{6}$$

$$i_{C1}(\omega t) = I_{L1}\left[1 - \frac{\pi \sin(\omega t + \phi)}{\cos(\pi + \phi) - \cos\phi}\right] \quad \pi < \omega t \le 2\pi \tag{7}$$

where $\phi = \tan^{-1}(\frac{-2}{\pi})$. The dependence of input voltage $V_{\rm dc} = V_{\rm IN}$ on the voltage across S_1 can be obtained by

$$V_{\rm IN} = \frac{1}{2\pi}\int_0^{2\pi} v_{S1}(\omega t)d(\omega t). \tag{8}$$

As a result, the voltage and current of the switching transistor S_1 in each half-cycle can be obtained as

$$i_{S1}(\omega t) = I_{\rm IN}\left[\frac{\pi}{2}\sin(\omega t) - \cos(\omega t) + 1\right] \quad 0 < \omega t \le \pi \tag{9}$$

$$v_{S1}(\omega t) = V_{\rm IN}\left\{\pi\left[\omega t - \frac{3}{2}\pi - \frac{\pi}{2}\cos(\omega t) - \sin(\omega t)\right]\right\} \quad \pi < \omega t \le 2\pi. \tag{10}$$

The amplitude of voltage across the load can be calculated from $v_{S1}(\omega t)$ as

$$V_L = -\frac{4\sin\left(\frac{\pi}{2} + \phi\right)}{\pi}. \tag{11}$$

Also, the inductor L_2 can be divided into two serially connected elements of L_A and L_B, where L_A and C_2 can be tuned to resonate at the fundamental frequency, while the values of L_B and C_1 for achieving ZVS and ZDS conditions can be obtained by the derived I_R, $V_{\rm IN}$, and the voltage across R_L as

$$C_1 = \frac{8}{\pi(\pi^2 + 4)\omega R_L} \tag{12}$$

$$L_B = \frac{\pi(\pi^2 - 4)}{16}\cdot\frac{R_L}{\omega}. \tag{13}$$

Fig. 2(b) plots the corresponding voltage and current waveforms based on (9) and (10), which shows nonoverlapping characteristics of current and voltage with no dc power consumption.

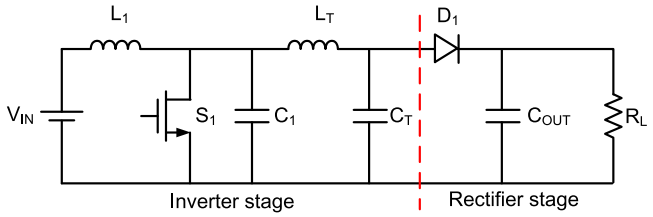

Fig. 3. Class-E dc–dc power converter including the inverter stage and the rectifier stage.

The peak values of i_{S1} is $2.86\times$ of $I_{\rm IN}$, and that of v_{S1} is $3.56\times$ of $V_{\rm IN}$. The output voltage across the load is also shown in the figure. The analysis indicates that the class-E topology can achieve the ZVS/ZDS condition with the ideal switching transistor and passive components. Based on the similar concept of creating nonoverlapping current and voltage across the switch, this topology is suitable for power converts to achieve high efficiency at high frequencies.

B. Class-E DC–DC Converter

Fig. 3 shows the design of a dc–dc power converter using class-E topology, which can be analyzed in two stages, the inverter stage and the rectifier stage. The inverter stage is composed of L_1, S_1, C_1, L_T, and C_T, and the rectifier stage includes D_1 with $C_{\rm OUT}$. The inverter stage of the class-E power converter is based on the aforementioned class-E RF power amplifier. The main difference is that the series capacitor C_2 is replaced by the shunt capacitor C_T, which allows the dc current of the power converter to pass while still resonating at the fundamental frequency. This design can also be considered as combining the input tank of the rectifier stage with the output resonant tank of the inverter stage [10], which can simplify the circuit and effectively reduce the size. In practical design, the initial value of L_T is chosen to be similar to L_2, and then optimized together with C_T for the ZVS condition of a maximum efficiency. Note that the current and waveform equations for the proposed class-E dc–dc converter are similar to those of the class-E amplifier at the reference plane before the rectifier stage (see the red dashed line in Fig. 3). The only difference is the additional dc level due to the modified shunt capacitor (C_2 becomes C_T). Detailed analysis about the impact of the rectifier stage on the output waveform can be found in the previous publication [14] for a high-frequency resonant boost converter with a similar topology to the proposed design. The analysis was conducted by replacing the inverter stage with a sinusoidal voltage source with a dc offset. It should be mentioned that if the diode and capacitor are ideal in the rectifier stage, the efficiency will not be degraded, which can be verified by simulation. In practice, the efficiency will drop mainly due to the loss introduced by the nonideal characteristics of the diode such as parasitic resistance and nonzero turn ON voltage.

The transfer function of the parallel resonant converter was analyzed [42]. Assume that both the switching network and rectifier stage are ideal, the transfer function of the parallel resonant tank $L_T - C_T$ and the voltage transfer ratio from $V_{\rm IN}$ to output voltage V_L can be expressed as follows (R_e is the effective resistive load looking into the rectifier stage, f_0 is the resonant frequency of $L_T - C_T$, and f_S is the operating frequency)

$$H(s) = \frac{Z_0(s)}{sL_T} \quad \text{where } Z_0(s) = sL_T \| \frac{1}{sC_T} \| R_e \tag{14}$$

$$\frac{V_L}{V_{\rm IN}} = \frac{8}{\pi^2} \frac{1}{\sqrt{(1-F^2)^2 + \left(\frac{F}{Q_e}\right)^2}} \tag{15}$$

where $F = f_S/f_0$, $f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{L_T C_T}}$, and $Q_e = R_0/R_e$ with $R_0 = \omega_0 L_T = 1/\omega_0 C_T$.

At resonance, the conversion ratio can be obtained as R_L/R_0. As mentioned, one advantage of the resonant-type converter should be emphasized is that parasitic elements in the circuit could be utilized as a part of the circuit to prevent performance degradation at high switching frequencies if properly designed. With the required LC components for resonance in the class-E power converter, the parasitics can be codesigned into the circuit to achieve the desired frequency response with suppressed harmonics and improved efficiency. On the other hand, one disadvantage of the resonant-type converter is that the ZVS condition can only be maintained at the resonant frequency. As indicated in (12) and (13), the values of passive devices are a function of the operating frequency, which should be designed properly to achieve the ZVS condition. The efficiency degrades when the operating frequency deviates from f_0 due to the increased switching loss. In a practical design, C_1 is obtained by incorporating the effective output capacitance of S_1, and the optimization of C_T is combined with the parasitic capacitances looking into the rectifier stage. The design of L_T and C_T should be such that the higher order harmonics are suppressed and the ZVS condition is achieved. The interconnects in the IPD layout are also considered by rigorous EM simulation to be codesigned with the IPD inductors of L_1 and L_T. More details will be discussed together with the IPD layout in Section III.

III. Proposed Class-E DC–DC Power Converter

Fig. 4 shows the complete circuit topology of the proposed class-E dc–dc power converter, including the resonant gate driver in 0.18-μm CMOS, the power transistor and diode in 0.25-μm GaN HEMT, and the passive components in IPD technology on the high-resistivity silicon substrate.

A. Resonant Gate Driver

The design of a gate driver capable of high-frequency operation while maintaining a high efficiency is critical to achieving a high-performance power converter. The conventional gate driver is usually realized by cascading inverters to provide sufficient driving capability. However, the power consumption increases significantly with the operating frequency. Also, a large supply voltage is often needed to achieve a high output swing. Differing from the conventional inverter-type gate drivers, the resonant gate drivers use the LC components to assist charging and discharging the large input parasitic capacitance of power devices more efficiently. The LC resonance techniques were reported to

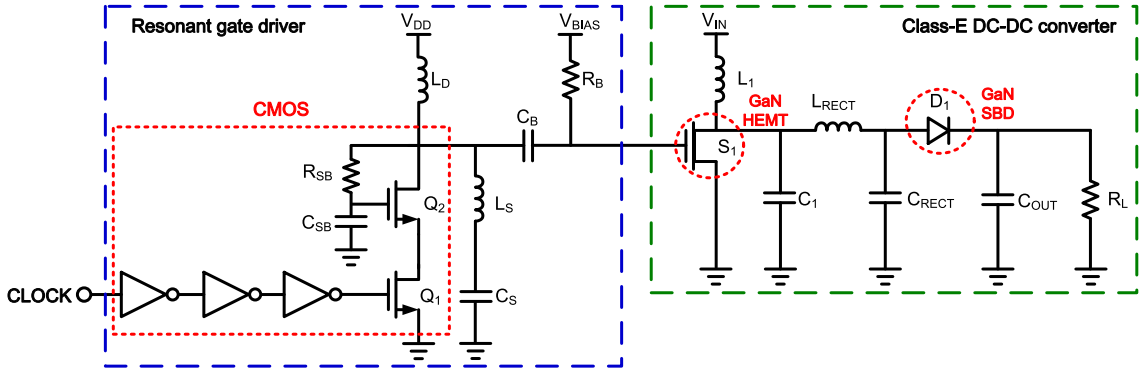

Fig. 4. Proposed 300-MHz dc–dc power converter with the resonant gate driver in standard 0.18-μm CMOS, and the class-E inverter stage with 0.25-μm GaN HEMT as the switch transistor. The whole circuit is integrated by the IPD technology in a high resistivity silicon substrate including all the passive components.

reduce the driving loss [17]–[19], [21]–[24]. A high-frequency resonant-type gate driver was demonstrated at 200 MHz [19]. However, most of the published results were designed and operated at relatively low frequencies (below 10 MHz).

In this work, a resonant gate driver is proposed based on the topology of class E/F switching-mode power amplifiers and class Φ_2 inverters [4], [48]–[51], where the series-connected L_S and C_S resonate at around the second harmonic frequency (short circuited to ground), and together with L_D to enhance the fundamental and third harmonic signals. Note that the dc block C_B is relatively large and has negligible impact at the frequency of interest. Similar to the principle in other resonant gate drivers [10], [24], the inductive energy-storage elements help to charge and discharge the input capacitance $C_{\rm IN}$ of the switching transistor to improve the efficiency. Also, L_D serves as an inductive load similar to a typical RF amplifier [52], which allows using a low supply voltage to achieve a large output swing. Moreover, the low-order harmonic shaping network in the class Φ_2 topology results in a trapezoidal waveform (see Fig. 7) [10], which is preferred for driving the class-E configuration [44]. The proposed resonant gate driver is composed of a three-stage predriver using CMOS inverters, and a main driving stage consisting of a self-biased *RC* feedback cascode configuration. It should be emphasized that GaN technology is also a good choice for realizing the gate driver, which can be integrated with the switching transistor directly to minimize the parasitic effects at high frequencies with an excellent driving capability [9]. However, the cost of GaN technology is a major concern. Also, the CMOS technology provides more freedom to combine the control circuits directly with the gate driver. As shown in Fig. 5(a), the conventional cascode topology is often adopted to prevent device breakdown [53]. With $V_{\rm DD}$ distributed to both transistors (Q_1 and Q_2), a large output swing can be achieved even with the submicron CMOS devices. However, the fixed gate voltage V_{G2} of Q_2 can still result in a considerable drain–gate voltage V_{DG2}, which stresses the transistor under large output swing and can raise the breakdown and reliability issues. With the proposed feedback path formed by $R_{\rm SB}$ and $C_{\rm SB}$, V_{G2} can vary with the output voltage, which effectively reduces the drain–gate voltage crossing on Q_2 to prevent transistor breakdown. Fig. 5(b) compares the simulated voltages of the two designs at different nodes. As can be seen, the drain–gate voltage of Q_2 is reduced

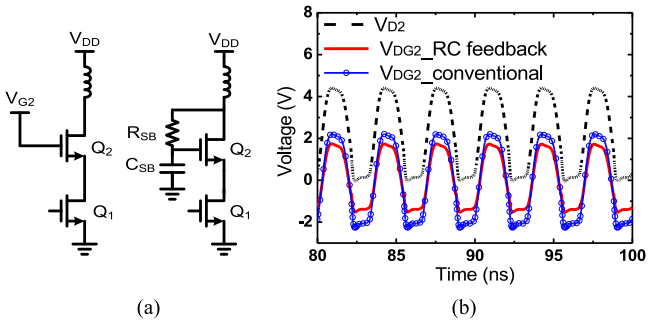

Fig. 5. (a) Comparison of the conventional and proposed *RC*-feedback self-biased cascode configuration, and (b) simulated characteristics of the circuits.

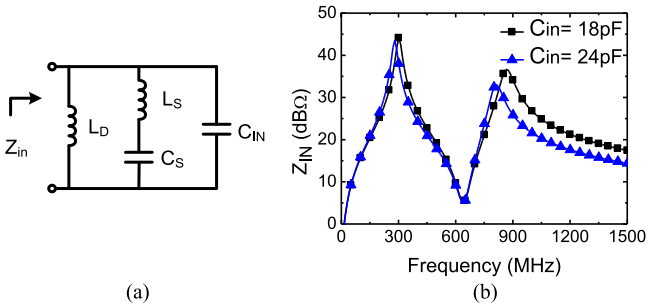

Fig. 6. (a) Harmonic shaping network at the output of gate driver, and (b) simulated impedance of the harmonic shaping network.

effectively with the *RC* feedback. Note that the 0.18-μm CMOS transistors used for the last stage (cascode with *RC* feedback) are the I/O devices in the standard process, and the operating voltage should not exceed 3.3 V as suggested by the foundry (common-source configuration). As shown in this figure, the voltage swing V_{D2} across the cascode transistors exceeds 4 V, while the most critical drain–gate voltage of Q_2 is kept below 2 V during operation. The circuit can be operated with sufficient reliability without the concern of device breakdown and degradation.

Fig. 6(a) shows the equivalent circuit of a multiresonant tank in the gate driver for harmonic shaping, formed by L_D of 8.5 nH, L_S of 5.5 nH, and C_S of 11 pF at 300 MHz, and the effective input capacitance $C_{\rm IN}$ of the power device. Fig. 6(b) shows the simulated result of input impedance $Z_{\rm IN}$ of the tank under two

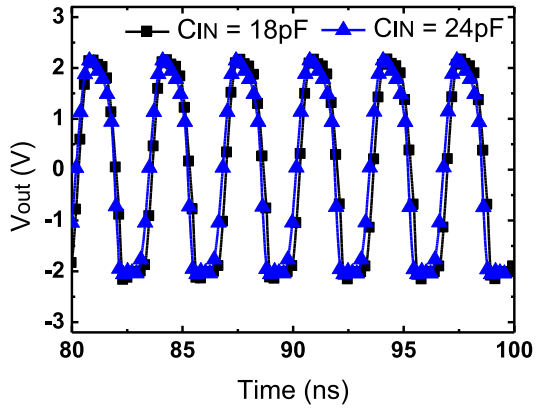

Fig. 7. Simulated output waveform of the proposed gate driver.

different loading conditions of 18 and 24 pF, corresponding to the actual range of $C_{\rm IN}$ in our design as can be estimated from the transistor model. As can be seen, very high impedance can be obtained at the fundamental tone of 300 MHz with a peak at the third harmonic around 900 MHz. With the techniques of inductive peaking and a multiresonant harmonic shaping network, a large trapezoidal output signal swing and a reduced gate driving loss can be obtained without the complicated control mechanism, as shown in Fig. 7. The total power consumption of the proposed resonant gate driver is 196 mW with $V_{\rm DD}$ of 2.2 V, which can provide an output voltage swing up to 4.2 V. Simulation was performed to compare the proposed design with the conventional inverter-type driver. Under the same loading condition of GaN switch and operating frequency of 300 MHz, the proposed design can achieve 4.2 V swing with a power consumption of 150 mW, while the inverter chain driver consumes 186 mW with an output swing of 3.3 V. The results indicate that the resonant-type gate driver exhibits a higher power efficiency as expected. In addition, assume that the gate capacitance of the switching device is 24 pF, the power needed to drive the capacitive load with a 4.2-V swing can be estimated by $P_{\rm diss} = C \cdot V^2 \cdot f$, which is ~127 mW in an ideal case. Considering the nonideal effects in both the active and passive components in the circuit, the efficiency of the driving stage is acceptable.

As mentioned, the output swing in the typical inverter gate driver could be limited by the breakdown voltage with a standard submicron CMOS process, which can be solved by the proposed topology. It is also possible to use a high-voltage CMOS process to realize the driver for improved output swing, but the cost, operating speed, and integration level with other control circuits are the main issues. One disadvantage in practical design is that the proposed resonant gate driver requires a larger area because of the inductive components. However, the IPD process offers a relatively low-cost design with high Q inductor and more design flexibility. Also, the resonant-type design of the output stage can absorb the parasitics as a part of the circuit, which is suitable for UHF operation. The proposed topology is a good alternative for the conventional inverter driver, especially at high frequencies. It should be mentioned that the CMOS chip area is expected to be similar for both the proposed resonant gate driver and the typical inverter-type gate driver.

B. Power Transistors and Diodes

Devices capable of high-speed and low-loss operation are essential for highly efficient power converters with compact size. With superior material properties, the GaN-based HEMT is a promising candidate to satisfy such requirements owing to the large bandgap and high electron saturation velocity of the material, and also a high carrier density in the two-dimensional (2-D) electron gas channel in the transistor. Using the class-E topology for the converter, the maximum voltage across and the peak current flowing through the switch could be as large as $3.56 \times V_{\rm IN}$ and $2.86 \times I_{\rm IN}$ respectively, as illustrated in Fig. 2(b) [47]. The GaN power devices are expected to be robust enough to sustain the harsh operating condition. In addition, a very high switching speed can be achieved while maintaining low ON-resistance and high breakdown voltage.

In this work, the 0.25-μm GaN HEMT technology on the SiC substrate provided by WIN Semiconductor is employed to realize both the switching transistor S_1 and the Schottky diode D_1 (see Fig. 4). We select the transistors with various layouts from the device library to meet the design specifications. Note that the internal transistor structure cannot be changed, and the main design parameters are the finger number and the width of each finger. The gate length employed is 0.25 μm for high-speed operation, which is the smallest value provided by this technology. The device is a depletion mode (normally ON) with a threshold voltage $V_{\rm TH}$ of -3 V, and the maximum drain–source voltage is around 120 V before transistor breakdown. The turn-ON voltage for the Schottky gate is 1.1 V. Note that the device is biased with a negative voltage $V_{\rm BIAS}$ at around $V_{\rm TH}$ of -3 V via the bias resistor R_B and dc block C_B (see Fig. 4), and the proposed gate driver is operated under a supply voltage $V_{\rm DD}$ of 2.2 V achieving a voltage swing of about 4.2 V, which is sufficient for switching the GaN HEMT.

Based on the estimated current density, the total width $W_{\rm tot}$ is determined by considering $R_{\rm on}$, power consumption of gate driver, output power level, and GaN chip area at the targeted switching speed. Different combinations of $W_{\rm fin}$ (width of each finger) and n (finger number) were evaluated by simulation. Under a fixed $W_{\rm tot}$ for the multifinger layout, a tradeoff exists between $W_{\rm fin}$ (width of each finger) and n (finger number). With increased n and decreased $W_{\rm fin}$, the parasitic resistance introduced from gate can be reduced effectively. However, the parasitic capacitance increases with n mainly due to coupling among the fingers. Also, the unevenly distributed current in each finger may become an issue when n is too large for a single transistor. The power level increases with the transistor size, but the driving capability of the gate driver and the parasitic capacitances of the power device will ultimately limit the switching speed of the power converter. Based on the above-mentioned considerations, $W_{\rm fin}$ is chosen as 125 μm and $n = 20$ of a transistor in our final design. Two of the transistors are connected monolithically on a single GaN chip by the provided metal layer, and then three units are combined in the IPD substrate. The effective $W_{\rm tot}$ is 15 mm to achieve the desired $R_{\rm ON}$ with a sufficient current level. Fig. 8(a) shows the measured I–V characteristics of the device with 125 μm $\times$ 20 fingers. The peak current density is about

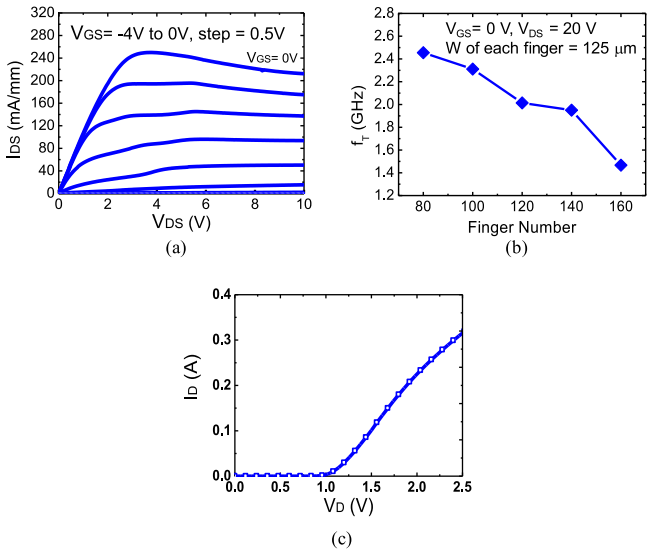

Fig. 8. *I–V* characteristics of (a) GaN HEMT (125 μm $\times$ 20 fingers), (b) cutoff frequency f_T as a function of transistor size, and (c) GaN Schottky diode (width = 5000 μm).

250 mA/mm, which is dropped by about 50% as compared with the foundry provided model. The discrepancy between the measured and modeled I–V characteristics could be attributed to the thermal effect, which is difficult to be predicted by the provided model due to the different ambient thermal conductivities (whole wafer for modeling vs. diced devices in this case) when extracting thermal parameters in the equivalent circuit model. Based on the results in Fig. 8(a), the effective $R_{\rm ON}$ is estimated to be about 0.5 Ω based on measurement with the parasitic resistance of measuring probes calibrated, which is larger than that obtained by the model of about 0.3 Ω. Fig. 8(b) shows the simulated f_T (cutoff frequency) as a function of the transistor size based on simulation. Note that the effective transistor size used in our design is 120 finger by 125 μm of each finger. As the size of power transistor increases, the parasitic capacitances of the transistor increase, which will eventually limit the switching speed of the transistor.

Another important circuit element to achieving a high switching frequency is the diode, which should have a short reverse recovery time. For the fully integrated converter using the IPD technology, a Schottky barrier diode (SBD) is also designed using the same GaN HEMT platform for the power transistor. Differing from an MOS transistor with an isolated gate by the oxide layer, the HEMT has an inherent Schottky gate formed by the gate metal and GaN. An intuitive way to realize a diode based on the transistor structure is to connect the drain and source terminals of GaN HEMT devices as the cathode, while using the gate as the anode to realize an SBD. The GaN diode has a large total finger width of 10 mm (two devices connected in parallel by IPD) to ensure a low $R_{\rm ON}$ for achieving a high overall efficiency. Fig. 8(c) shows the I–V characteristics of the GaN diode (width = 5000 μm). The relatively high turn-ON voltage $V_{\rm ON}$ of about 1.1 V is due to the large bandgap of GaN material. Different approaches were reported to reduce $V_{\rm ON}$ of GaN SBDs [54]–[56]. However, these are not available in the

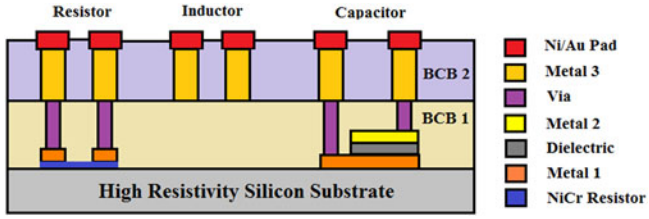

Fig. 9. Cross-sectional view of the integrated passive device (IPD) process.

technology used in this study. If using the Si Schottky diode with a typical $V_{\rm ON}$ of ~0.4 V to replace the GaN diodes in the proposed power converter, the efficiency can be improved by about 3% when only considering the extra power loss due to $V_{\rm ON}$. However, the operating speed of Si Schottky diode is much slower if similar ON-resistance and breakdown voltage need to be achieved, which makes it difficult to use the Si Schottky diode in the UHF range. Similarly, if using the CMOS transistor to replace GaN HEMT for the switching device, based on the fundamental material properties [57], the size will be significantly larger than its GaN counterpart, resulting in a limitation of the operating speed.

C. IPD Passive Components

The idea of power supply-in-package (PSiP) for a compact system with a high operating speed has attracted significant attention in recent years. One critical issue is how to miniaturize the passive devices in the power conversion circuits, especially the relatively large inductive components. Various approaches were proposed to achieve a small area/volume of power converters [6], [7], [58]. In this paper, we propose using the IPD technology to implement the reactive passive components for both gate driver and converter to achieve a compact size with a switching speed up to 300 MHz. As shown in Fig. 9 of the cross section, the IPD process adopted here, which is typically used for RF circuits, is fabricated on a high-resistivity silicon substrate and the benzocyclobutene (BCB) materials are employed for the dielectric layers ($\varepsilon_r = 2.65$) [59], [60]. The resistivity of silicon substrate is over 3 kΩ·cm with a thickness of 650 μm. The BCB layers have a low loss tangent ranging from 0.0008 to 0.002, and the total thickness of BCB 1 and BCB 2 is 13 μm. This technology provides three metallic Cu layers as denoted by metal 1, metal 2, and metal 3 with the thicknesses of 1, 0.65, and 10 μm, respectively. The top metal layer (M3) is mainly for interconnects and planar spiral inductors, which allows to reduce signal loss and obtain high Q inductors owing to the increased metal thickness. A NiCr layer with a thickness of 0.05 μm is deposited for resistors. The IPD process also provides a thin-film high dielectric constant layer ($\varepsilon_r = 6.7$ and $\tan\delta = 0.0002$) with a thickness of 0.2 μm between M1 and M2 to form MIM capacitors with a 300 pF/mm^2 capacitance density, and the breakdown voltage of the capacitor is 40 V. It should be mentioned that the skin depth of Cu is only 3.76 μm at 300 MHz, which implies that the top metal thickness of 10 μm in the IPD process is sufficient for low signal loss at the targeted operating frequency. In the proposed design, all the passive elements including the gate driver (except $C_{\rm SB}$ and $R_{\rm SB}$ in the

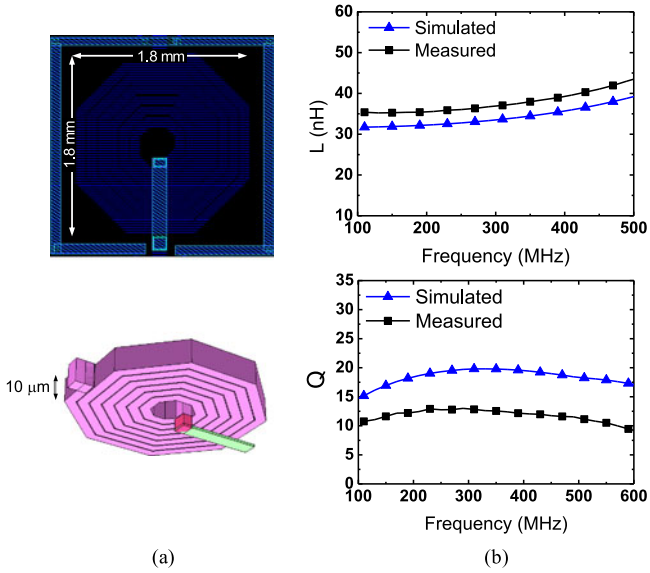

Fig. 10. (a) Layout of the choke inductor L_1. (b) Simulated and measured inductance and quality factor Q of L_1.

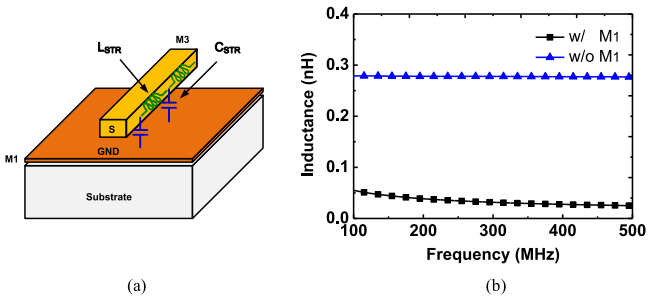

Fig. 11. (a) Conceptual plot of the interconnects used in the proposed UHF power converter, which is similar to a microstrip structure for RF applications. (b) Comparison of simulated parasitic inductance of the interconnects with and without the ground plane M1.

CMOS driver, see Fig. 4) and the class-E power converter are realized by IPD. Compared with implementing these components on either CMOS or GaN technology, IPD devices have the advantages of low cost and high quality factor.

Fig. 10(a) shows the layout and three-dimensional plot of the input choke inductor L_1, which is critical to the efficiency of the class-E resonant power converter. The planar spiral inductor is designed with an octagonal shape to mitigate resistive and capacitive losses [61]. Fig. 10(b) compares the full wave EM-simulated and measured results of the inductor. As can be seen, the measured and simulated inductances are in a good agreement. The discrepancy between the quality factors may be attributed to the process variation with the change of average metal thickness or conductivity. The CMOS gate driver and the GaN devices are flip-chip assembled together on the IPD substrate with the IPD passive devices, which minimizes the parasitic effects caused by bond wires.

Fig. 11(a) shows the interconnect structure of the IPD layout in the proposed UHF power converter, which allows to reduce the parasitic effects for high-frequency operation. The structure employed here is similar to a microstrip line typically used for

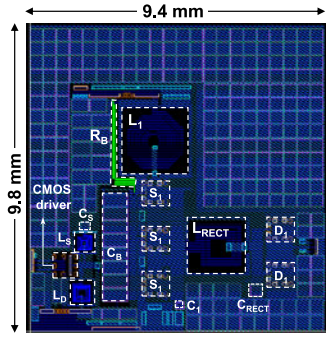

Fig. 12. IPD layout of the proposed UHF power converter, where the locations of different components are highlighted, including the three GaN HEMTs and two GaN Schottky diodes, and also the CMOS gate driver.

RF applications. The signal line is realized by the thick metal M3 of the IPD process, and the ground line is implemented by M1 as a plane throughout the whole chip for a common ground. With the paracitic capacitance $C_{\rm STR}$ existing between the two metal layers, the combination of the stray inductance $L_{\rm STR}$ and $C_{\rm STR}$ forms a microstrip transmission line structure. As a result, the characteristic impedance of the interconnect becomes maily with the real part, and the stray inductance can be effectively reduced. Fig. 11(b) compares the simulated results of a 1000-μm line in the actual IPD layout (width of 300 μm) with and without using M1 as ground. The result clearly indicates reduced parasitic inductance. Another point should be mentioned is that the substrate effect could also play a role as the operating frequency enters the UHF range. The shielding ground plane realized by M1 can isolate the coupled signals via the substrate, which minimizes the undesired interference in the circuit.

Fig. 12 presents the overall IPD layout of the power converter, where the locations of different components (see Fig. 4) are highlighted, including the three 5000-μm GaN HEMTs (S_1) and two 5000-μm GaN Schottky diodes (D_1), and also the CMOS gate driver. In practical design, the sizes of the IPD inductors are determined first due to the considerations of quality factor and chip area. For example, a large L_1 is preferred as the RF choke, but the final design is limited by the degraded quality factor as size increases, which is about 20 with a inductance of 33 nH based on simulation. Similarly, the initial value of $L_{\rm RECT}$ is designed based on the equations mentioned previously, but optimization is essential to obtain a reasonable quality factor at the desired operating frequency for the overall efficiency. In addition, L_S is determined first and then combined with C_S to resonant at around the second harmonic in the gate driver. The inductor load L_D is optimized with $C_{\rm IN}$, L_S, and C_S [see Fig. 6(a)] to shape the gate driver output voltage, and C_B is relatively large as a dc block. It should be emphasized that the core circuit only occupies about half of the chip area. The rest of the chip is mainly employed to obtain sufficient $C_{\rm OUT}$ in the rectifier stage for reducing the output ripple. The capacitances for C_1, $C_{\rm RECT}$, and $C_{\rm OUT}$ in the final design are 17 pF, 36 pF, and 11 nF, respectively. The IPD area can be further reduced if capacitance with a higher density could be realized in the IPD technology or part of the capacitance is also flip-chip stacked on the substrate.

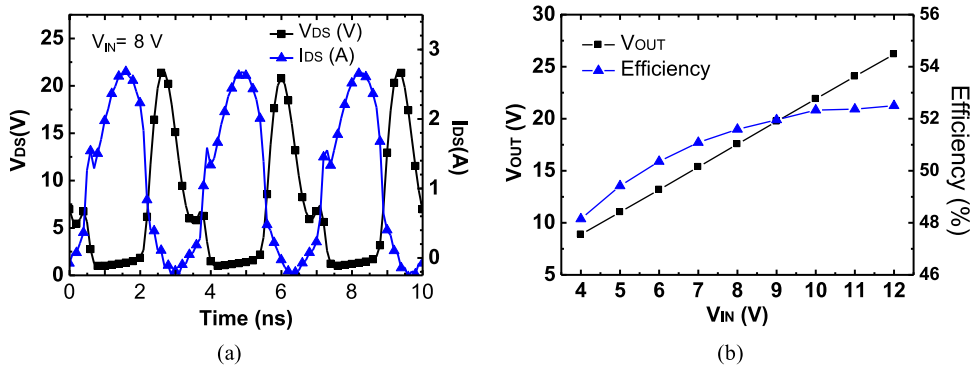

Fig. 13. Simulated results of the UHF power converter (load $= 50\,\Omega$). (a) Time-domain waveforms of voltage and current for the GaN HEMT switching transistor, and (b) output voltage and efficiency as a function of input voltage at 300 MHz.

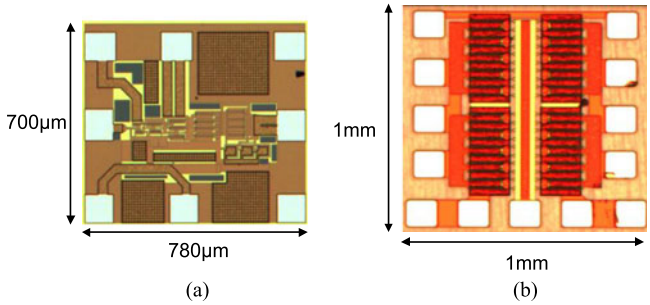

Fig. 14. Micrographs of (a) 0.18-μm CMOS gate driver, and (b) 0.25-μm GaN HEMT ($125\,\mu\text{m} \times 40$).

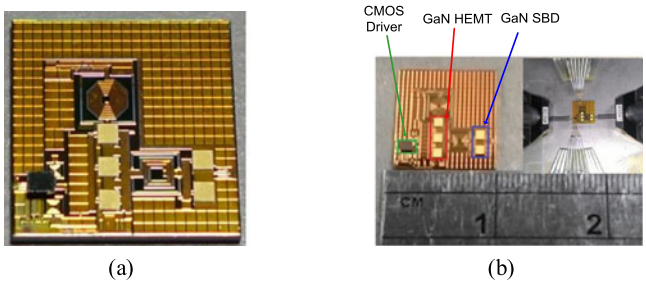

Fig. 15. (a) Photo of the flip-chip assembled power converter, and (b) circuit photo and on-wafer measurement (inset).

Fig. 13(a) shows the simulated waveforms of the GaN switching transistor S_1 in the circuit. The maximum $V_{\rm DS}$ and $I_{\rm DS}$ are about 22 V and 2.7 A ($V_{\rm IN} = 8$ V), respectively. The relatively small overlap between the voltage and current waveforms indicates that the design approaches the ZVS operating condition. The simulated results show that the switching loss is about 15.1% of the total loss under this condition. It should be mentioned that this design is optimized at 300 MHz. Reducing the switch frequency results in deviation from the ZVS condition in the resonant-type power converter, which is not helpful to further reduce the overlap as can be observed from the simulation. Fig. 13(b) shows the simulated output voltage and efficiency as a function of $V_{\rm IN}$. As can be seen, the maximum efficiency can be obtained is around 52% and the maximum $V_{\rm OUT}$ exceeds 25 V.

One issue should be discussed here is the closed-loop control of the proposed circuit, which is a critical part of the whole system. As mentioned previously, this work focuses on using novel SiP technology to explore the possibility of achieving high-speed UHF dc–dc power converter with a high power density. The closed-loop control is not within the scope of this work. Although not actually implemented, one possible control configuration can be used is the ON–OFF control scheme, which was reported for resonant power converters [10], [11]. The control algorithm is relatively simple, but practical implementation becomes challenging as the operating frequency increases. The main limitation could be the required high-speed comparator in the control circuit. Also, the stability of the circuit could be an issue in the board level design with unpredicted parasitic effects. It should be mentioned that the closed-loop controller demonstrated in previous works [10], [11] used the commercially available ICs to achieve the goal. In our design, we have the advantages of SiP technology with CMOS circuits. The control circuitry can be integrated with the gate driver using the standard CMOS process, which can reduce the cost and minimize the parasitic effects by the flip-chip package and is suitable for high-frequency operation.

IV. Results and Discussion

Fig. 14(a) and (b) shows the chip micrographs for the CMOS gate driver and the GaN HEMT device ($125\,\mu\text{m} \times 20$ fingers $\times$ 2), respectively. The overall circuit photo of the fully assembled converter on the IPD substrate is shown in Fig. 15(a). Fig. 15(b) shows the photo of the power converter, with the inset showing the on-wafer measurement using RF and dc probes. Fig. 16(a) and (b) shows the measured output power and dc voltage of the proposed class-E power converter at 300 MHz. An output power of 4.16 W (load $= 50\,\Omega$) and output voltage of 18 V (load $= 100\,\Omega$) can be achieved at $V_{\rm IN}$ of 12 V at 300 MHz. Fig. 16(c) plots the corresponding output current versus the input voltage. As can be observed, the current level reduces with the increased load, and the maximum current level in the measured voltage range is 288.5 mA (load $= 50\,\Omega$). Fig. 16(d) compares the measured and simulated output current levels. The discrepancy increases with $V_{\rm IN}$, which implies that the thermal effect becomes more significant at high power levels and cannot be predicted accurately by the provided model. Fig. 17(a) shows the measured overall efficiency of the proposed class-E power

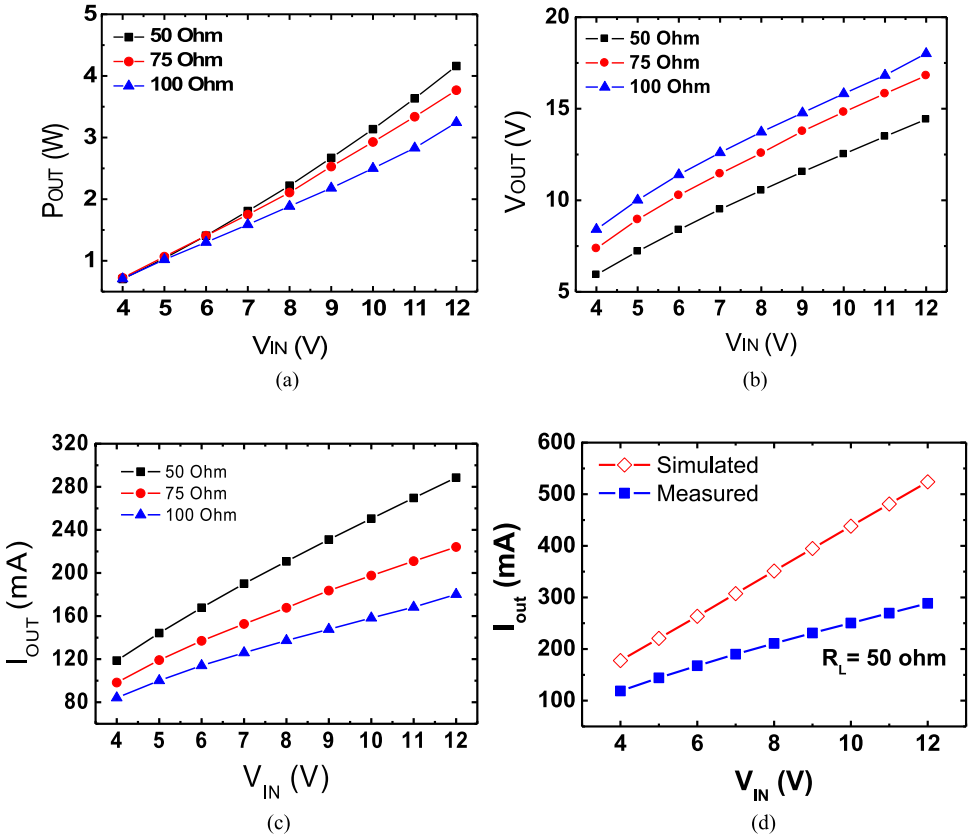

Fig. 16. Measured (a) output power, (b) output voltage, and (c) output current as a function of input voltage of the proposed class-E power converter. (d) Comparison between the simulated and measured output current.

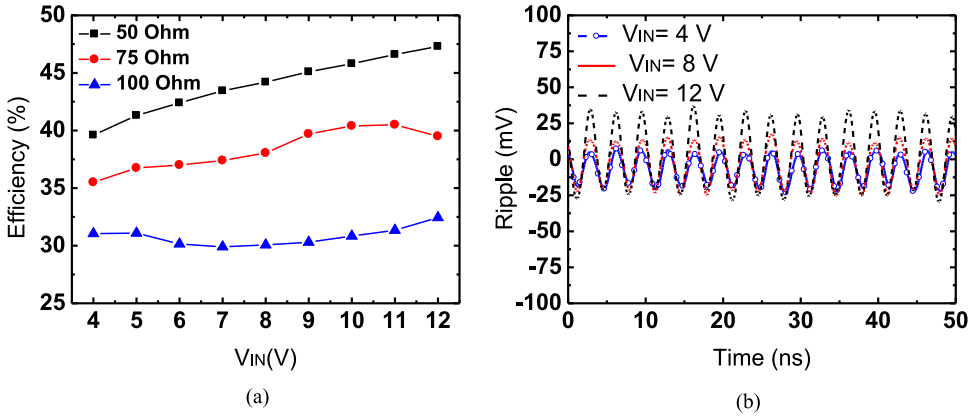

Fig. 17. (a) Measured overall efficiency of the proposed class-E power converter. (b) Measured output ripple with different input voltages.

converter. The highest efficiency of 47.3% can be obtained at $V_{\rm IN} = 12$ V with a load of 50 Ω. The result indicates a trend of reduced efficiency when the load moves away from the target value (50 Ω in this design). Fig. 17(b) shows the output ripple at different input voltages with a 50-Ω load, which is relatively small compared with the fully integrated converters reported in [9]. It should be emphasized that the reduced efficiency compared with the simulated results as shown in Fig. 13(b) can be mainly attributed to the degraded GaN device characteristics due to thermal effect, which is difficult to be predicted accurately in the foundry provided model. Another reason is the reduced Q factor of the IPD inductor compared with simulation (see Fig. 10), which also introduces extra loss and degrades the overall efficiency.

Fig. 18 analyzes the loss from different parts of the power converter based on simulation. The values of total power loss $P_{\rm loss}$ are 5.79, 6.96, and 7.89 W (total output power $P_{\rm out}$ are 6.17, 5.77, and 5.23 W) respectively, corresponding to the loads of 50, 75, and 100 Ω. Note that the measured results under this condition ($V_{\rm IN} = 8$ V) for $P_{\rm loss}$ are 2.80, 3.43, and 4.38 W ($P_{\rm out}$ are 2.22, 2.11, and 1.89 W). The efficiency limitation of the resonant power converter presented in this work can be mainly attributed to the loss of the power transistor and the loss of spiral inductors. As shown in the figure, the loss of the power

TABLE I
COMPARISON WITH PREVIOUS WORKS OF HIGH-SPEED POWER CONVERTERS IN DIFFERENT TECHNOLOGIES

Ref.	Type	Topology	Technology	f_{SW} (MHz)	V_{IN}/V_{OUT} (V)	$I_{OUT,max}$ (mA)	$P_{OUT,max}$ (W)	η_{max} (%)	Area/volume (cm^2/cm^3)	Power density (W/cm^2)
[3]	Module	Resonant Step-up	Discrete MOSFET + PCB	100	12/23.7	72	1.7	55	N/A	N/A
[4]				60	6/15	467	7	77	N/A	N/A
[5]		Step-down	GaN IC + discrete component + PCB	200	25/10	256	3.3	73	N/A	N/A
[6]	PSiP	Step-down	CMOS IC + stacked CMOS *LC* component	200	3.3/2.3	70	0.161	62	0.2×0.2	4
[7]			CMOS IC + bond wire inductor	50	3.3/2	300	0.6	68.7	$0.36 \times 0.28^{*}$ $0.72 \times 0.64^{**}$	5.95^{*} 1.3^{**}
[8]	PSoC	Step-down	CMOS IC	225	2.6/1.2	600	0.8	58	0.16×0.235	21
[9]		Step-up	GaN IC	680	12/20.2	90	1.8	34	0.3×0.3	20
This work	PSiP	Resonant Step-up	GaN IC + CMOS IC + IPD	300	$12/18^{\#}$	288	4.16	47.3	$0.94 \times 0.98/0.115$	$4.5/36.2$ (W/cm^3)

*Bonding wires not included; **Estimated including the bond wires; and #Maximum output voltage condition.

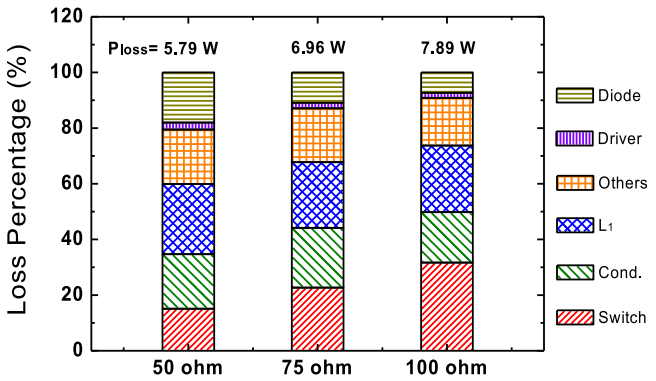

Fig. 18. Analysis of loss from different parts of the proposed class-E power converter for three different loads based on simulated results.

transistor is in the range of 36–50% including both switching and conduction losses. Also, the loss of the choke inductor L_1 plays an important role, up to 23–25% of the total. The major part in the loss of others comes from L_{RECT} in the parallel *LC* resonant tank. Compared with the conventional hard switching configuration, the higher conduction loss can be attributed to the larger current (2.86× of the input dc current) in the class-E topology. Also, the 2-D planar inductor adopted here with a relatively lower Q limits the overall efficiency, especially the relatively large inductors L_1 and L_{RECT}. It should be mentioned that the GaN HEMT devices have a high channel mobility and is expected to result in a small conduction loss. However, the pronounced thermal effect here seriously degraded the transistor performance, which can be improved by proper packaging technology of the GaN devices. In addition, compared with most previously published hard switching designs using the discrete inductors with much higher Q, the 2-D planar inductor in the IPD technology is much compact but the lower Q degrades the overall efficiency. If the discrete RF choke is employed or the IPD technology can be further improved with novel low-loss magnetic materials, the overall efficiency in the proposed design is expected to be further increased. The simulated results indicate if the Q factor is doubled and R_{ON} of the switching transistor and diode are reduced by half, the efficiency of the proposed power converter can be improved to 74%. With the proposed resonant gate driver, the loss is well controlled. The trend of increased transistor loss can be observed when the load deviates from a target of 50 Ω due to the change of the resonant frequency of the class-E topology. This also explains the obviously increased switching loss at light load operation of 100 Ω. As a result, the ZVS condition cannot be maintained, leading to efficiency reduction [12], [62]. Studies have been reported that proposed solutions to this issue [62], [63].

Table I compares the published high-frequency (from tens up to hundreds of MHz) power converters in different packaging types and technologies. The class-E and class Φ_2 dc–dc converters operating at 100 and 60 MHz were reported in [3] and [4], respectively, using discrete components on the printed circuit board (PCB) to demonstrate the resonant-type converters in the VHF range. An open-loop power converter with the GaN HEMTs operating at 200 MHz showed the possibility of using the high switching power converter for EER applications [5]. The studies in [6]–[8] utilized the CMOS passive components or bond wire inductor to demonstrate the potential of PSiP/power system-on-a-chip (PSoC) for low-power and high-speed applications. The circuit reported in [9] employed a fully integrated boost converter using GaN technology, and a high power density can be obtained at a switching frequency of 680 MHz. Compared with the prior arts listed in Table I, this work presents an effective approach using IPD heterogeneous integration for high power density with more design flexibility and low cost. As can be seen, the proposed resonant-type class-E design demonstrates a relatively high operating frequency compared with other PSiP studies. Also, the output power is among the highest compared with all the PSiP and PSoC designs. The efficiency of this work also achieves a level that is comparable with other PSiP or PSoC work.

V. CONCLUSION

A 300-MHz class-E dc–dc converter with a resonant gate driving technique was proposed and implemented using 0.25-μm

GaN HEMT power devices, a 0.18-μm CMOS gate driver, and IPD passive components. With all microfabricated components and circuit blocks, the miniaturized converter was fully integrated by a flip-chip assembly on the IPD substrate and has a volume of only 0.115 cm^3. A maximum output power of 4.16 W and a corresponding power density of 36.2 W/cm^3 can be obtained. The achieved efficiency of 47.3% was also comparable with the recently published work on highly integrated converters at high frequencies. This study demonstrates the possibility to realize highly integrated power converters using the approach of heterogeneous integration of different processes for next-generation miniature power converters. It should be emphasized that the limitations of the presented power converter are mainly from the thermal effect of GaN power devices and the relatively low Q of the IPD inductors. The thermal effect could be reduced by introducing proper package technology. Also, the low-loss magnetic materials may be incorporated to enhance the quality factor of the inductive components in the IPD process.

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