Design of 60-GHz Low-Noise Amplifiers With Low NF and Robust ESD Protection in 65-nm CMOS

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***Abstract*—This paper presents two 60-GHz low-noise amplifiers (LNAs) with different electrostatic (ESD) protection schemes, including the diode-based and *LC*-based configurations. By codesigning ESD network and input matching, both LNAs are optimized for minimum noise figure (*NF*) while maintaining a similar gain. Compared with the conventional double-diode approach, the proposed *LC*-based design uses a high current capability spiral inductor and a high breakdown voltage metal-oxide-metal capacitor as effective bidirectional ESD protection, showing much improved ESD protection level and *NF* under reduced power consumption. The test results demonstrate an over 8-kV human–body-model ESD level and an over 13-A very fast transmission line pulse current level for charge-device-model ESD protection. The measured *NF* and power gain are 5.3 dB and 17.5 dB, respectively, at 58 GHz, under a power consumption of only 18 mW. To the best of our knowledge, the *LC*-based ESD-protected LNA demonstrates a highest ESD protection level with a lowest *NF*, compared with prior arts operating at similar frequencies.**

***Index Terms*—Charge-device-model (CDM), CMOS, electrostatic discharge (ESD), human-body-model (HBM), low-noise amplifier (LNA), transmission line pulse (TLP), *V*-band, very fast transmission line pulse (VFTLP).**

I. Introduction

USING the millimeter-wave (mm-wave) frequency range for wireless communications has attracted a great deal of interest from both academia and industries over the past few years, which permits a compact system size and high data transmission rate up to multi-Gb/s [1]–[5]. At *V*-band (50–75 GHz), the large bandwidth allocated at around 60 GHz offers great potential and flexibility for various new applications. With continuous advances in process technology, CMOS demonstrates impressive f_T and $f_{\max}$ under low power consumption, and becomes a realistic low-cost solution for fully-integrated 60 GHz transceivers [2]–[5]. One critical issue for realizing the fully-integrated 60 GHz radio is the electrostatic discharge (ESD) problem. In advanced technology nodes, the reduced gate oxide thickness (~ 20 Å in 65 nm CMOS) and hence lowered gate oxide breakdown voltage (~ 6.5 V in 65 nm CMOS) make the device more vulnerable to ESD damage. Also, the recent trend of system-on-chip (SOC) design results in a large chip size with considerable amount of charges accumulated in the substrate. This increases the susceptibility to ESD damage for volume production [6]–[8].

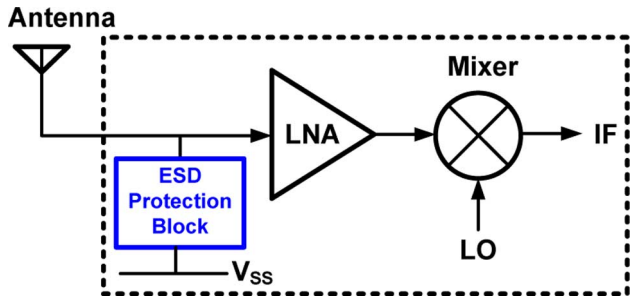

Fig. 1. Typical RF receiver front-end including the ESD protection block connected at the RF input terminal.

Different approaches for RF ESD protection design were reported [9]–[18]. The double-diode configuration is one of the most widely adopted designs for RF ESD protection, owing to the simplicity and relatively small parasitic capacitances. However, the ESD protection level is in general proportional to the parasitic capacitances of the diodes, [9], [10], which poses a significant challenge of designing robust on-chip ESD protection for a 60-GHz receiver with low noise figure (*NF*) in advance CMOS technology. Fig. 1 shows the circuit blocks of a typical RF receiver with ESD protection. In ideal cases, the ESD block should act as an open circuit under normal RF operation, while becoming a short circuit when ESD zapping occurs. The overall noise figure can be calculated as $F_{\text{total}} = F_{\text{ESD}} + F_{\text{LNA}} + (F_{\text{mixer}} - 1)/G_{\text{LNA}}$, assuming the noise contribution from the circuit blocks after the mixer can be neglected, where F_{total}, F_{ESD}, F_{LNA}, and F_{mixer} represent the *NF* of the overall system and the individual blocks, respectively, and G_{LNA} is the power gain of the LNA. It should be emphasized that F_{ESD} is equivalent to the loss introduced by the passive ESD block, and will be directly added to the overall system noise figure. With the double-diode topology, the increased insertion loss of the diodes would significantly degrade F_{total} if a high ESD protection level is desired at high operating frequencies.

Differing from the diode-based approach, the on-chip ESD protection design using the grounded inductive components was proposed [12]. The basic idea is to provide a direct ESD current path shunt to the ground, while also using the inductor to

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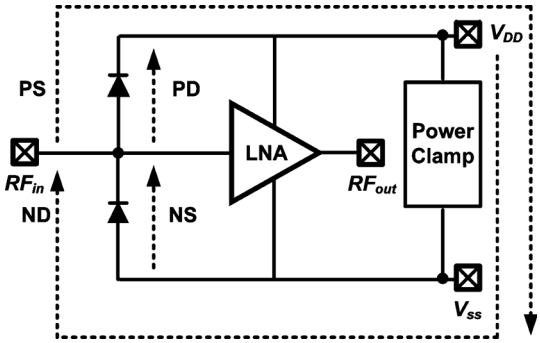

Fig. 2. Circuit blocks of the LNA with double-diode ESD protection. The four different testing modes are also indicated.

resonate with the pad parasitics, making the ESD block transparent at the operating frequencies. An ESD protection scheme with a grounded inductor by plug-and-play was proposed to tune out the parasitic capacitance at 5 GHz [13]. Using the similar concept of [12] and [13], a multilayer coplanar waveguide inductor $L_{\rm ESD}$ for grounding the ESD current was used to resonant out the pad capacitance at 77 GHz [14]. A transformer-based ESD protection for LNA was also reported [15], in which the ESD inductor and the LNA gate inductor were combined as a transformer to reduce the chip area, and a 7.3 kV Human-Body-Model (HBM) ESD level was achieved.

To realize the ESD-protected LNA with low noise figure, low power consumption, and high ESD protection level at 60 GHz, two different approaches of ESD network design are employed for comparison in this study. With the same core circuit configuration, the first LNA adopts the typical double-diode approach, whereas the second LNA proposes a shunt inductor and a series capacitor for ESD protection, denoted as *LC*-based design. It should be emphasized that the ESD protection scheme of the second LNA may look similar to the previously reported studies using inductive components for ESD design [12]–[18], however, the codesign concept with the entire input matching network was not mentioned before. Also, the significance of $C_{\rm ESD}$ to the ESD robustness in the inductor-based ESD design was not pointed out.

The ESD blocks are codesigned with the input matching network in both LNAs, and optimized for minimum *NF* with a similar gain. By comparing the results of the two LNAs, the second design shows clear advantages over the first design in *NF*, power consumption, and also ESD protection level with a small penalty of the chip area. The increases in the bandwidths of both input matching and power gain are also obvious with the *LC*-based ESD design. The second design demonstrates a state-of-the-art ESD-protected LNA at around 60 GHz, to the best of our knowledge. This paper is organized as follows. Section II presents the first LNA design using the diode-based ESD protection scheme. In Section III, the design details of the second LNA using the proposed *LC*-based ESD protection are presented. The experimental results including both RF and ESD measurements are shown in Sections IV, and V concludes this work.

II. Design of 60-GHz LNA With Diode-Based ESD Protection

Fig. 2 shows the widely used double-diode ESD protection scheme for RF applications [6]–[10] together with the power clamp [10]. The discharge paths for the four different ESD testing modes (PD, ND, PS, and NS) are also indicated in Fig. 2. The diodes could be realized by different approaches, such as shallow-trench-isolation (STI) diodes [9], poly diodes [19], and RF junction varactors [10]. The approach of using the customized RF junction varactors with accurate RF models is adopted in this design.

Fig. 3 shows details of the 60-GHz LNA using the double-diode ESD topology, consisting of the RF junction varactors (JV_T and JV_B) and the power clamp ($M_{\rm ESD}$, M_P, M_N, M_C, and R). The LNA core circuit employs a two-stage cascode topology with inductive loads (L_{D1} and L_{D2}) for high power gain and better input/output isolation. The inductive source degeneration (L_S) is employed to make it easier to achieve simultaneous noise and power matching. Note the input matching network includes L_{G1}, JV_T, and JV_B, together with L_S. The capacitor C_{12} functions as the dc block between the two stages, and works together with L_{G2} and L_{D1} as the interstage matching. The inductor L_{D2} and capacitor C_{D2} are utilized as the output matching network. The power clamp with a linear characteristic provides a low-impedance path from $V_{\rm DD}$ to the ground, and completes the ESD paths for PS and ND modes [10]. Note that the power clamp, connected between the $V_{\rm DD}$ power rail and the $V_{\rm SS}$ ground bus, is not critical to the LNA RF characteristics.

Using the codesign approach, the ESD devices JV_T and JV_B should be considered in the early design stage as a part of the input matching network. Therefore, an accurate RF model is required along with the known ESD protection level for the codesign procedure. In this study, the junction varactors are customized by utilizing the maximum allowed contact and via density ($\sim 10\ \mathrm{contacts}/\mu\mathrm{m}$ in each finger). Also, all six metal layers with a total thickness of $\sim 5\ \mu\mathrm{m}$ are connected by vias along the ESD current path to reduce the on-resistance. The RF models are established based on the measured results from the device testkeys. Also, the ESD protection levels are determined by the Transmission Line Pulse (TLP) tests with the testkeys. Table I shows the measured TLP results of the junction varactors with different geometries, where It_2 is the second breakdown current. The corresponding HBM ESD voltage level $V_{\rm ESD}$ is estimated by $It_2 \cdot R_{\rm HBM} (R_{\rm HBM} = 1.5\ \mathrm{k}\Omega)$ [6]. The extracted parasitic capacitance $C_{\rm ESD}$ and ratios of the ESD protection level to parasitic capacitances $V_{\rm ESD}/C_{\rm ESD}$ are also included. As can be seen, the ESD protection level increases with the device size and also the parasitic capacitance. Note $V_{\rm ESD}$ should increases proportionally with the total device periphery in ideal cases. However, as can be seen from Table I, the increase of $V_{\rm ESD}$ gradually reduces as the ESD device becomes larger due to increased series resistance of larger finger width. The junction varactor W2N25 (width of each finger $W = 2\ \mu\mathrm{m}$, and total finger number $N = 25$) with a high $V_{\rm ESD}/C_{\rm ESD}$ ratio of 98.1 is chosen for achieving a ~ 2 kV HBM ESD level in this design.

With the selected ESD diodes, the main remaining design parameters of the input stage are the size of M_1 and M_2, the source inductor L_S and the gate inductor L_{G1}. As mentioned, the design goal is to achieve a minimum *NF* but with a similar gain of the *LC*-based ESD design for fair comparison. Therefore, the power consumption is not the major design consid-

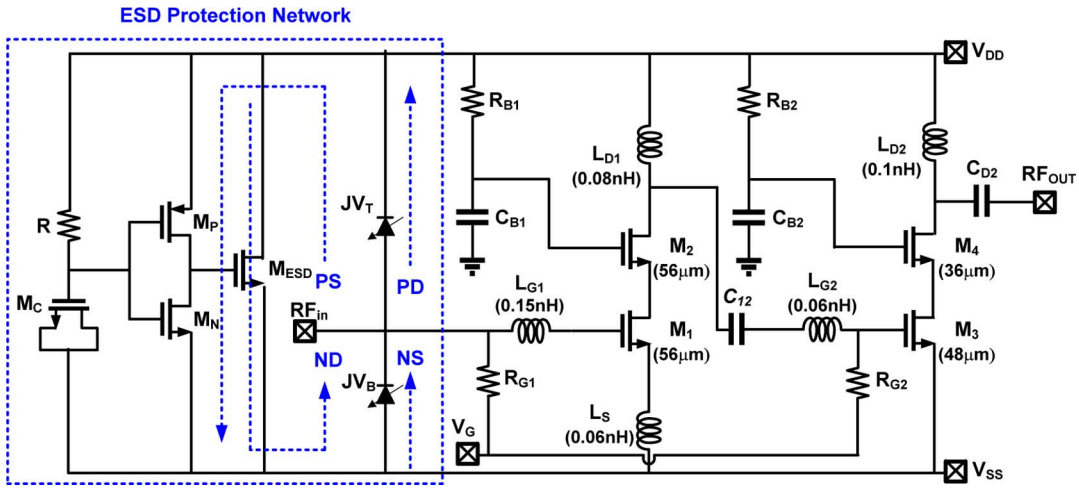

Fig. 3. Circuit schematic of the 60-GHz LNA with diode-based ESD protection, using the RF junction varactors (JV_T, JV_B) and a power clamp.

TABLE I
ESD CHARACTERISTICS WITH DIFFERENT DEVICE SIZES

	W	L	N	It_2	V_{ESD}*	C_{ESD}#	V_{ESD}/C_{ESD}
Unit	μm	μm	--	A	kV	fF	V / fF
W1N25	1	0.15	25	0.7	~ 1.0	10.9	91.7
W1N50	1	0.15	50	1.4	~ 2.1	21.7	96.7
W2N25	2	0.15	25	1.4	~ 2.1	21.4	98.1
W2N50	2	0.15	50	2.4	~ 3.6	47.9	75.2
W4N50	4	0.15	50	4.6	~ 6.9	98.3	70.2

* The ESD levels are estimated from the TLP tests ($V_{HBM} \sim It_2 \cdot R_{HBM}$).
\# The extract parasitic capacitance at 60-GHz.

eration here. For both gain and stability considerations, an Ls of 0.06 nH is used for the source degeneration. The transistor size of $M_1(W = 56\ \mu\text{m})$, $M_2(W = 56\ \mu\text{m})$, and the gate inductor L_{G1} of 0.15 nH are then determined based on optimization to achieve enough power gain and minimized noise figure with the predetermined junction varactors. The second stage are optimized mainly for obtaining enough power gain with the transistor $M_3(W = 48\ \mu\text{m})$ and a slightly smaller transistor $M_4(W = 36\ \mu\text{m})$. Determination of M_4 also needs to consider the output matching. Together with L_{D2} of 0.1 nH and C_{D2} of 23.4 fF, an output impedance of 50 Ω is achieved at around 60 GHz.

As will also be shown in Sections III–V, the second LNA can achieve an ESD protection level of over 8 kV by using a shunt inductor with a high current density and a series capacitor with a high breakdown voltage. It is interesting to see if this is feasible using the double-diode design. Figs. 4 and 5 show the simulated power gains and noise figures, respectively, of the double-diode LNA with several different ESD protection levels (same core circuit but different diode sizes). Note the ESD devices used for simulation are based on Table I, but the protection levels are estimated from ideal cases, assuming the ESD level increases proportionally to the device periphery. Also, the LNAs are all optimized to be conjugate-matched for a fair comparison. As shown in the figures, the power gain decreases with increasing ESD protection levels owing to the increased parasitic effect with larger ESD diodes, which is evident from the lowered Q value when the diode size increases. As the diode size becomes larger, the increased substrate parasitic capacitance C_{sub} [7] is

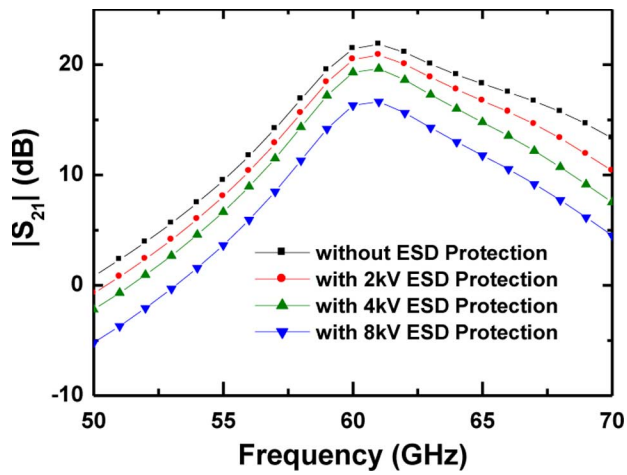

Fig. 4. Simulated $|S_{21}|$ of the LNA using double-diode design with various ESD protection levels.

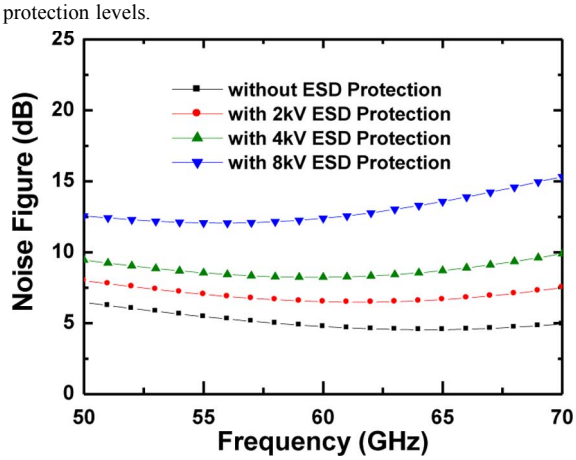

Fig. 5. Simulated *NF* of the LNA using double-diode design with different ESD protection levels.

responsible to the increased loss of the diode at high frequencies, which creates a low-impedance signal path to the substrate directly. Also, the increased series parasitic resistance from the long interconnects introduces additional losses. Similar explanation can be applied to the observed increasing noise figure. The gain and *NF* degradations are 5.1 dB and 7.6 dB, respectively, compared with the reference design without the ESD

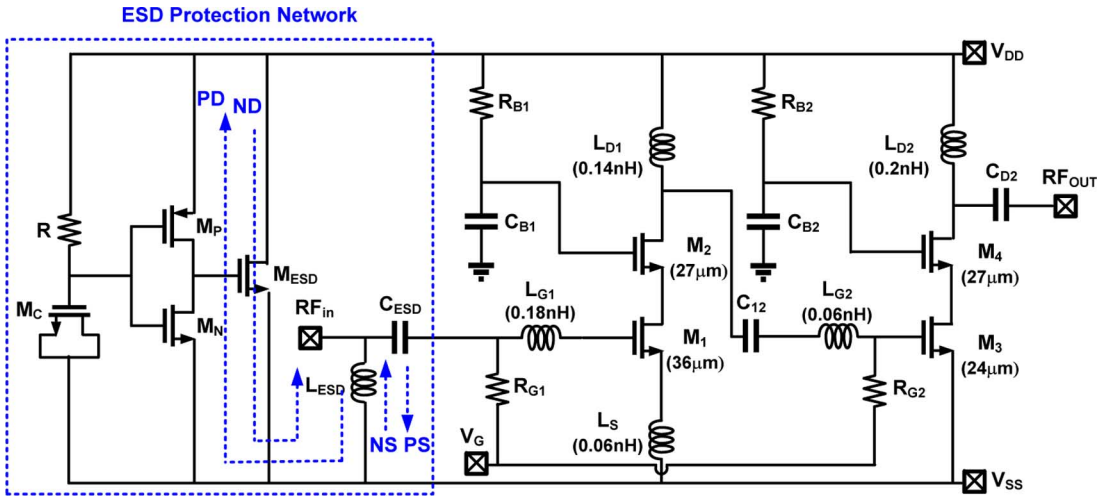

Fig. 6. Circuit schematic of the proposed 60-GHz LNA with *LC*-based ESD protection, consisting of the spiral inductor $L_{\rm ESD}$, MOM capacitor $C_{\rm ESD}$, and a power clamp.

diodes. Even with a 2-kV ESD design, a *NF* increase of 1.7 dB can be observed associated with a 1 dB gain reduction.

III. Design of 60-GHz LNA With *LC*-Based ESD Protection

In the second 60-GHz LNA, we propose using an *LC* high-pass network (low-pass for ESD current) codesigned with the entire input matching network to realize a robust ESD network while maintaining a very low noise figure. Compared with the previously reported LNAs using the inductive ESD devices [12]–[15], [20], the inductor $L_{\rm ESD}$ here is neither for RF choke [20] to make the ESD diode invisible at RF frequencies nor for resonating out the diode or pad parasitic capacitances [12]–[15]. Also, the importance of $C_{\rm ESD}$ to the ESD protection level, which was not emphasized before, will be pointed out in this study.

Fig. 6 shows the circuit configuration of the proposed LNA with the *LC*-based ESD protection network. The input matching network includes the shunt inductor $L_{\rm ESD}$, metal-oxide-metal (MOM) capacitor $C_{\rm ESD}$, gate inductor L_{G1}, and source inductor L_S. As a part of the matching network, the high-pass $L_{\rm ESD}$-$C_{\rm ESD}$ network acts like typical passive elements under normal RF operation. However, it becomes a low-pass network to the ground for the ESD current with relatively low frequencies. During ESD zapping, $L_{\rm ESD}$ provides a low-impedance bidirectional path to bypass the discharge current, and $C_{\rm ESD}$ further blocks the ESD current to protect the core circuit. Fig. 7 is the corresponding small-signal equivalent circuit model of the input stage. The impedance of the input stage can be represented by the following equations:

$$Z_{\rm IN} = \frac{g_{m1}L_S}{C_{\rm in}} + j\left[\omega L_S - \frac{1}{\omega C_{in}}\right] \quad (1)$$

$$Z_{\rm IN}\prime = (j\omega L_{\rm ESD}) \,//\, \left(\frac{1}{j\omega C_{\rm ESD}} + j\omega L_{G1} + Z_{\rm IN}\right). \quad (2)$$

The $L_{\rm ESD}$ and $C_{\rm ESD}$ are combined with L_{G1}, $C_{\rm in}$ (the equivalent input capacitance at the gate of M_1), and L_S to have the real part of $Z_{\rm IN}$' as 50 Ω, and the imaginary part of $Z_{\rm IN}$' to be zero. The transistor size is determined by investigating the noise and gain characteristics as a function of finger width and

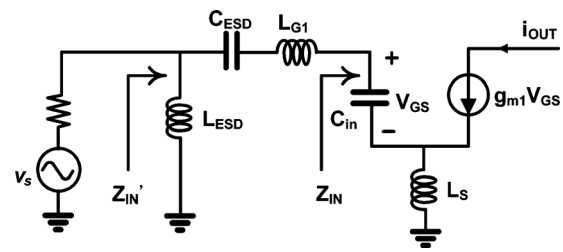

Fig. 7. Small-signal equivalent circuit model of the input stage of the LNA with *LC*-based ESD protection.

bias [21]. The final selected gate voltage is 0.65 V with a current density of 0.24 $\rm mA/\mu m$ for $M_1(W = 36\ \mu\rm m)$ for low noise characteristic. As a part of the matching network, determination of $L_{\rm ESD}$ and $C_{\rm ESD}$ should be in the early RF design stage for noise and gain optimization. The inductor $L_{\rm ESD}$ is the most critical component for the ESD protection level, which is determined first in the design flow. To sustain a large ESD current level (typical up to several Amperes) with a small parasitic resistance, the metal width of ESD inductor is designed to be 10 $\mu\rm m$. Also, a half-turn inductor realized by the top metal layer (thickness of 3.4 $\mu\rm m$) with a total length of only 115 $\mu\rm m$ is employed to avoid the high resistivity vias in multiple-turn inductors and to reduce *IR* drop during ESD zapping. Based on the measurement results, the maximum current capability of the inductor can be up to 39 A under an HBM TLP pulse.

The $C_{\rm ESD}$ is employed to increase the upper bound ESD design window from 6.5 V (gate oxide breakdown voltage) up to $\sim$ 75 V (MOM breakdown voltage). From the ESD protection point of view, $C_{\rm ESD}$ functions as a substitute of the gate capacitor of M_1. With the extremely robust MOM capacitor, the ESD protection level can be increased significantly. In addition, $C_{\rm ESD}$ increases the design freedom by adding one more parameter in the input matching network, resulting in a much wider bandwidth of the LNA. In practical design, L_S and $L_{\rm ESD}$ are determined first, and $C_{\rm ESD}$ and L_{G1} are cooptimized to obtain the minimum noise figure and maximum gain. With the codesign approach, relatively small $L_{\rm ESD}$ (60 pH) and $C_{\rm ESD}$ (0.47 pF) with high quality factors are allowed, and the reduced parasitics lead to excellent noise performance of the LNA. The detailed

TABLE II
DEVICE PARAMETERS OF $L_{\rm ESD}$ AND $C_{\rm ESD}$

Para.	Ind. / Cap.	W	V_{BD}	I_{max}	Q
L_{ESD}	60 pH	10 μm	--	39 A	44
C_{ESD}	0.47 pF	--	75 V	--	135

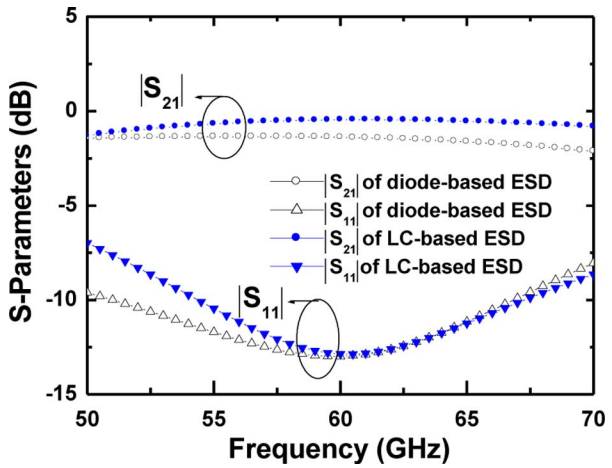

Fig. 8. Simulated insertion losses (ESD blocks only) of the two different ESD configurations under input/output conjugate matching.

design parameters for $L_{\rm ESD}$ and $C_{\rm ESD}$ are listed in Table II. In addition, the areas occupied by $L_{\rm ESD}$ and $C_{\rm ESD}$ are only $\sim$0.008 and 0.0006 $\rm mm^2$, respectively.

It should be emphasized that the ESD protection limitation in this design in fact arises from the power clamp instead of $L_{\rm ESD}$ and $C_{\rm ESD}$, differing from the typical diode-based RF ESD design. With a large enough width and short enough length, the *IR* drop across of $L_{\rm ESD}$ is very low. Also, the robust MOM capacitor $C_{\rm ESD}$ has a much higher breakdown voltage than the gate oxide. Consequently, the power clamp will be damaged by the discharge current before $L_{\rm ESD}$ and $C_{\rm ESD}$. Since the $L_{\rm ESD}$ and $C_{\rm ESD}$ are not the bottleneck of the ESD protection level, the codesign procedure becomes relatively straightforward, compared with the first design. Although also using the codesign approach in the double-diode scheme, the ESD level of the diode is the main consideration in the early design stage of diode size determination. With such a limitation, the optimization among *NF*, gain, and ESD protection level become more difficult. In practical design at V-band, the LNA characteristics are rather sensitive to the capacitive parasitics at the input node even in the range of only tens of fF. Also, the issue of a relatively low Q-factor ($\sim$4 at 60 GHz for the RF junction varactors) arises at high frequencies, which degrades both *NF* and gain owing to the insertion loss introduced by the diodes. Fig. 8 shows the simulated insertion losses of the two ESD protection configurations (ESD blocks only) with ideal input/output conjugate matching at 60 GHz. The relatively large matching bandwidth is due to the multistage topology (Pi-matching) used for the matching network, which is close to the condition in the actual LNAs. As can be seen, the insertion loss of the first ESD design (JV_T and JV_B both shunted to the ground with the size of $W = 2\,\mu$m, and $N = 25$, W2N25) is 1.4 dB, almost 1 dB higher than that of the second design ($L_{\rm ESD}$ shunted to the ground and $C_{\rm ESD}$ connected in series). The extra loss will add an equivalent

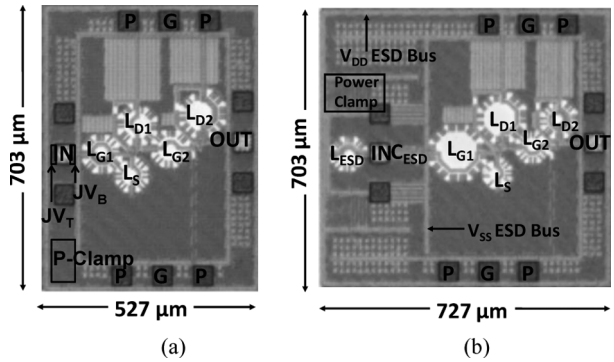

Fig. 9. Chip micrographs of the 60-GHz LNAs with (a) diode-based ESD protection, and (b) *LC*-based ESD protection.

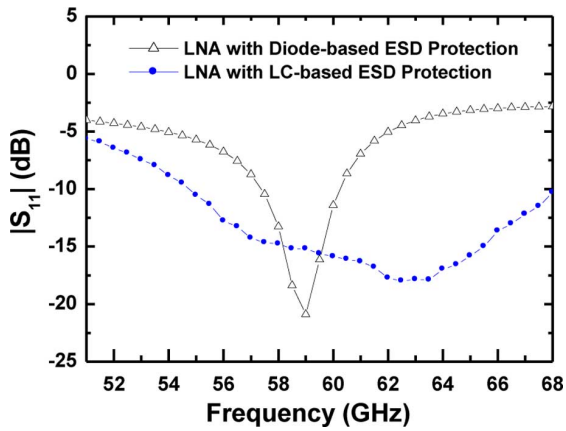

Fig. 10. Measured $|S_{11}|$ of the LNAs with diode-based and *LC*-based ESD protection.

amount of *NF* to the LNA directly, as illustrated in Fig. 1. Once the desired ESD level is determined with a certain amount of $C_{\rm ESD}$, the degradation of *NF* and gain cannot be avoided in the double-diode configuration even with the codesign approach. As a result, increased power consumption is essential to obtain a small noise figure and maintain a similar gain with the *LC*-based design. In practical design, the larger transistor sizes are used to accommodate the desired power gain with increased power consumption. In the second design with the *LC*-based approach, the designer can mainly focus on the optimization of gain and *NF* instead of the ESD protection level when selecting $L_{\rm ESD}$ and $C_{\rm ESD}$, which greatly simplifies the ESD/matching codesign procedure.

IV. RESULTS AND DISCUSSION

The LNAs were fabricated using 65-nm CMOS technology with both f_T and $f_{\rm MAX}$ exceed 200 GHz. Fig. 9(a) and (b) show the chip micrographs of the implemented 60-GHz LNAs with the diode-based and *LC*-based ESD protection schemes, respectively. The dc block is provided by an off-chip Bias-Tee at the input for RF measurements in both LNAs. With two sets of G–S–G RF probing pads and another two sets of the P–G–P dc probing pads, the chip sizes are 0.37 and 0.51 $\rm mm^2$ for the two designs, respectively. It should be emphasized that the sizes are pad limited in both chips. Compared with the intrinsic size of the first LNA (0.15 $\rm mm^2$), that of the *LC*-based design only increases by about 0.0086 $\rm mm^2$ (5.7%)

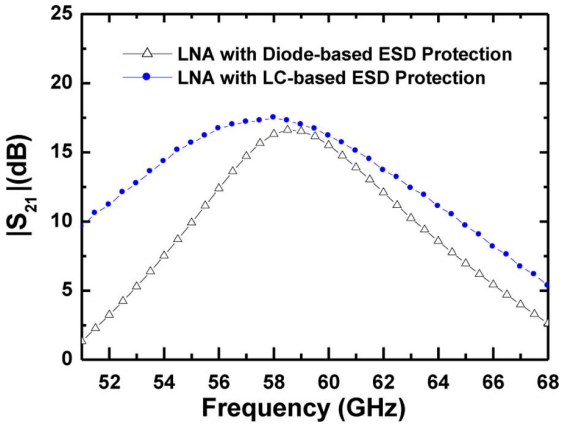

Fig. 11. Measured $|S_{21}|$ of the LNAs with diode-based and *LC*-based ESD protection.

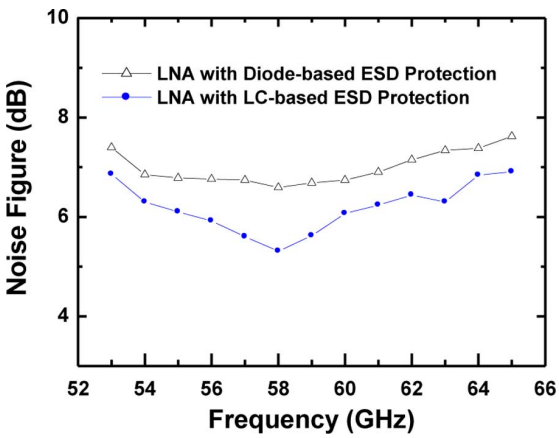

Fig. 12. Measured *NF* of the LNAs with diode-based and *LC*-based ESD protection.

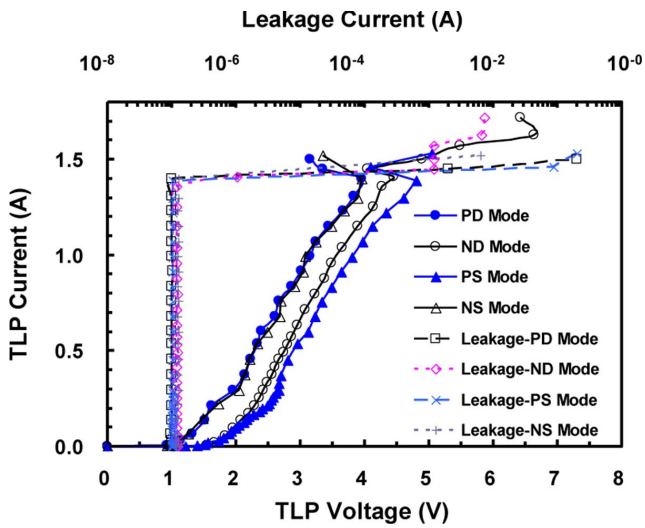

Fig. 13. Measured TLP *I–V* curves of the LNA with diode-based ESD protection.

A. RF Measurement Results

The RF characteristics of both LNAs were measured on-wafer using the Cascade G-S-G RF probes with a 100-μm pitch. The S-parameters and *NF* measurements were performed by the Agilent PNA network analyzer and Agilent 8975A noise figure analyzer, respectively. The first LNA operates from a 1.5-V supply voltage and draws a current of 18.6 mA with

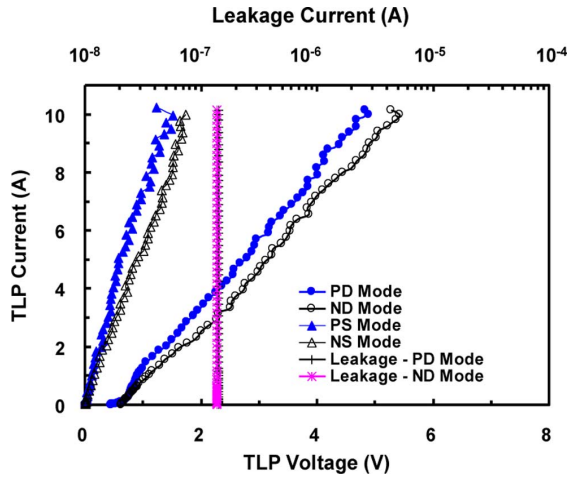

Fig. 14. Measured TLP *I–V* curves of the LNA with *LC*-based ESD protection.

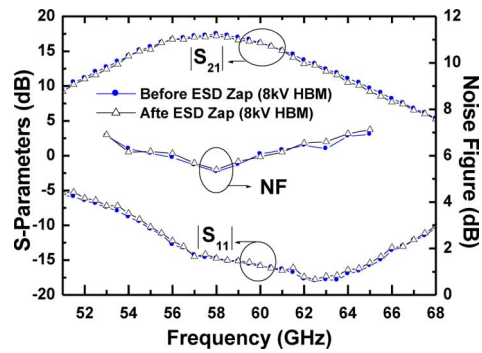

Fig. 15. Measured $|S_{11}|$, $|S_{21}|$, and *NF* of the LNA with *LC*-based ESD protection before/after ESD zap.

TABLE III
SUMMARY OF ESD TESTING RESULTS IN DIFFERENT MODES

TLP (A)/ VFTLP (A)	PD	PS	ND	NS
Diode-based ESD-LNA	1.4 / 1.8	1.4 / 1.9	1.4 / 1.9	1.4 / 2.1
LC-based ESD-LNA	10 / 13	10 / 14	10 / 13.6	10 / 14.2

*The TLP measurement is limited to 10 A by the TLP tester.

an associate dc power consumption of 27.9 mW. With the same supply voltage, the bias current is 12 mA and the power consumption is 18 mW for the second LNA. Figs. 10–12 compare the measured S_{11}, S_{21}, and *NF* of the LNAs using double-diode and *LC*-based ESD protection schemes, respectively. The diode-based design presents a peak power gain of 16.5 dB at 58.5 GHz, an input return loss greater than 21 dB at 59 GHz, and a minimum *NF* of 6.6 dB at 58 GHz. In contrast, the proposed *LC*-based design shows a peak power gain of 17.5 dB, an input return loss greater than 15 dB, and a minimum *NF* of only 5.3 dB all at 58 GHz. One distinct difference should be pointed out is that the second LNA has a much wider bandwidth regarding both input matching and gain, as can be seen in Figs. 10 and 11, respectively. The *LC*-based ESD configuration presents an input matching bandwidth up to $\sim$ 13 GHz ($|S_{11}| < -10$ dB, from 55 to 68 GHz) and a 3-dB power gain bandwidth up to $\sim$ 7 GHz (from 54.5 to 61.5 GHz). In contrast, the double-diode design only has the matching and

TABLE IV
PERFORMANCE COMPARISON OF THE PROPOSED LNAS WITH PRIOR WORKS

Ref.	This Work		[20]	[14]	[23]	[5]	[24]
Tech. (nm)	65		130	65	130	65	65
Freq. (GHz)	60		60	77	60	60	60
	Diode-based	LC-based					
NF (dB)	6.6	5.3	8.6	7.8	8.8	6.1	5.9
Power (mW)	27.9	18	65	37	54	35	30.8
S_{21} (dB)	16.5	17.5	20.4	10.5	12	22.3	15
S_{11} (dB)	-20	-15	-15	< -10	< -15	< -15	-10
HBM (kV)	2.0	> 8	6.5 / 1.5	4.05	--	--	--
TLP / VFTLP (A)	1.4 / 1.8	>10 / 13	--	--	--	--	--
Area (mm^2)	0.37	0.51	0.715	0.404	--	0.21	1.05
FOM^1	3.9	10.1	1.55	1.4	0.7	7.3	3.8
FOM^2	7.9	80.9	2.3	5.6	--	--	--

*HBM and TLP ESD levels are limited to 8 kV and 10 A by the ESD testers.

gain bandwidths of $\sim$2.5 and $\sim$ 4.5 GHz, respectively. The much improved bandwidth can be attributed to the multistage matching network consisted of $L_{\rm ESD}$, $C_{\rm ESD}$, L_{G1}, L_S, and the parasitic capacitances of M_1 in the *LC*-based design. In addition, the linearity of the LNAs was characterized by the two-tone test (58.5 and 58 GHz) for the third-order intermodulation. The measured *IIP3* are -10 and -11 dBm for the two LNAs at 58.5 and 58 GHz, respectively.

B. ESD Testing Results

The Barth Model 4002 TLP test system, which generates a pulse with a rise time of 10 ns along with a pulse width of 100 ns, was used for the on-wafer TLP characterization. Fig. 13 shows the TLP *I–V* characteristics of the diode-based ESD-protected LNA using the RF junction varactors. In the PD and NS modes, the ESD current goes through JV_T and JV_B, respectively (see Fig. 3). In contrast, the ESD current flows through both the diode and the power clamp in the PS and ND modes. As a result, an offset voltage appears compared with the PD and NS modes due to the additional voltage drop across the power clamp. In all four modes, the second breakdown current It_2 up to 1.4 A can be achieved, corresponding to about 2.0 kV HBM ESD level. The leakage currents are also monitored to quickly detect failure during ESD testing. Fig. 14 presents the measured TLP *I–V* characteristics of the *LC*-based ESD-protected LNA. With an It_2 over 10 A, the estimated ESD level is over 15 kV for PD and ND modes. Note the observed leakage current is mainly introduced from the power clamp, which is smaller than 1.5×10^{-6} A up to the measurement limitation of 10 A. For the PS and NS modes, the ESD network behaves like a short circuit due to $L_{\rm ESD}$ and the TLP current is conducted to the ground directly via $L_{\rm ESD}$ (see Fig. 6), and the leakage current cannot be monitored. Fig. 14 indicates that a lower voltage drop along the PS and NS modes under the same TLP current level, compared with the PD and ND modes. Although it is reasonable to claim that the PS and NS modes can also sustain an above 10-A TLP current, there is no direct evidence to support this point. To further exam the ESD protection capability of the LNA, a different testing equipment HANWA-W5100 is used to provide ESD zapping. The ESD protection level is verified by comparing the RF characteristics of the LNA before and after the ESD zapping. After applying an 8-kV ESD pulse (maximum value available from the equipment) to the LNA with the *LC*-based ESD design, the identical results verify that the ESD current has been successfully bypassed via $L_{\rm ESD}$ to the ground or $V_{\rm DD}$ without damaging the core circuit as shown in Fig. 15.

In addition to the typical HBM ESD tests, the charge-device-model (CDM) ESD event is also of great importance to the SOC chips [22]. The CDM event describes the self-discharge procedure of the charges accumulated in the substrate of ICs through a suddenly grounded pin. Compared with the HBM event, the CDM occurs at a much faster rising time, which makes the ESD protection more challenging. The HANWA HED-T5000 TLP test system was used for Very Fast TLP (VFTLP) characterization to investigate the CDM ESD protection capability. Compared with the typical TLP test, the rise time of VFTLP is shortened from 10 to 0.2 ns and the pulse width is reduced from 100 to 1 ns to meet the CDM pulse specifications given in the JEDEC standard. Table III summarizes the TLP and VFTLP measurement results of different pin combinations of the two LNAs. The *LC*-based ESD-protected LNA shows a substantially higher ESD protection level compared with the conventional double-diode design. Table IV summaries this work and compared with other previously published ESD-protected LNAs at *V*-band, where $\rm FOM^1$ and $\rm FOM^2$ (modified from [13]) are as follows:

$$\mathrm{FOM}^1 = \frac{\mathrm{Gain\,[abs]} \times \mathrm{f_C\,[GHz]}}{(\mathrm{NF}-1)\,[\mathrm{abs}] \times P_{\rm DC}\,[\mathrm{mW}]} \tag{3}$$

$$\mathrm{FOM}^2 = \frac{\mathrm{Gain\,[abs]} \times \mathrm{f_C\,[GHz]} \times \mathrm{ESD\,[kV]}}{(\mathrm{NF}-1)\,[\mathrm{abs}] \times P_{\rm DC}\,[\mathrm{mW}].} \tag{4}$$

With low noise, high gain, low power consumption, and high ESD protection level, the proposed *LC*-based ESD-protected LNA achieves state-of-the-art figure-of-merits.

V. CONCLUSION

In this paper, different ESD protection schemes were employed for two 60-GHz LNAs. The second LNA with the proposed *LC*-based ESD design presented significantly higher ESD levels with reduced noise figure, lowered power consumption, and also improved bandwidths, compared with the first design using the conventional double-diode ESD protection scheme. With a high current capability half-turn spiral inductor and a

high breakdown voltage MOM capacitor as effective bidirectional ESD protection, the LNA demonstrated an over 8-kV HBM ESD level and an over 13-A VFTLP current level for CDM ESD protection in 65 nm CMOS. By the ESD/matching codesign approach, the proposed LNA achieved a noise figure of 5.3 dB and a power gain of 17.5 dB, under a power consumption of only 18 mW. The achieved FoMs are among the best compared with prior works at similar operating frequencies.

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REFERENCES

[1] S. T. Choi, K. S. Yang, S. Nishi, S. Shimizu, K. Tokuda, and Y. H. Kim, "A 60-GHz point-to-multipoint millimeter-wave fiber-radio communication system," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 5, pp. 1953–1960, May 2006.

[2] D. Huang, R. Wong, Q. Gu, N. Wang, T. Ku, C. Chien, and M. C. Chang, "A 60 GHz CMOS differential receiver front-end using on-chip transformer for 1.2 volt operation with enhanced gain and linearity," in *Proc. VLSI Circuits Symp.*, Jun. 2006, pp. 144–145.

[3] B. Razavi, "A 60-GHz CMOS receiver front-end," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 17–22, Jan. 2006.

[4] S. Emami, C. H. Doan, A. M. Niknejad, and R. W. Brodersen, "A highly integrated 60 GHz CMOS front-end receiver," in *ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 190–191.

[5] C. Weyers, P. Mayr, J. W. Kunze, and U. Langmann, "A 22.3 dB voltage gain 6.1 dB NF 60 GHz LNA in 65 nm CMOS with differential output," *ISSCC Dig. Tech. Papers*, pp. 192–606, Feb. 2008.

[6] A. Z. H. Wang, *On-Chip ESD Protection for Integrated Circuits: An IC Design Perspective*. : Kluwer Academic, 2002.

[7] S. Voldman, *ESD: Circuits and Devices*. New York: Wiley, 2006.

[8] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, 2nd ed. London, U.K.: Wiley, 2002.

[9] M.-H. Tsai, S. Hsu, F. Hsueh, and C. Jou, "A multi-ESD-path low-noise amplifier with a 4.3-A TLP current level in 65-nm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 12, pp. 4004–4011, Dec. 2010.

[10] M.-H. Tsai, S. Hsu, F. Hsueh, and C. Jou, "ESD-protected K-band low-noise amplifiers using RF junction varactors in 65-nm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 12, pp. 3455–3462, Dec. 2011.

[11] M.-H. Tsai, S. Hsu, T. Yeh, C. Jou, and F. Hsueh, "A V-band low-noise amplifier with 5.3-dB NF and over 8-kV ESD protection in 65-nm RF CMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2012, pp. 1–3.

[12] P. Leroux and M. Steyaert, "High-performance 5.2 GHz LNA with on-chip inductor to provide ESD protection," *Electron. Lett.*, vol. 37, no. 7, pp. 467–469, 2001.

[13] D. Linten, S. Thijs, M. I. Natarajan, P. Wambacq, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Donnay, and S. Decoutere, "A 5-GHz fully integrated ESD-protected low-noise amplifier in 90 nm RF CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1434–1442, Jul. 2005.

[14] R. Berenguer, G. Liu, and Y. Xu, "A low power 77 GHz low noise amplifier with an area efficient RF-ESD protection in 65 nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 12, pp. 678–680, Dec. 2010.

[15] J. Borremans, S. Thijs, P. Wambacq, Y. Rolain, D. Linten, and M. Kuijk, "A fully integrated 7.3 kV HBM ESD-protected transformer-based 4.5–6 GHz CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 344–353, Feb. 2009.

[16] C. Lin, L. Chu, and M. Ker, "ESD protection design for 60-GHz LNA with inductor-triggered SCR in 65-nm CMOS process," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 3, pp. 714–723, Mar. 2012.

[17] K. Raczkowski, S. Thijs, J. Tseng, T. Chang, M. Song, D. Linten, B. Nauwelaers, and P. Wambacq, "60 GHz low noise amplifiers with 1 kV CDM protection in 40 nm LP CMOS," *Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pp. 16–18, Jan. 2012.

[18] K. Raczkowski, S. Thijs, W. Raedt, B. Nauwelaers, and P. Wambacq, "50-to-67 GHz ESD-protected power amplifiers in digital 45 nm LP CMOS," *ISSCC Dig. Tech. Papers*, pp. 382–383, Feb. 2009.

[19] Y. Li, J. J. Liou, J. E. Vinson, and L. Zhang, "Investigation of LOCOS-and polysilicon-bound diodes for robust electrostatic discharge (ESD) applications," *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 814–819, Apr. 2010.

[20] B. Huang, C. Wang, C. Chen, M. Lei, P. Huang, K. Lin, and H. Wang, "Design and analysis for a 60-GHz low-noise amplifier with RF ESD protection," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 2, pp. 298–305, Feb. 2009.

[21] W. Cho and S. Hsu, "An ultra-low-power 24 GHz low-noise amplifier using 0.13 m CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 12, pp. 681–683, Dec. 2010.

[22] M.-H. Tsai and S. Hsu, "A 24 GHz low-noise amplifier using RF junction varactors for noise optimization and CDM ESD protection in 90 nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 7, pp. 374–376, Jul. 2011.

[23] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.

[24] A. Natarajan, S. Nicolson, M. Tsai, and B. Floyd, "A 60 GHz variable-gain LNA in 65 nm CMOS," in *Proc. IEEE Asian Solid-State Circuit Conf.*, Nov. 2008, pp. 117–120.

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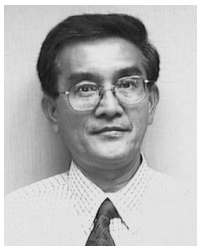

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