Power Performance of InP-Based Single and Double Heterojunction Bipolar Transistors

Donald Sawdai, *Student Member, IEEE,* Kyounghoon Yang, *Member, IEEE,*
Shawn S.-H. Hsu, Dimitris Pavlidis, *Fellow, IEEE,*
and George I. Haddad, *Life Fellow, IEEE*

***Abstract*— The microwave and power performance of fabricated InP-based single and double heterojunction bipolar transistors (HBT's) is presented. The single heterojunction bipolar transistors (SHBT's), which had a 5000-Å InGaAs collector, had $BV_{\rm CE0}$ of 7.2 V and $J_{C\,\rm max}$ of 2×10^5 A/cm^2. The resulting HBT's with 2×10 μm^2 emitters produced up to 1.1 mW/μm^2 at 8 GHz with efficiencies over 30%. Double heterojunction bipolar transistors (DHBT's) with a 3000-Å InP collector had a $BV_{\rm CE0}$ of 9 V and $J_{C\,\rm max}$ of 1.1×10^5 A/cm^2, resulting in power densities up to 1.9 mW/μm^2 at 8 GHz and a peak efficiency of 46%. Similar DHBT's with a 6000-Å InP collector had a higher $BV_{\rm CE0}$ of 18 V, but the $J_{C\,\rm max}$ decreased to 0.4×10^5 A/cm^2 due to current blocking at the base–collector junction. Although the 6000-Å InP collector provided higher $f_{\rm max}$ and gain than the 3000-Å collector, the lower $J_{C\,\rm max}$ reduced its maximum power density below that of the SHBT wafer. The impact on power performance of various device characteristics, such as knee voltage, breakdown voltage, and maximum current density, are analyzed and discussed.**

I. Introduction

POWER amplifiers for wireless communication systems require high-frequency active devices that have acceptable gain, produce significant output power, and cause little signal distortion. In addition, hand-held units require power amplifiers with high power-added efficiency (PAE) in order to maximize battery lifetime. Due to their ability to handle high power densities at microwave frequencies, heterojunction bipolar transistors (HBT's) operating linearly under Classes A and AB are good candidates for such amplifiers. While their breakdown voltages are typically not as high as GaAs-based HBT's, the excellent high-frequency performance and lower turn-on voltage of InP-based HBT's make them of interest for wireless applications.

The simplest InP-HBT designs use a single heterojunction between the emitter and base, with the base and collector both composed of InGaAs. However, the narrow-bandgap collectors in these single heterojunction bipolar transistors (SHBT's) limit the breakdown voltage below 10 V for typical collector thicknesses, and the maximum $V_{\rm CE}$, while conducting appreciable collector current, drops below 5 V. While this limited output voltage imposes limitations, output power levels up to 1.4 mW/μm^2 at 10 GHz have been reported by the authors using SHBT designs [1].

In order to increase the output voltage swing, InP is often used for the collectors of InP-based HBT's, which forms a second heterojunction with the InGaAs base. While breakdown voltages as high as 32 V [2] have been reported with these double heterojunction bipolar transistors (DHBT's), the base–collector heterojunction must be designed carefully to suppress collector current blocking due to conduction-band spikes. Published results on InP-based DHBT's include a tunneling InP collector [3], a linearly graded InGaAlAs junction [4], a step-graded InGaAsP junction [5], and linearly-graded chirped superlattices (CSL's) using either InGaAs/InP [6] or InGaAs/InAlAs [2]. Power densities as high as 3.5 mW/μm^2 (2.5 W total) with PAE of 56% at 9 GHz using the InGaAs/InAlAs CSL approach [2] have been reported by Hughes Research Laboratories, Malibu, CA. While more difficult to design, DHBT's with InP collectors offer an advantage over InGaAs–collector HBT's for power amplifiers. InP-based DHBT's offer similar power performance to GaAs-based HBT's at X-band; however, the 0.67-V lower turn-on voltage of InP-based HBT's decreases its power-supply requirements [7].

In this paper, we present issues and results on power amplification using InP-based HBT's and perform a comparative study of InP/InGaAs SHBT's and InP/InGaAs/InP CSL DHBT's in terms of their power capability. First, some issues for efficient linear power amplification are discussed. Then, device results are presented for both the SHBT's and the DHBT's used in this study. Finally, the results from power and load–pull measurements of both the SHBT's and DHBT's are presented and discussed, leading to conclusions regarding the merits of these SHBT's and DHBT's for power amplification.

II. Issues for Power Amplification in HBT's

In order to reduce the supply voltage for longer battery life, single-transistor output stages are common in power amplifiers for hand-held units. Due to the linearity requirements set by wireless modulation schemes such as QPSK, these output-stages usually employ Classes A or AB operation, operating

Manuscript received December 20, 1998; revised April 1999. This work was supported by the Army Research Office Multidisciplinary University Research Initiative under Contract DAAH04-96-1-0001.

D. Sawdai, S. S.-H. Hsu, D. Pavlidis, and G. I. Haddad are with the Solid-State Electronics Laboratory, Department of Electrical Engineering and Computer Science, The University of Michigan at Ann Arbor, Ann Arbor, MI 48109 USA.

K. Yang was with the Solid-State Electronics Laboratory, Department of Electrical Engineering and Computer Science, The University of Michigan at Ann Arbor, Ann Arbor, MI 48109 USA. He is now with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Taejon 305-701, Korea

Publisher Item Identifier S 0018-9480(99)06086-X.

at power levels that do not exceed the 1-dB gain compression point $(P_{O-1\,\mathrm{dB}})$.

In the first order, the maximum output power and efficiency of an HBT under Class A is limited by the breakdown voltage BV_{CE0}, the knee voltage V_k, the maximum collector current $I_{C\max}$, and the gain G. While it does not precisely scale with the HBT emitter area, $I_{C\max}$ increases with emitter area and can be approximated by $A \times J_{C\max}$ for this analysis, where $J_{C\max}$ is the maximum collector current density and is limited by the HBT design. Under these assumptions and neglecting HBT nonlinearity, maximum output power is generated by sweeping between V_k at $I_{C\max}$ and BV_{CE0} at $I_C = 0$, resulting in an optimal (real part of the) load impedance

$$R_L = \frac{BV_{\mathrm{CE0}} - V_k}{A \cdot J_{C\max}}. \tag{1}$$

The peak linear output power and efficiency can then be estimated as

$$P_L = \frac{A \cdot J_{C\max} \cdot (BV_{\mathrm{CE0}} - V_k)}{8} = 0.125\frac{(BV_{\mathrm{CE0}} - V_k)^2}{R_L} \tag{2}$$

and

$$\mathrm{PAE} = 0.5 \cdot \frac{BV_{\mathrm{CE0}} - V_k}{BV_{\mathrm{CE0}} + V_k}\left(1 - \frac{1}{G}\right). \tag{3}$$

Analogous expressions can be derived for Class-B operation, where the pre-factor in (2) is increased from 0.125 to 0.149, and the PAE expression has a similar form and peaks at 78% rather than 50%. Typically, the circuit technology limits the minimum R_L that can be synthesized for output matching, which then determines the maximum usable device area from (1). The peak output power and PAE are then limited by (2) and (3).

Since power HBT's need high P_L and PAE, this brief analysis indicates the required HBT characteristics: high G, high BV_{CE0}, and low V_k. High $J_{C\max}$ is also desired to reduce the required HBT area, which is limited by space, nonuniform heating, and signal phasing concerns. Note that the R_L presented here, which generates the most linear output power, is *not* directly related to the matched load impedance Z_L for the highest gain. Therefore, the actual load impedance presented to the HBT is chosen between this R_L and Z_L to trade off G, P_L, and PAE.

InP-based SHBT's and DHBT's each offer advantages for power amplifiers. Best reported values of some relevant parameters were compiled from a variety of different published HBT's and are shown in Table I. The higher BV_{CE0} primarily allows DHBT's to generate more output power than SHBT's, and the lower thermal resistance to the substrate due to the InP collector allows for lower and more uniform junction temperatures. The higher saturation velocity of the InP collector also allows for proportionally higher $J_{C\max}$ before the onset of the Kirk effect at a given collector doping. With emitter–base and base–collector compositional grading, the offset voltage and V_K are theoretically slightly smaller for DHBT's. The higher BV_{CEO} together with this lower V_K allows slightly higher efficiencies for DHBT's as compared to SHBT's. For example, by using (2) and (3) for Class-A operation together with the data in Table I and a system minimum R_L of 5 Ω, large DHBT's should be able to generate 25.2-W output power at 44% PAE, while similar SHBT's should generate 1.2-W output power at 42% PAE. Therefore, DHBT's are the best choice for high-power applications.

TABLE I
BEST REPORTED STATISTICS COMPILED FROM A VARIETY OF DIFFERENT InP-BASED MICROWAVE SHBTs AND DHBTs. THE BOTTOM TWO ROWS SHOW MATERIAL PARAMETERS FOR InGaAs (SHBT) AND InP (DHBT) COLLECTORS

	InP SHBTs	*InP DHBTs*
Highest f_T (GHz)	235	160
Highest f_{max} (GHz)	236	267
Offset voltage (V)	0.20	0.10
V_K @ 10^4 A/cm^2 (V)	0.30	0.25
Turn-on voltage @ 10^4 A/cm^2 (V)	0.7	0.7
BV_{CE0} (V)	7.6	32
P_{out} @ 10 GHz (mW/μm^2)	1.37	3.5
and associated gain (dB) @ P_{out}	11	10
v_{sat} of collector (cm/s)	6×10^6	9×10^6
Thermal conductivity of collector (W/cm-K)	0.05	0.68

However, the spike in the conduction band of DHBT's may limit $J_{C\max}$, may increase V_K, and may also limit the gain at low J_C, which can introduce additional nonlinearities to the output characteristics. Since SHBT's are also easier to design and grow than DHBT's, they may be more cost effective and a better choice for power amplifiers that only require moderate output power levels. This will be discussed and clarified more in Sections V and VI.

III. SHBT DESCRIPTION AND PERFORMANCE

The SHBT epilayers were grown by low-pressure metal–organic chemical vapor deposition (MOCVD) at The University of Michigan at Ann Arbor. It consisted of a 2000-Å undoped InP buffer on a semi-insulating InP substrate, a 5000-Å n$^+$ (2×10^{19} cm^{-3}) InGaAs subcollector layer, a 5000-Å n$^-$ (5×10^{16} cm^{-3}) InGaAs collector, a 600-Å p$^+$ (1.5×10^{19} cm^{-3}) InGaAs base, a 100-Å undoped InGaAs spacer, a 1500-Å n (5×10^{17} cm^{-3}) InP emitter, a 700-Å n$^+$ (2×10^{19} cm^{-3}) InP layer, and a 2000-Å n$^+$ (2×10^{19} cm^{-3}) InGaAs cap. The base employed the maximum achievable p-doping of InGaAs in this MOCVD using zinc, as determined by studies on zinc activation. The 600-Å base provided a good tradeoff between base transit time and base resistance, and the 100-Å undoped emitter–base spacer was employed to minimize zinc diffusion difficulties.

The SHBT's were fabricated using a self-aligned emitter process, which uses selective wet etches to produce a 0.2-μm base contact-to-emitter separation. The base–collector capacitance was minimized by using the base contact as a self-aligned etch mask for the base mesa. The emitter and collector ohmic contacts used nonalloyed Ti/Pt/Au metallization, and the base contact used Pt/Ti/Pt/Au metallization.

Typical I_C–V_{CE} characteristics for SHBT's with 2×10 μm^2 emitters are shown in Fig. 1. The devices had a dc

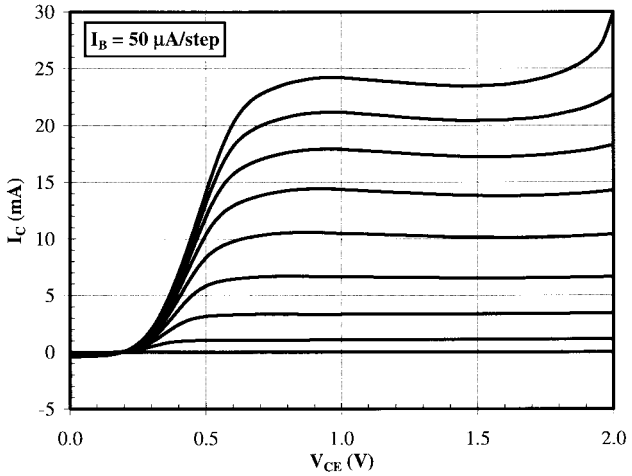

Fig. 1. I_C-$V_{\rm CE}$ characteristics of 2 × 10 μm^2 SHBT with I_B = 50 μA/step.

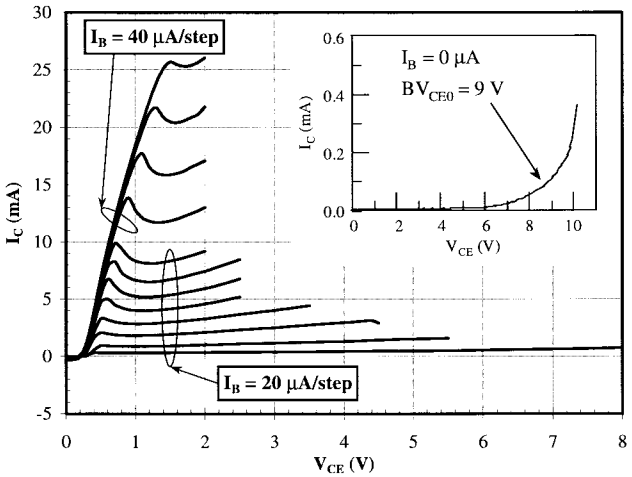

Fig. 2. I_C–$V_{\rm CE}$ characteristics of 2.5 × 10 μm^2 device from DHBT A with I_B = 20 or 40 μA/step.

small-signal gain $h_{fe} > 60$, and $n_b = 1.7$ and $n_c = 1.3$ from the Gummel plots. Although $BV_{\rm CE0}$ for large n-p-n HBT's was as high as 7.2 V, the maximum $V_{\rm CE}$ for $J_C > 5 \times 10^4$ A/cm^2 was approximately 2.5 V. Microwave performance measured up to 25.5 GHz and extrapolated at 20 dB/decade resulted in optimal f_T and matching f_{max} of 95 and 55 GHz, respectively, at $V_{\rm CE} = 1.5$ V and $I_C = 12.6$ mA. The f_{max} increased to 58 GHz when VCE was increased to 2.0 V. Although the peak f_T occurred at $J_C = 6.3 \times 10^4$ A/cm^2, the HBT's could be operated above $J_C = 2 \times 10^5$ A/cm^2, where the Kirk effect and high-level injection degraded f_T to 60 GHz and $f_{\rm max}$ to 37 GHz at $V_{\rm CE} = 1.7$ V. Further details on device performance can be found in an earlier report by the authors [1].

IV. DHBT Description and Performance

The InP/InGaAs DHBT epilayers were grown by chemical beam epitaxy (CBE) at The University of Michigan at Ann Arbor. They consisted of a 6000-Å n$^+$ (10^{19} cm^{-3}) InGaAs subcollector layer on a semi-insulating InP substrate, an n$^-$ (3×10^{16} cm^{-3}) InP collector, a base–collector grading region including a 10-period 500-Å n$^-$ (3×10^{16} cm^{-3}) InP/InGaAs CSL, a 600-Å p$^+$ (3×10^{19} cm^{-3}) InGaAs base, a 20-Å undoped InGaAs spacer, a 1500-Å n (5×10^{17} cm^{-3}) InP emitter, a 500-Å n$^+$ (10^{19} cm^{-3}) InP layer, and a 1000-Å n$^+$ (10^{19} cm^{-3}) InGaAs cap. Two heterostructures with different InP collector-layer thicknesses were grown: DHBT A with $W_C = 3000$ Å and DHBT B with $W_C = 6000$ Å. The overall base–collector junction design consists of the ten-period InGaAs/InP CSL, sandwiched by a 40-Å n-type delta-doped (4×10^{18} cm^{-3}) InP layer and a thin (20 Å) InGaAs undoped spacer. The InP delta-doped layer was inserted at the end of the CSL prior to the InP collector to suppress the quasi-electric field generated by the compositional grade. The thickness of the CSL InP layers was linearly increased from 5 Å at the interface of the base–collector junction to a thickness of 45 Å at the collector side with a period thickness of 50 Å. The beryllium-doped base was set to the maximum achievable doping with good material quality for this CBE. The DHBT's were fabricated using a similar process and layout to the SHBT's. The CSL structure was etched by either a reactive ion etch (RIE) or a nonselective wet etch [6].

The dc and small-signal device performance of the DHBT's were characterized from measured input/output *I–V* characteristics and bias-dependent S-parameters. Gummel plots of this DHBT had ideality factors of $n_b = 1.65$ and $n_c = 1.3$. Typical I_C-$V_{\rm CE}$ characteristics for a 2.5 × 10 μm^2 device from DHBT A are shown in Fig. 2. The current peaking at low $V_{\rm CE}$ has been attributed to coherent electron transport through some periods of the InGaAs/InP CSL [6], which is less pronounced than similar oscillatory I_C–$V_{\rm CE}$ behavior reported from an InGaAs/InAlAs CSL with 25-Å-thick periods [8]. The DHBT's demonstrated not only high breakdown voltages due to the use of a wide-bandgap InP collector, but also good injection properties because of the CSL grade design, which suppressed the current blocking effect occurring at the InP/InGaAs base–collector junction. The knee voltage was limited by slight current blocking at low $V_{\rm CE}$ and was almost identical to that reported for DHBT's with InGaAs/InAlAs CSL designs [9]. The current blocking could be reduced through the use of more superlattice layers with a thinner period in the CSL [8], which should allow very low knee voltages such as 0.6 V at 10^5 A/cm^2, as reported for a step-graded InGaAsP base–collector heterojunction [5].

The important performance parameters of the DHBT's with two different collector thicknesses are summarized and compared with the SHBT's in Table II. $BV_{\rm CE0}$ scales almost linearly with the thickness of the lightly doped InP collector and demonstrates approximately double that of SHBT's with similar collector thicknesses. Due to the thicker collector of DHBT B when compared to DHBT A, the larger τ_c reduced f_T by 23%, and the smaller $C_{\rm BC}$ increased $f_{\rm max}$ by 43%. The SHBT had a lower base doping and a slightly different lateral layout than the DHBT's, all of which contribute to a reduced τ_b, increased R_B, and increased $C_{\rm BC}$ for the SHBT. These effects resulted in the higher f_T and lower $f_{\rm max}$ of the SHBT. The base doping was low enough for all three wafers in

TABLE II
PERFORMANCE OF HBTs WITH $2 \times 10\ \mu m^2$ EMITTERS FABRICATED FROM THE SHBT AND BOTH DHBT WAFERS

	SHBT	*DHBT A*	*DHBT B*
W_C (Å):	5000	3000	6000
J_{Cmax} (10^5 A/cm^2)	2	1.1	0.4
β_{max}	70	90	55
BV_{bco} (V)	8.3	14	23
BV_{ceo} (V)	7.2	9	18
V_k (V)	0.7	1.3	1.5
Max. f_T (GHz)	95	92	71
Max. f_{max} (GHz)	58	102	146

which Auger recombination did not severely limit the current gain.

The injection performance improved when moving from DHBT B to A, which had higher $J_{C\max}$ and current gain with a slightly smaller knee voltage. This is because for a given base–collector reverse bias, the overall electric field across the base–collector junction and collector region is higher for the shorter collector, which suppresses the electron blocking at the base–collector heterojunction more effectively. In addition, the higher electric field in the shorter collector delays base push-out to higher current density. However, once base push-out occurs, the reduced electric field causes the base–collector heterojunction to start blocking electrons, causing the gain to drop rapidly for currents above $J_{C\max}$ on both DHBT wafers. In comparison, the absence of any heterojunction barrier at the base–collector interface of the SHBT reduced its knee voltage to 50% of that for the DHBT's. Similarly, due to the lack of barrier, the SHBT demonstrated only a slight decrease in gain as base push-out occurred, allowing it to operate at a thermally limited current density approximately twice that of the DHBT's. Since the SHBT and both DHBT wafers had similar emitter–base junction designs, all HBT's measured had fairly uniform gain versus collector current, which is required for linear amplifiers.

V. POWER CHARACTERIZATION

The power characteristics of both the SHBT's and DHBT's were measured on-wafer at 8 GHz using a source– and load–pull system developed in-house. The system uses dual FOCUS electromechanical tuners under computer control to synthesize source and load reflection factors up to 0.8 at the HBT's. For all measurements, the source and load impedances were simultaneously optimized for optimal gain at a fixed bias point and fixed level of input power. Then the input power was swept while maintaining constant $V_{\rm CE}$ and $V_{\rm BE}$ bias, and the output power and the HBT currents were measured.

The optimal bias points and source/load impedances for maximum output power from several SHBT's and one DHBT from each wafer are shown in Table III. Note that these conditions, which were slightly into Class-AB operation, indicate the best output power, but not the best gain or PAE performance of the HBT's. These HBT's were representative of all devices measured. While the HBT's presented here are all relatively small devices, which can generate only limited output power, previous power studies indicated that the X-band performance scales linearly from one to four identical emitter fingers and fairly well up to ten emitter fingers [1]. Additional difficulties encountered for very large HBT's include thermal management and matching of very small input and output impedances.

All HBT's were optimized for maximum output power under large-signal operation near the 1-dB gain compression point. Note that none of the HBT's could be operated at $V_{\rm CE}$ above $\sim 1/3 BV_{\rm CE0}$ without causing the HBT's to burn out at moderate-to-high collector currents, which forced the choice of low $V_{\rm CE}$ in Table III. Nevertheless, the higher breakdown voltages of the DHBT's allowed for a higher $V_{\rm CE}$ bias than for the SHBT's. Similarly, the collector bias current followed the trends for $J_{C\max}$ of the three wafers, with the SHBT wafer allowing the highest current density and DBHT B allowing the least. Note that as $P_{\rm in}$ increased, self-biasing caused I_C to increase much above the I_{C0} values listed in the table.

Table III also shows the peak gain, output power at 1-dB gain compression ($P_{O-1\,\rm dB}$), and associated PAE under these Class-AB bias points and source/load impedances. These values and the real part of Z_L roughly correspond to the Class-A predictions from the simplified expressions in (1)–(3). For example, the predicted Class-A maximum output power for SHBT 1 and DHBT B1 is 8.8 and 14.6 dBm, respectively. Similarly, the predicted Class A PAE for SHBT 1, DHBT A1, and DHBT B1 are 31%, 27%, and 34%. Analysis of these equations indicates that the PAE is mostly limited by the difference $(BV_{\rm CE0} - V_K)$: if V_K were reduced to 0, PAE would be 47%–49% (where the theoretical maximum is 50% for Class A). More realistic HBT optimizations could produce $V_K \sim 0.3$ V, which would result in PAE of 39%, 41%, and 45% for SHBT 1, DHBT A1, and DHBT B1, respectively. Further analysis indicated that larger HBT emitters (with correspondingly smaller load impedances) can be used to generate more output power, provided that gain does not degrade as the HBT area increases. Note that all of these HBT's were actually biased such that both the dc bias $V_{\rm CE}$ and the transient $v_{\rm CE}$ were significantly below $BV_{\rm CE0}$. For better accuracy in this case, $BV_{\rm CE0}$ in (1)–(3) was replaced by the peak transient $v_{\rm CE,max}$ as estimated from $V_{\rm CE}$ and V_k—i.e., $v_{\rm CE}(t) = V_{\rm CE} + v_O \sin(t)$, so that $v_{\rm CE,max} = V_{\rm CE} + (V_{\rm CE} - V_k)$.

The input–output power curves when tuned for maximum output power (conditions from Table III) are shown in Fig. 3. The higher $f_{\max}$ of HBT's on DHBT B allowed them to produce more gain at 8 GHz than on DHBT A for all HBT's measured. However, the same high $f_{\max}$ caused $K \ll 1$ for DHBT B at 8 GHz, making the optimal matching impedances $\Gamma > 0.8$ under small-signal operation. On the other hand, the optimal Γ_L under large-signal operation was smaller since operation occurs under full current and voltage swing, as partially determined by the dc load line of (1). This created a tradeoff in the optimal load impedance for either small- or large-signal operation for DHBT B. For example, Fig. 4 shows the load–pull characteristics of DHBT B1 at $V_{\rm CE} = 3.0$ V and $I_C = 1.2$ mA under small-signal excitation. As can be seen, the peak gain is 21.05 dB at $\Gamma_L = 0.800\angle 46°$, while

TABLE III
BIAS POINTS AND SOURCE/LOAD IMPEDANCES FOR MAXIMUM OUTPUT POWER UNDER LARGE-SIGNAL OPERATION FOR SEVERAL DEVICES FROM THE SHBT WAFER AND ONE DEVICE FROM EACH DHBT WAFER. GAIN AND PAE WHEN MATCHED FOR MAXIMUM OUTPUT POWER ARE ALSO LISTED

	SHBT 1	*SHBT 2*	*SHBT 3*	*DHBT A1*	*DHBT B1*
A_E (μm^2)	2×10	3×10	2f×3×10	2×10	3f×2×10
V_{CE} (V)	1.8	1.8	2.0	3.0	5.0
V_{BE} (V)	0.87	0.82	0.82	0.831	0.867
I_{C0} (mA)	7.34	9.39	15.12	7.2	7.2
I_{B0} (mA)	0.22	0.27	0.52	-	-
Opt. Γ_S	0.209∠114°	0.336∠135°	0.327∠155°	0.423∠158°	0.297∠143°
Opt. Γ_L	0.202∠143°	0.222∠165°	0.298∠-175°	0.577∠102°	0.518∠18°
Peak Gain (dB)	12.4	11.4	11.9	12.3	15.6
$P_{O\text{-}1dB}$ (dBm)	10.4	11.2	14.4	13.7	12.6
Peak PAE (%)	30	29	35	25	26

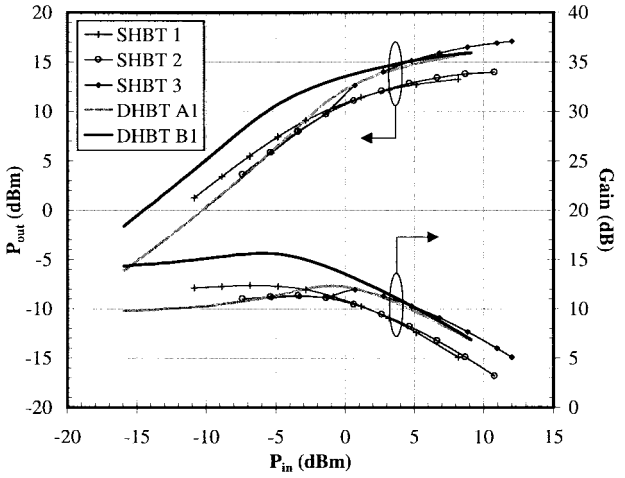

Fig. 3. Output power from the HBT's as a function of input power under the conditions shown in Table III.

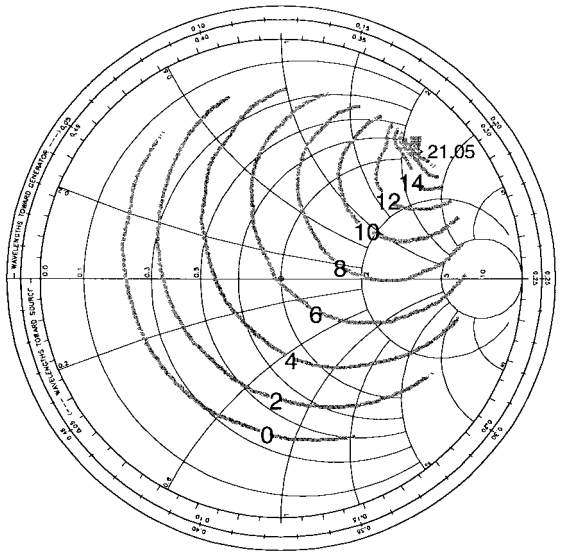

Fig. 4. Load–pull measurement of gain (in decibels) for $3f \times 2 \times 10$ μm^2 device from DHBT B at $P_{\rm in} = -19.1$ dBm. Peak gain is 21.05 dB at $\Gamma_L = 0.800\angle 46°$.

the gain is only 10 dB at $\Gamma_L = 0.518\angle 18°$ (i.e., maximum output power) from Table III. This results from the increase of optimum load impedance from $Z_{\rm SS} = 34 + j109\ \Omega$ at small signal to $Z_{\rm LS} = 129 + j57\ \Omega$ at large signal and from the resulting impedance mismatch when the device is terminated with $Z_{\rm LS}$, but is operated at small signal.

Unlike DHBT B1, the lower $f_{\max}$ of SHBT 1 permitted simultaneous source and load matching at small signal with $\Gamma_L = 0.521\angle 53°$. Even so, the effects of the dc characteristics caused the optimal Γ_L to move to $0.202\angle 143°$ under large-signal operation. The SHBT's demonstrated a smaller improvement in gain when optimized for small-signal operation; e.g., the peak gain for SHBT 1 when optimized for small-signal operation increased from 12.4 to 15.1 dB. The similar dc characteristics of DHBT A1 to SHBT1 caused similar variations with increasing input power: Γ_L moved from $0.527\angle 16°$ when tuned for maximum gain at small signal to $0.577\angle 102°$ when tuned for maximum output power at large signal. Overall, the thick-collector/high-$f_{\max}$ DHBT's manifest a larger difference between optimal impedance for small- and large-signal operation, while this is not the case for thin-collector/low-$f_{\max}$ DHBT's or SHBT's. Therefore, in order to optimize the design of a circuit that operates over a large range of input power, thick-collector DHBT's should be characterized over the whole range of input power. On the other hand, such circuits that operate over a large range of input power and employ thin-collector DHBT's or SHBT's manifest an output impedance which is more immune to variation at large-signal operation. This translates to circuit designs that are less dependent on the precise characterization and knowledge of the device large-signal properties.

An estimate of the power-handling capability of the various HBT's is presented in Table III by $P_{O-1\,\rm dB}$. As can be seen, $P_{O-1\,\rm dB}$ approximately scales with area for the SHBT's on the same wafer. DHBT A1 can handle approximately twice the power as the SHBT with the same area, mostly due to the higher collector voltage. However, the power output of DHBT B1 is limited by its low current-handling capability due to its lower peak electric field at the base–collector heterojunction (described in Section IV), which results in a lower $P_{O-1\,\rm dB}$ than that of DHBT A1. Even so, Fig. 3 demonstrates that

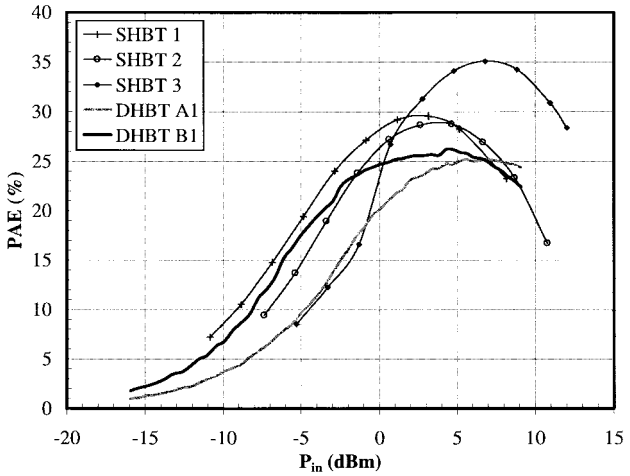

Fig. 5. PAE of the HBT's as a function of input power under the conditions shown in Table III.

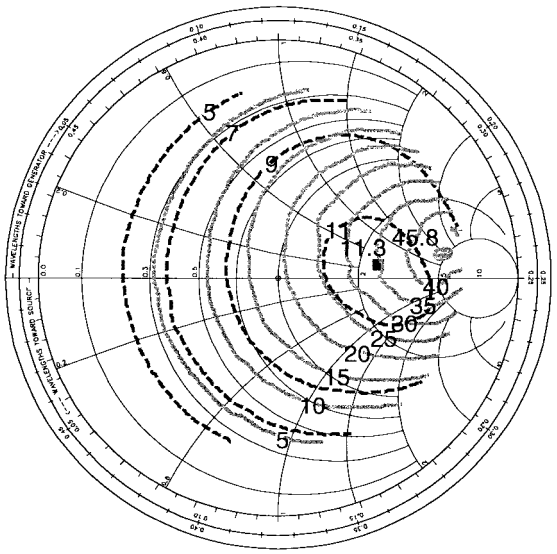

Fig. 6. Load–pull measurement of PAE (solid lines, in percent) and gain (dashed lines, in decibels) for 2×10 μm^2 device from DHBT A at $P_{\rm in} = 2.6$ dBm with I_B held constant. Peak PAE is 46% at $\Gamma_L = 0.694\angle 8°$. Peak gain is 11.4 dB at $\Gamma_L = 0.423\angle 5°$.

DHBT B1 produces more output power (but at a lower power density) than DHBT A1 at all input power levels. DHBT A1 and DHBT B1 produced maximum output powers of 15.85 and 15.94 dBm, respectively, resulting in output power densities of 1.9 and 0.65 mW/μm^2, respectively. The maximum power density of the 2×10 μm^2 SHBT, 1.1 mW/μm^2, was smaller than that of the same-area DHBT A1 due to the lower breakdown voltage of the SHBT. Thus, in determining the optimum design for maximum power, one should aim for designs such as thick-collector DHBT's that result in higher $BV_{\rm CE0}$ while, at the same time, ensuring that the current handling capability of the device is not handicapped. As shown by the results, a thinner collector DHBT is often a better tradeoff since its higher current density overcomes its smaller $BV_{\rm CE0}$ to allow a higher power density than thick-collector DHBT's. Also, SHBT's can deliver output power levels between that of thin- and thick-collector DHBT's. In the above considerations, however, one needs to take into account $f_{\rm max}$, which again gives thick-collector DHBT's the advantage in not only power performance, but also gain and frequency performance. Finally, when scaled up to very large areas for very high power applications, the higher $BV_{\rm CE0}$ of the thick-collector DHBT will give it a higher output impedance according to (1), which will alleviate the impedance-matching difficulties that often occur for large devices.

Fig. 5 shows the PAE for the HBT's under the conditions from Table III, and the maximum PAE values are shown in the table. Note that the bias and load impedance are optimized for maximum output power, which caused the measured PAE of these SHBT's to be higher than the DHBT's due to the decreased knee voltage. However, the higher breakdown voltage of the DHBT's compensates somewhat for the higher knee voltage, according to (3). As expected, the higher gain of DHBT's with thick collectors leads to earlier saturation and, thus, maximum PAE is obtained at a lower power density than both SHBT's and thin-collector DHBT's.

When the load impedance is optimized for maximum PAE, all HBT's demonstrate a substantial increase in PAE. For example, Fig. 6 shows the load–pull measurement for another 2×10 μm^2 HBT from DHBT A with $V_{\rm CE} = 3.0$ V and $\Gamma_S = 0.189\angle 103°$, which was optimized under large-signal operation near 1-dB gain compression with $V_{\rm CE}$ and I_B held constant. Note that this bias scheme pushed the operation deeper into Class AB. The peak PAE, 46%, occurred at $\Gamma_L = 0.694\angle 8°$ with an associated gain of 10.4 dB, while the peak gain of 11.4 dB occurred at $\Gamma_L = 0.423\angle 5°$ with an associated PAE of 34%. Thus, by trading off the device gain by 1 dB, one can benefit from a substantial improvement in PAE. Similar effects were shown by a 2×20 μm^2 HBT from the SHBT wafer, whose PAE increased from 27%, when matched for maximum output power, to 41% when matched for maximum PAE.

The load–pull characteristics of SHBT 1 is shown in Fig. 7 near 1-dB gain compression with $V_{\rm CE}$ and $V_{\rm BE}$ held constant. Similar to DHBT A in Fig. 6, the peak gain and peak PAE do not occur at the same impedance: the peak PAE, 34%, occurred at $\Gamma_L = 0.132\angle 165°$ with an associated gain of 11.2 dB, while the peak gain of 11.8 dB occurred at $\Gamma_L = 0.360\angle 130°$ with an associated PAE of 27%. Note that when compared to DHBT A, the PAE of SHBT 1 does not peak as high or drop off as quickly with load impedance variation, both of which can be attributed to the constant $V_{\rm BE}$ bias scheme. At high power levels, self-biasing under constant $V_{\rm BE}$ bias pushes HBT's toward Class-A operation with lower efficiency, but higher gain, while self-biasing under constant I_B bias pushes HBT's toward Class-AB operation with higher efficiency but lower gain, as described in [1].

VI. Discussion

All HBT's presented here demonstrated good power performance at 8 GHz. The SHBT's have good breakdown voltages and current handling, considering their InGaAs collector. However, the low $f_{\rm max}$ resulting from high base resistance and the partially depleted collector limits their microwave

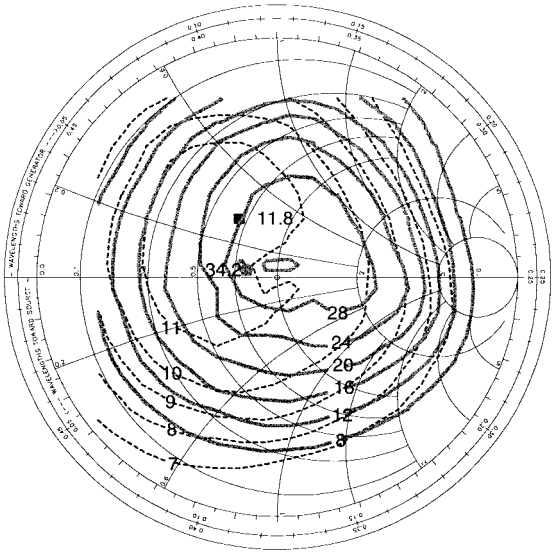

Fig. 7. Load–pull measurement of PAE (solid lines in percent) and gain (dashed lines, in decibels) for a 2×10 μm^2 SHBT at $P_{\rm in} = -2.5$ dBm with VBE held constant. Peak PAE is 34% at $\Gamma_L = 0.132\angle 165^\circ$. Peak gain is 11.8 dB at $\Gamma L = 0.360\angle 130^\circ$.

gain. Doubling the base doping, doubling the base thickness, increasing the collector thickness to 6000 Å, and reducing the collector doping to ensure full depletion would decrease these parasitics, which would raise $f_{\rm max}$ to 115 GHz at the expense of lowering f_T to 80 GHz. This would result in 3 dB more gain and 2% higher PAE for the SHBT's at X-band. The increased collector depletion width and reduced doping would also increase the breakdown voltage at the expense of lower current handling. Also, in order to enhance the PAE and maximum output power, the knee voltage could be reduced by optimizing the layers and contacts for reduced emitter and collector parasitic resistances. Together, the higher breakdown voltage and lower knee voltage could increase the PAE by 10%. Finally, SHBT designs with better thermal management would decrease thermal-generated current at high $V_{\rm CE}$, allowing for biasing above 2.0 V and closer to $BV_{\rm CE0}$.

While the DHBT power performance can be improved by many of the same optimizations as listed above for the SHBT's, more fundamental issues should be addressed to obtain the full potential power performance of the DHBT's. The two major power limitations on these DHBT's are the high knee voltage V_k and the low maximum current density $J_{C\,\rm max}$. Both are limited by transport of electrons over the barrier in the base–collector heterojunction. By introducing more layers in the CSL with a thinner period, the barrier could be lowered for decreased V_k and increased $J_{C\,\rm max}$. Modifications to the spacer/delta-doped layers between the CSL and the base–collector layers could lower the barrier further. Other possible enhancements are grading the emitter–base junction to remove the offset voltage of 0.15 V and optimizing the collector doping for the best $BV_{\rm CE0}/J_{C\,\rm max}$ tradeoff.

Finally, note that while the low $J_{C\,\rm max}$ of the DHBT's limits their power *density*, the first-order analysis of (2) and (3) demonstrates that the *absolute* output power and PAE are dependent on $BV_{\rm CE0}$ and not $J_{C\,\rm max}$ (for a fixed system-minimum R_L). Therefore, the higher breakdown voltage of the DHBT's should enable much greater output power than the SHBT's when scaled to very large emitters. For example, DHBT's with 33-layer CSL designs using 15-Å periods demonstrated the record output power density for InP-based HBT's of 3.5 mW/μm^2 at 56% PAE at X-band, which was achieved at $V_{\rm CE} = 14$ V and $J_C < 6 \times 10^4$ A/cm^2 [2].

VII. Conclusions

HBT's need to exhibit high gain, high breakdown voltage, low knee voltage, and high maximum collector current density in order to generate high output power at high efficiency under Class A and B operations. The SHBT's presented in this paper exhibited substantial power performance considering the use of an InGaAs collector. Power densities up to 1.1 mW/μm^2 at 8 GHz with efficiencies over 30% were measured. In order to increase their power performance, several minor optimizations, such as decreasing the collector doping and reducing parasitic resistances, can be made to increase the breakdown voltage and reduce the knee voltage.

The DHBT's presented here demonstrated significantly higher breakdown voltages than the SHBT's. However, current blocking at the base–collector junction at high current levels limited the $J_{C\,\rm max}$ of the DHBT's below that of the SHBT's. Along with much greater knee voltages than the SHBT's, the lower $J_{C\,\rm max}$ limited the improvement in power performance in the DHBT's to 1.9 mW/μm^2 with a peak efficiency of 46% for the DHBT with a 3000-Å collector. Although the DHBT's with a 6000-Å collector offered $\sim$3 dB more gain than the DHBT's with the 3000-Å collector due to the higher $f_{\rm max}$, the lower electric field in the collector enhanced the electron blocking at high current levels and limited its maximum power density below that of the SHBT wafer. In order to demonstrate the full power potential of InP-based DHBT's, the base–collector junction of these DHBT's needs to be further improved to increase the maximum collector current and decrease the knee voltage.

Additional power measurements on the HBT's indicate that the high $f_{\rm max}$ of the 6000-Å DHBT moves its optimal load impedances for gain, output power, and PAE further apart than corresponding optimal impedances for the 3000-Å DHBT or for the SHBT. Similarly, the optimal load impedance of the 6000-Å DHBT moves more due to variations in the input power level. This makes choosing the appropriate load impedance for circuit designs more difficult for the thick-collector DHBT. However, at the same time, the larger breakdown voltage of the thick-collector DHBT allows it to scale to larger areas than either the 3000-Å DHBT or for the SHBT before reducing the optimal load impedances to impractical values for matching.

The results presented here demonstrate the suitability of InP-based SHBT's for applications requiring up to moderate power levels and the potential of InP-based DHBT's for high-power applications.

Acknowledgment

The authors thank Dr. K. Hong for the growth of the SHBT wafers and Dr. G. Munns for the growth of the DHBT wafers.

REFERENCES

[1] D. Sawdai, J.-O. Plouchart, D. Pavlidis, A. Samelis, and K. Hong, "Power performance of InGaAs/InP single HBT's," in *8th Int. Conf. InP Related Mater.*, Apr. 1996, pp. 133–136.

[2] C. Nguyen, T. Liu, M. Chen, H.-C. Sun, and D. Rensch, "AlInAs/GaInAs/InP double heterojunction bipolar transistor with a novel base–collector design for power applications," *IEEE Electron Device Lett.*, vol. 17, pp. 133–135, Mar. 1996.

[3] J.-I. Song, B. Hong, C. Palmstrom, and K. Chough, "InP based carbon-doped base HBT technology: Its Recent Advances and Circuit Applications," in *6th Int. Conf. Indium Phosphide Related Mater.*, 1994, pp. 523–526.

[4] J. Cowles, L. Tran, T. Block, D. Streit, and A. Oki, "A 140 GHz $f_{\max}$ InAlAs/InGaAs pulse-doped InGaAlAs quaternary collector HBT with a 20 V BV_{CE0}," in *IEEE Device Res. Conf.*, 1995, pp. 84–85.

[5] S. Yamahata, K. Kurishima, H. Nakajima, T. Kobayashi, and Y. Matsuoka, "Ultra-high $f_{\max}$ and f_T InP/InGaAs double-heterojunction bipolar transistors with step-graded InGaAsP collector," in *GaAs IC Symp. Tech. Dig.*, 1994, pp. 345–348.

[6] K. Yang, G. O. Munns, and G. I. Haddad, "High $f_{\max}$ InP double heterojunction bipolar transistors with chirped InGaAs/InP superlattice base–collector junction grown by CBE," *IEEE Electron Device Lett.*, vol. 18, pp. 553–555, Nov. 1997.

[7] D. Streit, A. Gutierrez-Aitken, J. Cowles, L.-W. Yang, K. Kobayashi, L. Tran, T. Block, and A. Oki, "Production and commercial insertion of InP HBT integrated circuits," in *19th Annu. GaAs IC Symp. Dig.*, 1997, pp. 135–138.

[8] C. Nguyen, T. Liu, M. Chen, and R. Virk, "Bandgap engineered InP-based power double-heterojunction bipolar transistors," in *9th Int. Conf. InP Related Mater.*, 1997, pp. 15–19.

[9] T. Liu, M. Chen, C. Nguyen, and R. Virk, "InP-based DHBT with 90% power-added efficiency and 1 W output power at 2 GHz," *Solid State Electron.*, vol. 41, pp. 1681–1686, 1997.

Donald Sawdai (S'91), for photograph and biography, see this issue, p. 1446.

Kyounghoon Yang (S'90–M'92) received the B.S. and M.S. degrees in electronic engineering from Seoul National University, Seoul, Korea, in 1984 and 1986, respectively, and the Ph.D. degree in electrical engineering from The University of Michigan at Ann Arbor, in 1994.

He worked as a Post-Doctoral Research Fellow from 1994 to 1995 and, from 1995, as an Assistant Research Scientist in the Solid-State Electronics Laboratory, Department of Electrical Engineering and Computer Science, The University of Michigan at Ann Arbor, where he was engaged in research on compound semiconductor heterojunction devices, microwave power amplifiers, and high-speed optoelectronic devices and integrated circuits. His research interests include the fabrication, modeling, and characterization of high-speed semiconductor devices and their integration into microwave/millimeter-wave and optoelectronic integrated circuits. In 1999, he joined the faculty of the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Taejon, Korea.

Dr. Yang is a member of the IEEE Electron Devices, IEEE Microwave Theory and Techniques, and IEEE Lasers and Electro-Optics Societies.

Shawn S.-H. Hsu, photograph and biography not available at the time of publication.

Dimitris Pavlidis (S'73–M'76–SM'83–F'93), for photograph and biography, see this issue, p. 1448.

George I. Haddad (S'57–M'61–SM'66–F'72–LF'97), for photograph and biography, see this issue, p. 1432.