A Compact 0.1–14-GHz Ultra-Wideband Low-Noise Amplifier in 0.13-μm CMOS

Po-Yu Chang and Shawn S. H. Hsu, *Member, IEEE*

***Abstract*—A compact ultra-wideband low-noise amplifier (LNA) with a 12.4-dB maximum gain, a 2.7-dB minimum noise figure (NF), and a bandwidth over 0.1–14 GHz is realized in a 0.13-μm CMOS technology. The circuit is basically an inductorless configuration using the resistive-feedback and current-reuse techniques for wideband and high-gain characteristics. It was found that a small inductor of only 0.4 nH can greatly improve the circuit performance, which enhances the bandwidth by 23%, and reduces the NF by 0.94 dB (at 10.6 GHz), while only consuming an additional area of 80 $\times$ 80 μm^2. The LNA only occupies a core area of 0.031 mm^2, and consumes 14.4 mW from a 1.8-V supply.**

***Index Terms*—CMOS, current reuse, inductorless, low-noise amplifier (LNA), resistive feedback, ultra-wideband (UWB).**

I. Introduction

In RECENT years, for the demand of short-range (within 10 m) and high data-rate (up to 480 Mb/s) wireless communications, the standard of ultra-wideband (UWB) was set up by the Federal Communications Commission (FCC) in 2002. The FCC authorized the unlicensed 7.5-GHz band (3.1–10.6 GHz) for UWB applications. Motivated by implementing the transceivers with low cost and a high integration level, CMOS technology becomes the most attractive candidate. Owing to the rapid progress of CMOS technology, many studies of CMOS RF integrated circuits (RFICs) for UWB applications were published in succession with good results [1]–[6].

In an UWB receiver, the low-noise amplifier (LNA) with a wideband operation capability is critical to the overall receiver performance. The bandwidth of the LNA is ultimately limited by the parasitic capacitances of the devices. Two techniques for extending the bandwidth are commonly used to design UWB LNAs in CMOS technology, namely, the inductive peaking techniques [1]–[3] and the distributed amplifier (DA) topology [5]. LNAs based on the two techniques were both reported with adequate bandwidth for UWB applications. However, one drawback is that the design usually employs many spiral inductors, which occupy a large chip area.

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The authors are with the Department of Electrical Engineering and Institute of Electronics Engineering, National Tsing Hua University, Hsinchu 300, Taiwan (e-mail: g9561574@oz.nthu.edu.tw; shhsu@ee.nthu.edu.tw).

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Recently, inductorless design for wideband LNAs in CMOS technology attracts much attention because of the considerably reduced chip area. Various approaches were proposed for wideband LNA design without using any inductors [7]–[12]. The noise-canceling technique was adopted [7]–[9], which sensed the dominant noise source and canceled it by an auxiliary out-of-phase forward path to lower the noise figure (NF). However, the phase error becomes difficult to predict, and the noise cancellation is not as effective at high frequencies. The resistive-feedback technique was also reported [10]–[12]. With a large enough input transconductance, the resistive-feedback LNA can achieve several gigahertz of bandwidth, over 10-dB gain, and less than 3-dB NF, but usually under a large bias current [10] or with a more advanced technology [12] needed. To lower the power consumption, the current-reuse technique is employed to enhance the input transconductance [11].

In this study, a compact UWB LNA in 0.13-μm CMOS technology is proposed. Based on the concept of inductorless design, the amplifier includes a resistive-feedback configuration and a current-reuse input stage. One small inductor of only 0.4 nH is employed at the most critical node, namely, the gate of the input stage of the LNA to enhance the bandwidth and lower the NF simultaneously. Compared with the circuit without the inductor, the bandwidth is increased by 23% and the NF is reduced by 0.94 dB (at 10.6 GHz) with an additional area of only 80 $\times$ 80 μm^2. The proposed LNA achieves a wide enough bandwidth to cover the whole 3.1–10.6-GHz frequency range, a 12.4-dB maximum gain, and a 2.7-dB minimum NF with a 0.031 mm^2 core area under a 14.4-mW power consumption.

This paper is organized as follows. Section II analyzes the design techniques in this study including resistive feedback and gate inductive peaking. Section III discusses the amplifier design in detail. Section IV presents the measured results. Finally, Section V concludes this study.

II. Techniques of UWB LNA Design

A. Resistive Feedback

Feedback is a common technique to design wideband amplifiers. Shown in Fig. 1 is the common-source amplifier with a resistive feedback. In this configuration, the NF and input matching are generally a tradeoff [7], [12]. The tradeoff can be alleviated with a voltage buffer inserted in the feedback path, as shown in Fig. 2(a). Theoretically, the NF in this topology can be lowered by increasing the transconductance g_m of the transistor [7], [12], and the matching condition can be maintained by designing the feedback resistor R_f and the load R_L appropriately. A source follower is commonly used to implement the voltage

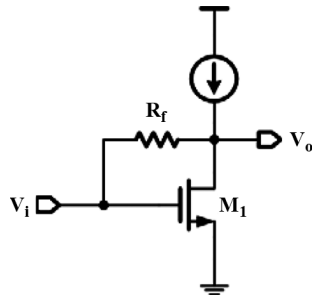


Fig. 1. Common-source amplifier with resistive feedback.

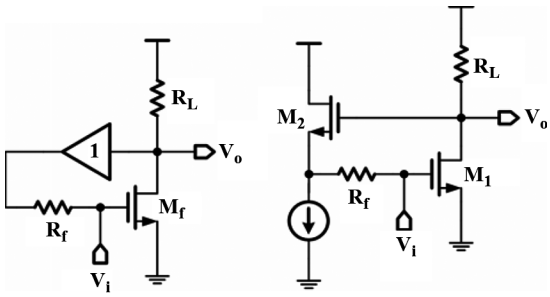


Fig. 2. Resistive-feedback amplifiers with: (a) an ideal voltage buffer and (b) a source follower buffer in the feedback path.

buffer, as indicated in Fig. 2(b). The voltage gain A_v of the amplifier in Fig. 2(b) can be derived as (1), shown at the bottom of this page, where g_{m1} is the transconductance of M_1, g_{m2} is that for the buffer stage M_2, and C_L represents the equivalent input capacitance of the following stage. If $R_L C_L \gg C_{\mathrm{gs2}}/g_{m2}$, and R_f and R_L are with similar values, A_v can be simplified as

$$\begin{aligned} A_v &\approx -\frac{g_{m1}R_L\left[1+s\left(\frac{C_{\mathrm{gs2}}}{g_{m2}}\right)\right]}{[1+sR_LC_L]\left[1+\frac{sR_LC_L\left(\frac{C_{\mathrm{gs2}}}{g_{m2}}\right)}{R_LC_L}\right]} \\ &= -\frac{g_{m1}R_L}{1+sR_LC_L} \\ &= -\frac{g_{m1}R_L}{1+j\omega R_LC_L}. \end{aligned} \tag{2}$$

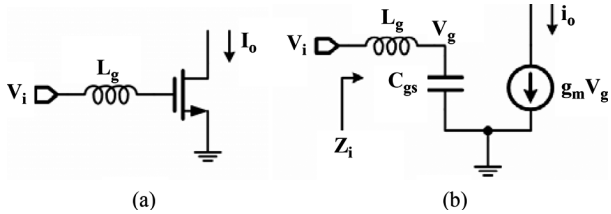


Fig. 3. (a) Common-source amplifier with a gate inductor. (b) Small-signal model of (a).

Equation (2) shows that this amplifier can be approximated as a single-pole system. The input impedance Z_{in} can also be calculated as

$$\begin{aligned} Z_{\mathrm{in}} &\approx \frac{1}{sC_{\mathrm{gs1}}}\left\|\frac{R_f}{g_{m1}R_L}\frac{1+sR_LC_L}{1+s\left(\frac{C_L}{g_{m1}}\right)}\right. \\ &= \frac{R_f}{g_{m_1}R_L}\frac{1+sR_LC_L}{1+s\frac{C_{\mathrm{gs1}}R_f+C_LR_L}{g_{m1}R_L}+s^2\left(\frac{C_{\mathrm{gs1}}C_LR_f}{g_{m1}}\right)} \\ &= \frac{R_f}{g_{m_1}R_L}\frac{1+j\omega R_LC_L}{1+j\omega\frac{C_{\mathrm{gs1}}R_f+C_LR_L}{g_{m1}R_L}-\omega^2\left(\frac{C_{\mathrm{gs1}}C_LR_f}{g_{m1}}\right)}. \end{aligned} \tag{3}$$

For wideband applications, the low-frequency input impedance $R_f/g_{m1}R_L$ is designed to be R_S ($50\,\Omega$ in most cases) for input matching. As can be seen from (3), the frequency response of Z_{in} contains one zero and two poles. If the parasitic capacitances are small, the poles and zero will locate at high frequencies, and thus a wideband matching is possible. However, good input matching near the 3-dB frequency is not easy to be achieved in practical design [10], [11].

B. Inductive Peaking

Fig. 3(a) shows a common-source stage with a gate inductor L_g, and Fig. 3(b) is the corresponding small-signal model. The voltage signal v_g at the gate can be expressed as

$$v_g = \frac{\left(\frac{1}{j\omega C_{\mathrm{gs}}}\right)v_i}{j\omega L_g+\frac{1}{j\omega C_{\mathrm{gs}}}} = \frac{v_i}{1-\omega^2L_gC_{\mathrm{gs}}}. \tag{4}$$

$$\begin{aligned} A_v &= \frac{v_o}{v_i} \\ &\approx -\frac{g_{m1}R_L\left[1+s\left(\frac{C_{\mathrm{gs2}}}{g_{m2}}\right)\right]}{1+s\left[R_LC_L+\left(\frac{C_{\mathrm{gs2}}}{g_{m2}}\right)\left(1+\frac{R_L}{R_f}\right)\right]+s^2R_LC_L\left(\frac{C_{\mathrm{gs}}}{g_{m2}}\right)} \\ &\approx -\frac{g_{m1}R_L\left[1+s\left(\frac{C_{\mathrm{gs2}}}{g_{m2}}\right)\right]}{\left\{1+s\left[R_LC_L+\left(\frac{C_{\mathrm{gs2}}}{g_{m2}}\right)\left(1+\frac{R_L}{R_f}\right)\right]\right\}\left\{1+s\frac{R_LC_L\left(\frac{C_{\mathrm{gs}}}{g_{m2}}\right)}{\left[R_LC_L+\left(\frac{g_{\mathrm{gs2}}}{g_{m2}}\right)\left(1+\frac{R_L}{R_f}\right)\right]}\right\}} \end{aligned} \tag{1}$$

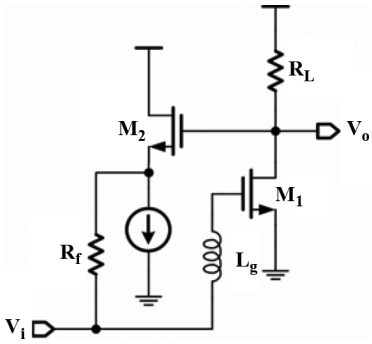


Fig. 4. Resistive-feedback amplifier with a gate inductor connected to the input stage.

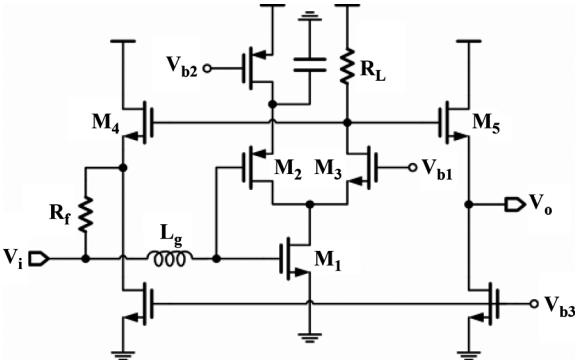


Fig. 5. Circuit schematic of the proposed compact UWB LNA.

Therefore, the output current induced by v_g is

$$i_o = g_m v_g = \frac{g_m v_i}{1-\omega^2 L_g C_{\rm gs}}. \tag{5}$$

From (5), we obtain the equivalent transconductance of this configuration

$$G_m = \frac{i_o}{v_i} = \frac{g_m}{1-\omega^2 L_g C_{\rm gs}}. \tag{6}$$

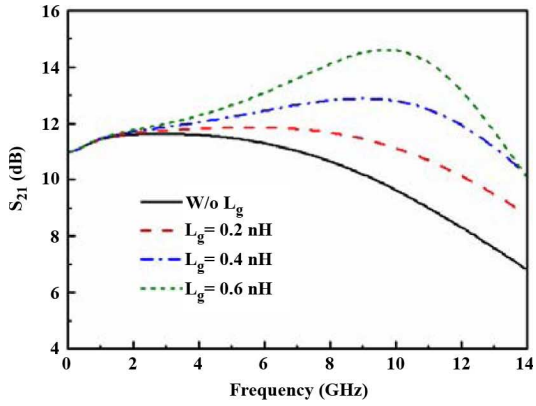
Equation (6) indicates that G_m increases with frequency when the operation is below the resonance of L_g and $C_{\rm gs}$. The input-referred noise sources can be expressed as

$$\overline{v_{n,i}^2} = \frac{\overline{i_{n,Id}^2}}{G_m^2} = \frac{4kT\gamma}{g_m}(1-\omega^2 L_g C_{\rm gs})^2 \Delta f \tag{7}$$

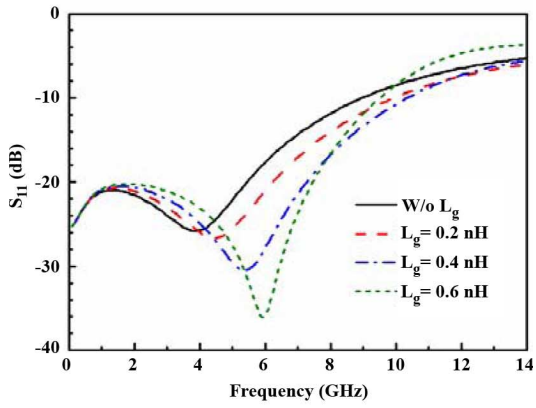
and

$$\overline{i_{n,i}^2} = \frac{\overline{i_{n,Id}^2}}{G_m^2 Z_i^2} = \frac{4kT\gamma}{g_m}\omega^2 C_{\rm gs}^2 \Delta f \tag{8}$$

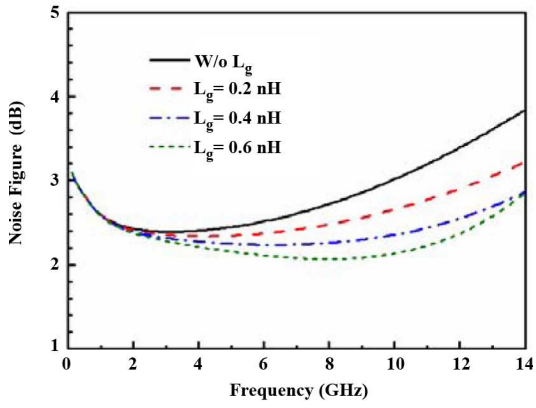
where k is the Boltzmann's constant, T is the absolute temperature, Δf is the noise bandwidth, and γ is the thermal excess noise factor, which is ~2/3 in a saturated long channel device [13]. Note that γ increases as the channel length scales down. Equation (7) indicates that $\overline{v_{n,i}^2}$ decreases with frequency, while it is independent of frequency if L_g is not considered. Obtained from (8), $\overline{i_{n,i}^2}$ is identical to that without L_g. As a result, the total input-referred noise can be suppressed at high frequencies with the gate inductor in a common-source topology.



(a)



(b)



(c)

Fig. 6. Simulated: (a) S_{21}, (b) S_{11}, and (c) NF with different L_g.

C. Resistive-Feedback LNA With Gate-Inductor Peaking

Fig. 4 shows the resistive-feedback design through a source follower with the gate-inductor peaking [14]. The voltage gain can be calculated by replacing g_{m1} in (2) with the equivalent transconductance G_{m1}, as obtained in (6). Therefore,

$$\begin{aligned} A_v &\approx -\frac{G_{m1}R_L}{1+j\omega R_L C_L} \\ &= -\frac{\left[\frac{g_{m1}}{(1-\omega^2 L_g C_{\rm gs1})}\right] R_L}{1+j\omega R_L C_L} \\ &= -\frac{g_{m1}R_L}{(1-\omega^2 L_g C_{\rm gs1})(1+j\omega R_L C_L)}. \end{aligned} \tag{9}$$

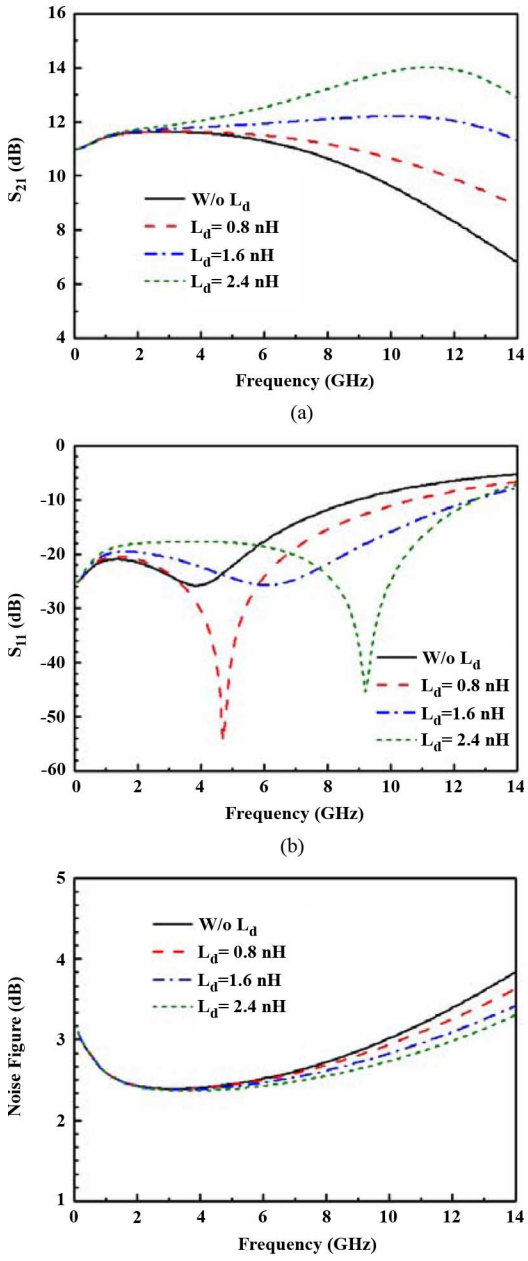


Fig. 7. Simulated: (a) S_{21}, (b) S_{11}, and (c) NF with different L_d.

Since $(1-\omega^2 L_g C_{\rm gs1})$ decreases with frequency, the gain reduction due to the pole can be compensated, and thus the bandwidth is enhanced. The analytical equations of $Z_{\rm in}$ and NF are rather complicated, do not provide intuitive guidance, and are not shown here. For the following analysis, Agilent Technologies' Advanced Design System (ADS) is employed to provide quantitative explanation and also observe the tradeoffs between different design considerations such as NF, gain, and circuit stability. In practical design, the input impedance for wideband matching is mainly determined by L_g and $C_{\rm gs}$ of $\rm M_1$. For high gain and low noise design, it is required to have a large input transconductance, and thus a large $\rm M_1$ is preferred. However, a large $\rm M_1$ is associated with large parasitic capacitances, which can degrade the matching and gain characteristics at high frequencies. For example, $\rm M_1$ with a total channel width of 200 μm

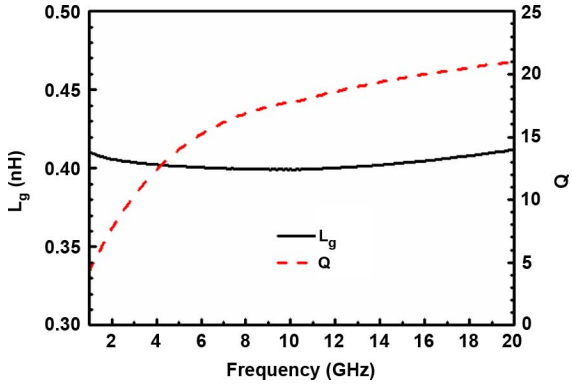


Fig. 8. Simulated inductance and Q of the gate inductor L_g.

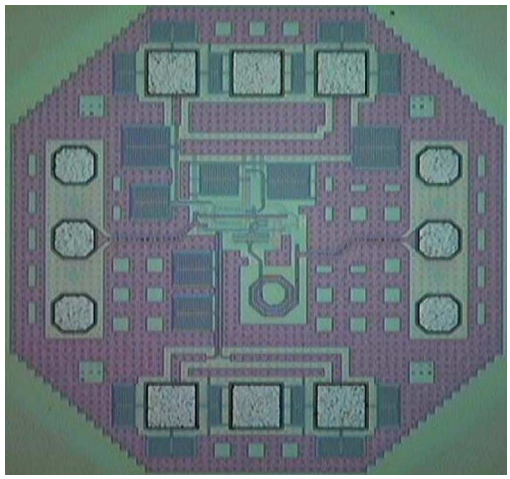


Fig. 9. Chip micrograph of the proposed LNA.

(0.13-μm NMOS) has a large g_m of $\sim$ 100 mA/V (under a drain current of 10 mA), but also with a large $C_{\rm gs}$ of $\sim$ 300 fF. Note that the effective gate–source capacitance would be even larger if considering the Miller effect. On the contrary, if $\rm M_1$ is too small (associated with a small $C_{\rm gs}$), a large enough transconductance cannot be obtained, and a large L_g is needed to have a suitable resonant frequency for bandwidth enhancement. It can be estimated that a relatively large peaking inductor L_g of $\sim$ 0.8 nH is needed for a 60-μm $\rm M_1$ based on the circuit topology in Fig. 4 for the desired UWB applications. The size selection of $\rm M_1$ plays a critical role in this configuration and more discussion will be carried out with the proposed topology.

For noise considerations, the main noise contributor is the first-stage transistor $\rm M_1$. Since an ideal feedback network has no impact on the circuit noise performance [15], it is expected that the NF has a similar trend with that of the gate peaking design shown in Fig. 3(a), i.e., the inductor can suppress the high-frequency noise, as will be illustrated in Section III.

III. Design of Compact UWB LNA

A. Circuit Topology

Fig. 5 shows the circuit schematic of the proposed compact UWB LNA, which includes a cascode amplifier with a current-reuse input stage, a source follower as the feedback buffer, a feedback resistor, a gate peaking inductor, and another

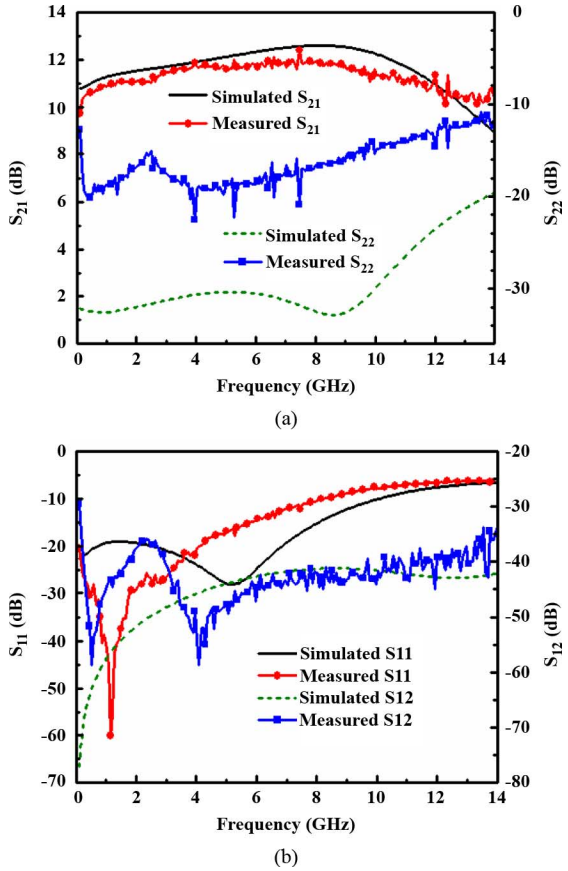


Fig. 10. Measured S-parameters. (a) S_{21} and S_{22}. (b) S_{11} and S_{12}.

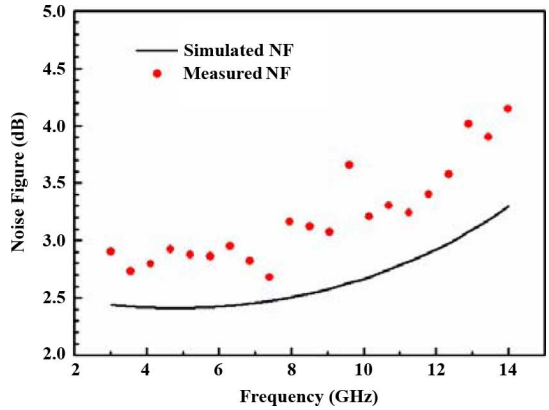


Fig. 11. Measured NF.

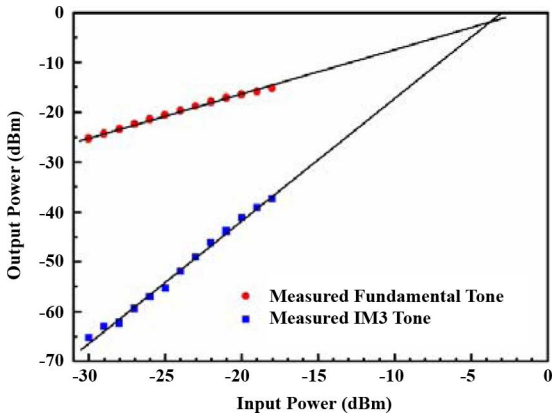


Fig. 12. Measured IIP3 at 6 GHz.

source follower for the output buffer. The cascode amplifier includes three transistors, i.e., M_1, M_2, and M_3. The two common-source transistors M_1 (NMOS) and M_2 (PMOS) are arranged as a current-reuse topology, and the transistor M_3 functions as the common-gate stage of the cascode topology. In the current-reuse design, the overall transconductance is the sum of both transistors. The enhanced transconductance allows high-gain performance under low power consumption. Note that the bias current of M_3 is only part of the current of M_1, and the voltage drop of R_L is reduced, leading to increased output headroom.

In this configuration, the input transconductance stage (M_1 and M_2) first converts the input voltage to a current signal, which then flows through M_3 to the load R_L as the output signal. The amplified signal is also fed back to the input through the feedback buffer M_4 (source follower) and the feedback resistor R_f. As described in Section II, L_g is resonated with the gate capacitances of M_1 and M_2. As a result, the voltage signal at the gate of $\mathrm{M}_1(\mathrm{M}_2)$, and thus the equivalent transconductance, both increase rapidly when the operation approaches the resonant frequency.

The transistor size and bias condition of M_1 and M_2 are critical for achieving high gain and low noise in this design. For the input transconductance, M_1 is more important than M_2 since M_1 is an NMOS and also with a larger bias current than that of M_2. The total width of transistor M_1 is chosen as 96 μm to have sufficient transconductance and low noise. Both M_1 and M_2 contribute to the gate capacitance of the input stage, and thus affect the resonant frequency for bandwidth extension. With the current-reuse design, the transistor M_2 can not only enhance the transconductance, but also provide the flexibility to optimize the input equivalent capacitance. The transistor M_2 contributes additional capacitance allowing a small gate peaking inductor while maintaining an appropriate resonant frequency for bandwidth extension. The M_2 transistor selected for this design has a width of 64 μm.

B. Design of Gate Inductor

The peaking inductor L_g is determined by considering the resonant frequency with the combined input capacitance contributed of M_1 and M_2. The input capacitances of M_1 and M_2 can be extracted from the foundry provided device model to estimate the required value of L_g. With a desired bandwidth up to 10.6 GHz, the LC resonant frequency should be higher than this frequency to ensure stable circuit operation. L_g can be estimated to be in the order of 0.3 $\sim$ 0.4 nH to create a resonant frequency at about 14 $\sim$ 16 GHz. Fig. 6 shows the simulated S_{21}, S_{11} and NF versus frequency with different L_g. Note that the results shown here are based on electromagnetic (EM) simulated spiral inductors for more precise prediction. The 3-dB circuit bandwidth is enhanced from 11.5 GHz (without any inductor) to 14.2 GHz ($\sim 23\%$) with a gate inductor of 0.4 nH. An improved input matching can also be obtained. Moreover,

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ARTS

	[4]	[5]	[9]	[16]	This Work
Technology	0.13 μm CMOS	0.13 μm CMOS	0.13 μm CMOS	0.13 μm CMOS	0.13 μm CMOS
Frequency (GHz)	3.1–10.6	1–10.6	2–9.6	3–11	3.1–10.6
Supply Voltage (V)	1.2	1	1.5	1.3	1.8
Power (mW)	9	26	19	2.4	14.4
S_{11} (dB)	< -9.9	< -12	< -8.3	< -7.5	< -7.3
Max. Gain (dB)	16.5	16	11	10	12.4
–3 dB Bandwidth (GHz)	~ 9	~ 12	7.6	8	> 13.9 [(2)]
Noise Figure (dB)	2–2.8	2.3–4.5	3.6–4.8	2.9–3.6	2.7–3.7
IIP3 (dBm)	-5.1	2	-7.2	9.5	-3.8
Num. of Coils	3	17	0	2	1
Core Area (mm^2)	~ 0.33	0.268	0.05	0.134	0.031 [(1)]
FOM (GHz/(mW · mm^2))	27.2	8.7	17.2	70.2	119.4

[(1)] Including the output buffer.
[(2)] 3dB bandwidth exceeds the measured frequency range (0.1–14 GHz).

the NF is reduced by 0.94 dB at 10.6 GHz. For the proposed resistive-feedback amplifier peaking with a gate inductor, the gain and NF tradeoff can be clearly observed in Fig. 6. As the gate inductance increases, the gain and bandwidth can both be effectively improved. However, a large gate inductor can lead to overpeaking of gain, and hence, circuit instability. As suggested by simulation, the circuit becomes unstable when the gate inductor exceeds $\sim$ 1 nH.

It is worth pointing out that the gate inductor peaking is more effective compared with a drain peaking design in the proposed topology. As discussed in Section III-A, a well-designed current-reuse stage only needs a small gate inductor for effective peaking. In addition, since the drain peaking connects the inductor at the load, its impact on the input-referred noise is relatively small. Fig. 7 illustrates this point by simulation. The core circuit is identical to that as shown in Fig. 5, except the peaking inductor L_d is connected in series with the load R_L. Compared with the results in Fig. 6(a), a significantly larger inductance is required for similar bandwidth enhancement, as shown in Fig. 7(a). More importantly, the gate peaking is much more effective in suppressing the high-frequency noise, which can be clearly seen from the difference between Figs. 6(c) and 7(c). Fig. 8 presents the inductance and Q as a function of frequency for the gate peaking inductor in our design. The top metal (whose thickness is 3.4 μm) is used for the inductor, which only occupies an area of 80×80 μm^2. The inductor is $\sim$ 0.4 nH in the frequency range of interest and the Q value is 17.8 at 10 GHz.

IV. MEASUREMENT RESULTS

The proposed UWB LNA was fabricated in a standard 0.13-μm CMOS process. Fig. 9 shows the chip micrograph. The overall chip area is 0.58×0.63 mm^2 and the core circuit area is only 0.14×0.22 mm^2 (0.031 mm^2). The LNA consumes 14.4 mW from a 1.8-V supply. The S-parameters measured from 0.1 to 14 GHz by on-wafer coplanar probing are shown in Fig. 10 together with the simulation results. Within 3.1–10.6 GHz, the measured small-signal gain (S_{21}) achieves a maximum value of 12.4 dB at 7.5 GHz, and has a minimum value of 11.1 dB at 9.8 GHz. In this frequency range, the measured output return loss (S_{22}) is less than -14 dB, the measured input return loss (S_{11}) is less then -7.3 dB, and the measured isolation (S_{12}) is less than -38.9 dB. The simulation in general agrees well with the measured results. The relatively large discrepancy in S_{22} can be attributed to the source follower used for output matching. In measurements, it is difficult to have the actual voltage applied to the circuit exactly the same with that used in simulation. Since the output impedance of the source follower is sensitive to the bias current controlled by V_{b3} (see Fig. 5), a small variation of V_{b3} could cause an obvious difference in S_{22}, which can be verified by simulation. The stability factor K calculated from the measured S-parameters is greater than 1 suggesting unconditional stability of the circuit. Note that the 3-dB bandwidth of the gain exceeds the measured frequency range (the gain varies from 9.7 to 12.4 dB within 0.1–14 GHz). Fig. 11 shows both the simulated and measured NF from 3 to 14 GHz with a minimum of 2.7 dB at 7.4 GHz and a maximum of 3.7 dB at 9.6 GHz (within the 3.1–10.6-GHz range). Fig. 12 shows the measured input third-order intermodulation (IIP3) at 6 GHz with a two-tone separation of 5 MHz. An IIP3 of -3.8 dB is obtained by extrapolation.

Since this study emphasizes a wideband LNA realized in a compact area, the figure-of-merit (FOM) proposed in [17] is adopted here, which takes the core chip area into consideration

$$\mathrm{FOM} = \frac{\mathrm{Gain}_{\max}[1] \cdot \mathrm{BW}_{3\mathrm{dB}}\,[\mathrm{GHz}]}{(\mathrm{NF}_{\mathrm{avg}} - 1)[1] \cdot P_{\mathrm{DC}}\,[\mathrm{mW}] \cdot \text{Core Area}\,[\mathrm{mm}^2]} \tag{10}$$

where $\mathrm{NF}_{\mathrm{avg}}$ is defined as the mean of the minimum and maximum values. Table I summaries the performance of the proposed LNA. The comparison with the prior arts based on 0.13-μm CMOS technology is also listed. For the FOM calculation, the 3-dB bandwidth is considered, while the NF is the average value within the range of 3.1–10.6 GHz. If this frequency range cannot be covered [9], the NF within the 3-dB bandwidth is employed to calculate the FOM.

V. Conclusion

A compact UWB LNA with a core area of only 0.031 mm^2 was demonstrated in a standard 0.13-μm CMOS technology. Based on the inductorless design considerations, the resistive-feedback and current-reuse techniques were employed. A small inductor of 0.4 nH was added at the gate of the input stage to effectively extend the bandwidth and suppress the increase of the NF at high frequencies. The amplifier achieved a bandwidth more than 13.9 GHz, a minimum NF of 2.7 dB, and a maximum gain of 12.4 dB. The proposed amplifier presented an FOM among the best compared with other published UWB LNAs in 0.13-μm CMOS technology.

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Po-Yu Chang was born in Changhua, Taiwan, in 1983. He received the B.S. degrees in engineering and system science and electrical engineering (double major) and M.S. degree in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2006 and 2009, respectively.

He is currently serving as a Corporal in the R.O.C. Army. His research included CMOS RF and analog integrated circuits design.

Shawn S. H. Hsu (M'04) was born in Tainan, Taiwan. He received the B.S. degree from National Tsing Hua University, Hsinchu, Taiwan, in 1992, and the M.S. degree in electrical engineering and computer science and Ph.D. degree from The University of Michigan at Ann Arbor, in 1997 and 2003, respectively.

In 1997, he joined the III–V Integrated Devices and Circuits Group, The University of Michigan at Ann Arbor, as a Research Assistant. He is currently an Associate Professor with the Institute of Electronics Engineering, National Tsing Hua University. His current research interests include the design of monolithic microwave integrated circuits (MMICs) and RFICs using Si/III–V-based devices for low-noise, high-linearity, and high-efficiency system-on-chip (SOC) applications. He is also involved with the design and modeling of high-frequency transistors and interconnects.

Prof. Hsu has served as a Technical Program Committee member of the SSDM (2008-present) and A-SSCC (2008-present). He was the recipient of the Junior Faculty Research Award of National Tsing Hua University in 2007 and the Outstanding Young Electrical Engineer Award of the Chinese Institute of Electrical Engineering in 2009.