A Low-Loss Fully Integrated CMOS Active Probe for Gigahertz Conducted EMI Test

Yin-Cheng Chang, Ping-Yi Wang, Da-Chiang Chang, and Shawn S. H. Hsu, *Member, IEEE*

***Abstract*— A fully integrated CMOS active probe for characterizing conducted electromagnetic interference (EMI) in the gigahertz range is presented. Based on the direct coupling method of International Electrotechnical Commission standard, the active 1-Ω current probe is designed and realized by a standard 0.18-μm CMOS technology to overcome a large insertion loss of 34.2 dB in the conventional passive probe. A high-precision on-chip 1-Ω resistance is implemented at the input, followed by a high gain and wideband amplifier in the proposed EMI probe. The measured insertion loss is significantly reduced to ∼18 dB with a bandwidth up to 3 GHz. Also, the conducted emission of a microcontroller unit is tested, which demonstrates that the proposed active probe could capture very low-level high-frequency interference overlooked by the conventional passive probe.**

***Index Terms*— Active current probe, CMOS, conducted emission, electromagnetic emission (EME), electromagnetic interference (EMI), integrated circuit (IC).**

I. Introduction

With the rapid progress of technology, integrated circuits (ICs) become more noisy and sensitive due to the increased operating speed and transistor number at a reduced supply voltage. As a result, the semiconductor vendors are often requested to provide testing information about the conducted electromagnetic interference (EMI) of ICs. Compared by identifying the EMI/electromagnetic susceptibility (EMS) issues at the system level in a final product, it is more efficient to run the test at the IC level first, which can avoid the complicated situation and evaluating the root cause of a specification violation of electromagnetic emission (EME) regulation. Via the measurements at the IC level, the electromagnetic compatibility (EMC) can be compared among various versions of design at different levels (IC, PCBs, modules, and system), which is beneficial for shortening the period of product development.

Two series of measurement standards, IEC 61967 [1] and IEC 62132 [2], for evaluating IC-level EME and EMS were published by the International Electrotechnical Commission (IEC). Different approaches were proposed based on these standards. The transverse electromagnetic (TEM) cell method [3], [4] collects the radiation from the device under test (DUT) for EME by a shielded enclosure, and the surface scan method [5], [6] captures near-field electric/magnetic wave above the DUT. The conducted-type EME can be measured by using a magnetic probe [7], [8] to receive the magnetic field resulted from current flowing on a metal trace designed for that purpose. As an alternative, the direct coupling method with the 1-Ω/150-Ω probes [9], [10] can be employed. The physical connection with the DUT can ensure the measured results with high repeatability.

The most important step to obtain reliable measurement results with the direct coupling method is to realize probes that satisfy the strict the IEC standards. One particular challenge is to meet the specifications with the 1-Ω current probe. The issue of parasitic effect that degrades the frequency response was improved by shunting multiple lumped resistors [11], and the current probe can be built to comply with the 1-GHz bandwidth of the IEC standard. A model for characterizing the conducted emission up to 3 GHz [12] was proposed by using the 1-Ω current probe. In addition, the on-chip 1-Ω/150-Ω probes implemented by the integrated passive device (IPD) technology [13] demonstrated the capability of conducted emission measurement up to 15 GHz in our previous study. It should also be mentioned that the bandwidth of the emission measurement has been successfully extended to the bandwidth of the immunity measurement approaches such as the gigahertz TEM (GTEM) cell method [14] and the extended power injection (DPI) method [15] to evaluate the modern high-speed ICs operating in the range of several gigahertz.

Although the 1-Ω current probe has been demonstrated with satisfactory bandwidth [11], an issue remained is the relatively large loss in the passive-type probes. Typically, the test point is with the lowest voltage potential of DUT; hence, the magnitude of the captured signal is often very small. As a result, the power level of some high-frequency interference could be close or even below the noise floor of the test receiver under a resolution bandwidth (RBW) setting of 100 kHz with a video bandwidth (VBW) of 10 kHz (10:1 ratio) defined by the IEC standards [1], [2]. Such low-level interference signals may be observed if the setting of the spectrum analyzer is adjusted to have a very narrow RBW down to several hundreds of hertz or below. However, the measurement becomes extremely time-consuming, which makes massive product testing with a high-throughput impossible.

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Y.-C. Chang, P.-Y. Wang, and S. S. H. Hsu are with the Department of Electrical Engineering, National Tsing Hua University, Hsinchu 300, Taiwan (e-mail: shhsu@ee.nthu.edu.tw).

D.-C. Chang is with the National Chip Implementation Center, National Applied Research Laboratories, Hsinchu 300, Taiwan (e-mail: dcchang@narlabs.org.tw).

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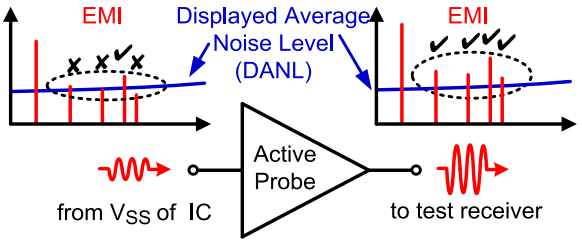


Fig. 1. Detection of the concealed interference around the noise floor of test receiver by the active probe.

On the other hand, overlook the weak interference of IC by a typical testing setup could lead to EMI problems in the final system. The noise is mainly caused by the transient current in IC. As the low-level transient current encounters high-impedance power distribution network (PDN), the voltage fluctuation may become significant. It has been reported that increase of the PDN impedance at frequencies above 100 MHz is dominant by the parasitic loop inductance [16], which is difficult to be reduced. Also, some resonances may occur at the unexpected frequencies [17], [18]. The proposed active probe could be used to measure the current spectrum at IC level as a reference for trouble shooting.

In this paper, an active 1-Ω probe is proposed to investigate the often neglected weak conducted emission based on the direct coupling method. The fully integrated active probe by the TSMC 1P6M 0.18-μm CMOS process is composed of a high-precision 1-Ω resistor and a wideband amplifier. Fig. 1 illustrates the concept of using the active probe to detect the concealed interference under the noise floor of the test receiver. Note that, the noise floor in Fig. 1 indicates the displayed average noise level (DANL) of the equipment. More explanation will be provided later with the experimental results in Section IV. With the additional gain provided by the amplifier, the weak interference can be observed by the test receiver even under a relatively wide RBW setting, which is suitable for high-throughput EMI testing. To the best of our knowledge, no study has been published to address the integrated 1-Ω current probe with gain enhancement for inspecting the EMI issues of ICs in the gigahertz frequency range. This paper is organized as follows. Section II reviews the direct coupling method for EMI test. The topology of the proposed active probe is also analyzed and compared with the passive probe. Section III presents the design of the proposed 1-Ω active probe, and the measured specifications are compared with the IEC standard. In Section IV, a microcontroller unit (MCU) with a customized test board is employed for EMI test using the active probe. The measured results demonstrate that the proposed active probe can perform the conducted emission measurements in a wide frequency range within a short period of time, which can identify the weak interference in modern high-speed ICs.

II. Direct Coupling Method and Active Probe

A. IEC 61967-4 Direct Coupling Method

The fast changes of currents/voltages in ICs cause the EME, which distributes via the PDN and becomes interference. Fig. 2 illustrates the configuration by using a 1-Ω current probe to measure the conducted emission based on the IEC 61967-4 direct coupling method. The 1-Ω probe is typically inserted between the V_{SS} port of the IC and the ground of PCB to measure the RF disturbance, because most of the return current would flow through the V_{SS} pin. The low impedance of 1-Ω resistor in the probe ensures normal operation of IC, which also allows extracting a small portion of the interference signal for analysis. Note that, the 49-Ω resistor provides 50-Ω impedance matching with the test receiver.

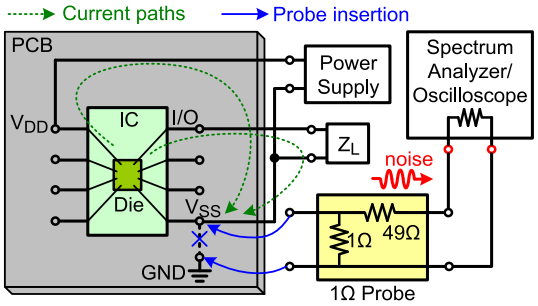


Fig. 2. Direct coupling method by using 1-Ω probe to measure the conducted emission of IC.

It should be emphasized that simultaneous switching in high-speed ICs results in the transient current drawn at the fundamental frequency and harmonics of the reference clock. These signals spread over a wide frequency range and act as the latent aggressors. If the impedance of PDN is not kept low enough on the PCB, the return current flows in the ground path would cause the appearance of transient voltage in the ground path. Consequently, the ground bounce affects the operation of other circuit blocks or even the entire system, leading to EMI issues. With the proposed active 1-Ω low-impedance probe, the signal level and frequency range of interference can be identified. The information not only could be used for PCB layout optimization of EMC issues but also give a comprehensive understanding of interference generated from the high-speed ICs for system design reference.

B. Topology Analysis of 1-Ω Probe

A conventional passive 1-Ω current probe based on the IEC standard is illustrated in Fig. 3(a). The probe has a relatively large insertion loss of 34.2 dB in a 50-Ω system, which is inevitable due to the resistive elements in the configuration. A straightforward approach is to add an amplifier at the output stage to improve the loss as shown in Fig. 3(b). Assuming an ideal 50-Ω (both input and output ports) amplifier with a gain of 10 dB is employed, the overall insertion loss can be reduced to 24.2 dB. By carefully investigating each element in this topology, the 49-Ω resistor is removed in the proposed active probe as shown in Fig. 3(c) to further improve the probe regarding insertion loss. Note that, the 49-Ω resistor provides 50-Ω impedance matching from the test receiver with the conventional passive probe. Similarly, it could also provide matching for the amplifier of a 50-Ω Z_{in}. However, the 49-Ω resistor is not necessary if the 1-Ω resistor and the amplifier can be fully integrated on chip at very close proximity in the frequency range of interest. Fig. 4 shows the simulated insertion loss (S_{21}) compared with the aforementioned

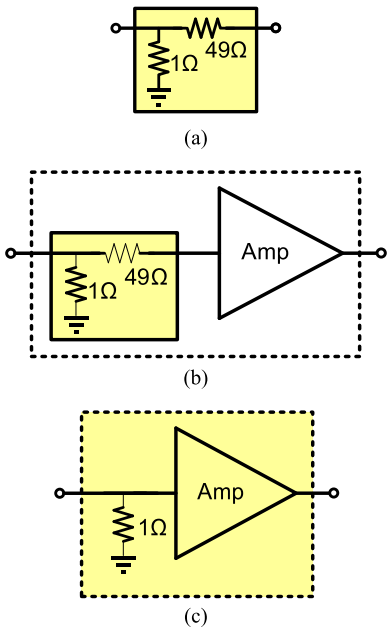


Fig. 3. Different topologies of 1-Ω current probe. (a) Conventional passive probe (IEC standard). (b) Conventional passive probe followed by an external amplifier. (c) Proposed fully integrated active probe.

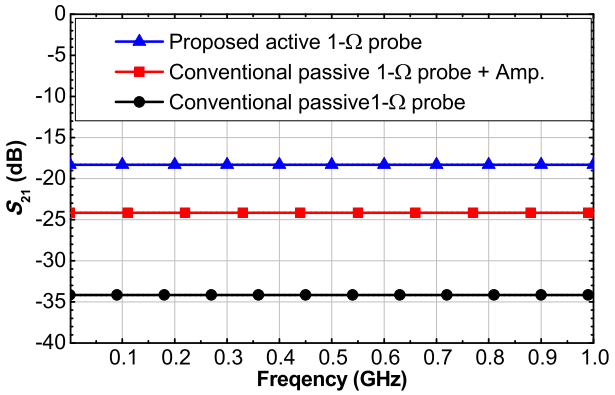


Fig. 4. Comparison of S_{21} with different 1-Ω current probe topologies.

different topologies. As can be seen, the proposed topology shows the best performance without the extra loss resulted from the 49-Ω resistor connected in the signal path. The insertion loss can be reduced from 34.2 dB (conventional passive probe) and 24.2 dB (active probe with the series of 49-Ω resistor) to only 18.3 dB. Note that, the results shown in Fig. 4 are based on the behavior model to demonstrate the proposed idea. Compared with the measured results as will be shown later for the actual 1-Ω probe (see Fig. 9), the results agree very well at low frequencies. Discrepancies can be observed at high frequencies since the ideal model does not consider the frequency response. It should also be emphasized that integration of the 1-Ω resistor and the LNA on chip can simplify the circuit by removing the 49-Ω matching resistor. The insertion loss can be further improved by about 6 dB to enhance the performance of active probe. Also, the integration of the 1-Ω resistor with the amplifier can directly eliminate extra connectors and cables, which is helpful for reducing the interference from the environment at high frequencies and maintain a wide bandwidth of measurements. With the much improved insertion loss, this topology is chosen as the fully integrated active probe for conducted emission measurements in this paper.

III. Design and Realization of 1-Ω Active Probe

The ideal design of the active current probe should have a precise 1-Ω Z_{in} with a high-transimpedance gain in a wide frequency range. Design an amplifier with a low Z_{in}, high gain, and a bandwidth from dc-to-gigahertz is a challenging task. The current feedback operational amplifier could achieve a low Z_{in} while tradeoff existing between bandwidth and gain [19], [20]. Also, the circuit stability is an issue for gigahertz range operation. The topology of common-gate amplifier with relatively low Z_{in} (about $1/g_m$) is a possible candidate [21]. However, it is very difficult to achieve an accurate 1-Ω Z_{in} in a wide bandwidth by active circuits. Besides, the large power consumption and bandwidth limitation make this approach impractical. In order to guarantee the precise 1-Ω Z_{in} and stable amplification with a wide bandwidth, the proposed active probe is composed of two parts, namely, the high-precision 1-Ω resistor and a wideband amplifier as described below, respectively.

A. High-Precision On-Chip 1-Ω Resistor

The implementation of a high-precision 1-Ω resistor by a standard IC process is critical for realizing the proposed active probe. The process variation should be considered during layout to minimize deviation from the desired resistance value. The layout technique of size expansion [22] was applied to achieve a wideband 1-Ω probe [13] with precise resistance by using the IPD process. The technique of shunting multiple resistors [11], which reduces the parasitic inductance and enhances power handling capacity of precision 1-Ω resistor for the current probe. There are several choices available to realize resistors in the adopted CMOS technology. The large sheet resistance and nonlinearity effect from the depletion layer make the n-well resistor unsuitable for the targeted low impedance application. The n+/p+ diffusion resistor could provide the moderate sheet resistance. However, the process variation due to diffusion is difficult to control. The main variation of IC resistors is introduced by the change of width (ΔW), since the length can be well defined by the contact formation during process. The p+ diffused resistor shows a ΔW of 0.08 μm (sheet resistance 7.76 Ω/□), which is much higher than that of the adopted p+ poly with silicide resistor (ΔW of 0.025 μm with the sheet resistance of 7.9 Ω/□). Assuming a typical 20% variation of the p+ diffused resistor, the 1-Ω resistor would range from 0.8 to 1.2 Ω, which results in a gain variation about ±1.5 dB compared with that of an ideal 1-Ω active probe. The p+ poly resistor with silicide is employed to obtain low resistance with high accuracy in this paper.

One important issue should be mentioned is the parasitic contact resistance, which needs to be carefully considered as realizing such a small resistance on chip. To highlight this issue, two resistors, R_1 ($L \times W$: 0.35 μm × 2.75 μm) and R_2 (0.7 μm × 5.5 μm, both L and W are doubled from R_1),

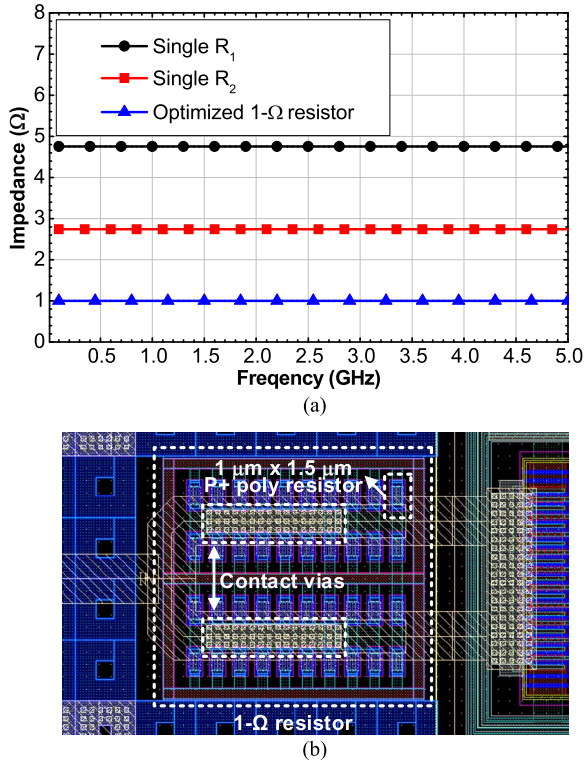


Fig. 5. 1-Ω resistor. (a) Design for precise 1-Ω resistance. (b) Optimized layout.

are both designed to have an intrinsic 1-Ω resistance according to the sheet resistance of 7.9 Ω/□ for the p+ ploy resistor with silicide. Fig. 5(a) shows the actual values from the postlayout simulation. The resistances are 4.75 and 2.74 Ω, respectively, which are quite different from the expected values. The results indicate that the parasitic contact resistance associated with the layout plays an important role here. Also, R_2 using the size expansion technique with the increased periphery and thus more contacts can reduce the parasitic resistance effectively. In the final design, the targeted 1-Ω resistance is realized by using both techniques of size expansion and shunting multiple resistors. By considering the tradeoff between the overall layout size and accuracy, the optimized 1-Ω resistor is composed of $40 \times 1\ \mu$m $\times$ 1.5 μm p+ poly resistors as shown in Fig. 5(b) of the layout. Note that, the IC designers tend to use the component with a minimal layout size such as R_1 with a minimal length of 0.35 μm (0.18-μm CMOS technology) in our initial design to save the chip area. As mentioned above, the size is expended gradually (e.g., R_2) by considering the process variation. As a result, the final 1-Ω resistor is optimized with the tradeoff between accuracy and size.

B. Design of Wideband Amplifier

The overall topology of the proposed active probe is shown in Fig. 6, where R_1 represents the 1-Ω resistor as described in Section III-A. Based on IEC 61967-1, the input port of the 1-Ω probe should be connected to a testing node, which often exhibits an extremely low voltage level (the V_{SS} node of DUT). A pMOS common-source (CS) amplifier consisting of M_1 and R_2 is served as the first stage for the active probe, which allows an almost zero gate voltage operation as long as

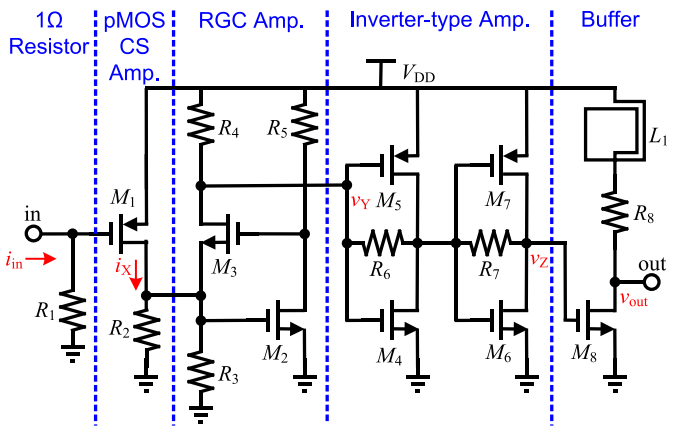


Fig. 6. Circuit topology of the proposed active probe.

V_{DD} and R_2 are properly chosen and designed to keep M_1 in the saturation region. Also, the high input impedance of CS stage can maintain an overall input impedance of 1 Ω for the active probe up to high frequencies.

The regulated cascode (RGC) configuration [23] is adopted for the second stage (M_2 and M_3 and $R_3 - R_5$), which is used for the transimpedance amplifier to achieve wideband operation. The RGC topology can be viewed as a CS amplifier together with a shunt transistor feedback. As shown in Fig. 6, M_2 and R_5 form the CS amplifier, which provides the amplified input signal back to M_3. The effective transconductance of M_3 is increased effectively. As a result, this topology has a much smaller input resistance compared with the common-gate stage. The small input resistance can avoid creating a dominant pole at the second stage, leading to an extended bandwidth. Also, the tradeoff between gain and bandwidth is relaxed due to isolation from the parasitic capacitance of the previous stage [24]. The cascaded inverter-type amplifiers ($M_4 - M_7$ and R_6 and R_7) with resistor feedback [25] can further enhance the overall gain of the active probe. The last stage of the active probe is an open-drain buffer for matching to the 50-Ω test receiver. A series peaking inductor at drain is employed to enhance the overall bandwidth.

The overall transimpedance gain v_{out}/i_{in} of the active probe can be expressed as

$$G = G_{1\,\Omega\_CS} G_{RGC} G_{inv} G_{buf} \tag{1}$$

where the overall gain expression is divided into four stages. The current gain of the pMOS CS stage with the 1-Ω resistor $G_{1\,\Omega\_CS}$ can be derived as (g_{mn} represents the transconductance of each MOSFET M_n, and R_{out_CS} and R_{out_RGC} are the output resistances of the CS and RGC stages, respectively)

$$G_{1ohm\_CS} = \frac{i_X}{i_{in}} = (-g_{m1} i_{in} R_1)/i_{in} \cdot \frac{R_{out\_CS}}{R_{out\_CS} + R_{in\_RGC}} \approx -g_{m1} R_1 \tag{2}$$

$$R_{in\_RGC} = \frac{1}{g_{m3}(1 + g_{m2} R_5)}. \tag{3}$$

Assume the input resistance of RGC stage R_{in_RGC} is relatively small and can be neglected, as shown in (3) [24]. As a result, i_X flows mainly into the source of M_3. The transimpedance gain of the second stage G_{RGC} can be expressed as (4) with

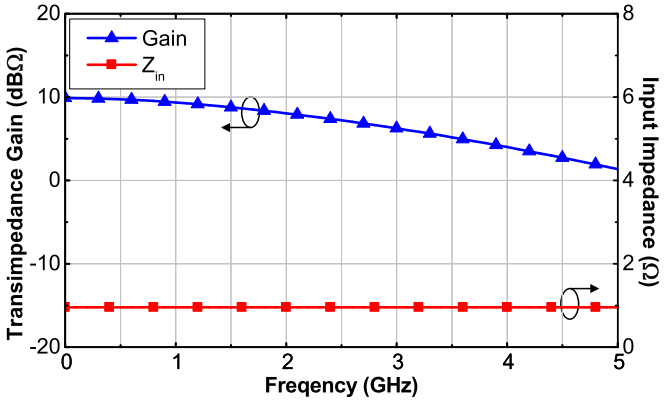


Fig. 7. Simulated transimpedance gain and Z_{in} of the active 1-Ω probe.

TABLE I
DEVICE PARAMETERS OF THE PROPOSED ACTIVE PROBE

Transistors	W/L (μm/μm)	Resistors	value(ohm)/type
M_1	60/0.18	R_1	1/P+ poly w/ silicide
M_2	24/0.18	R_2	50/P+ poly w/ silicide
M_3	12/0.18	R_3	560/P+ poly w/o silicide
M_4	9/0.18	R_4	840/P+ poly w/o silicide
M_5	36/0.18	R_5	265/P+ poly w/ silicide
M_6	9/0.18	R_6	840/P+ poly w/o silicide
M_7	36/0.18	R_7	840/P+ poly w/o silicide
M_8	45/0.18	R_8	40/P+ poly w/ silicide

the consideration of the next stage loading

$$G_{\mathrm{RGC}} = \frac{v_{\mathrm{Y}}}{i_{\mathrm{X}}} \approx R_4 \cdot \frac{R_{\mathrm{in\_inv}}}{R_{\mathrm{out\_RGC}} + R_{\mathrm{in\_inv}}} \tag{4}$$

where $R_{\mathrm{in\_inv}} \approx R_6/(1 + G_{\mathrm{m}}R_{\mathrm{T}})$ is the input impedance of the cascaded inverter-type amplifiers, and the gain is given by [25]

$$G_{\mathrm{inv}} = \frac{v_{\mathrm{Z}}}{v_{\mathrm{Y}}} \approx G_{\mathrm{m}}R_{\mathrm{T}} \tag{5}$$

where $R_{\mathrm{T}} \approx R_6//R_7$ and G_{m} is the effective transconductance ($g_{\mathrm{mn}}+g_{\mathrm{mp}}$) of the nMOS and pMOS in a single-stage inverter-type amplifier. The gain of the last stage is shown in (6), where it serves as a buffer that has a gain close to unity in this design. Note that, the impedance of L_1 is assumed to be a short circuit at low frequencies

$$G_{\mathrm{buf}} = \frac{v_{\mathrm{out}}}{v_{\mathrm{Z}}} \approx -g_{\mathrm{m8}}(R_8//R_{\mathrm{L}}). \tag{6}$$

Note that, the transistors in the proposed amplifier are all self-biased, and no extra gate biases for the MOSFETs are used. As a result, there is no need for the series ac coupling capacitors, which allows the dc-to-gigahertz operation frequency for EMI test. The design goal of the active probe is to provide a transimpedance gain of 10 dBΩ for amplifying the interference below/around the noise floor of a test receiver with an extended bandwidth above 3 GHz. Fig. 7 shows the simulated gain of the complete amplifier as illustrated in Fig. 6 including the 1-Ω resistor.

The detailed parameters of resistors and transistors are provided in Table I. In addition, the impacts of both process and temperature variations on the active probe are estimated by simulation. The gain variation ranges from 2.4 dB (at 1 GHz) to 3.7 dB (at 3 GHz) within the operating bandwidth at three different process corners (TT: normal case, FF: best case, and SS: worst case). Note that, the gain (at 1 GHz, TT case) changes about 2.1 dB as the temperature varies from 0 °C to 60 °C.

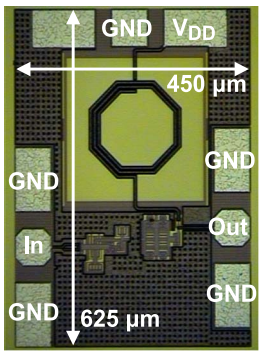


Fig. 8. Micrograph of the fabricated active probe realized in a standard 0.18-μm CMOS process.

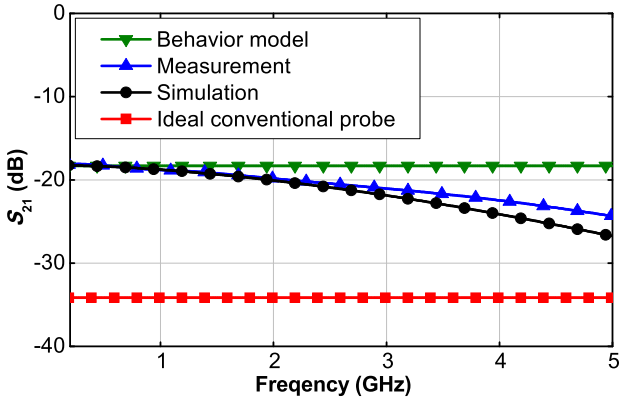


Fig. 9. S_{21} of the active 1-Ω probe.

C. Characteristics of Active 1-Ω Probe

The fabricated active probe chip as shown in Fig. 8 has a total chip size of 450 μm × 625 μm, including the RF and dc bias pads. With a supply voltage of 2 V, the circuit consumes a dc current of 35.2 mA. The S-parameters were measured by using Keysight N5222A Network Analyzer and compared with the specification of the IEC standard. As shown in Fig. 9, the simulated and measured S_{21} agree very well with a wide frequency range. The measured S_{21} of the active probe meets the target of around −18 dB as mentioned in Fig. 4. The bandwidth of active probe can be extended up to 3 GHz due to the wideband characteristics of both the 1-Ω resistor and amplifier. Figs. 10 and 11 show the simulated and measured results of the input and out impedance, respectively. The results show very good agreements and both meet the design targets. Note that, the simulated results shown in Fig. 5(a) are based on postsimulation, which has already considered the parasitic effects. The postlayout simulation adopted is RCC, which means that the resistance, capacitance, and the coupling capacitance are extracted from the layout. The impact of reactive parasitics can be optimized with a careful layout and selection of resistance type, and no frequency dependence can be observed within the desired bandwidth. As can be seen

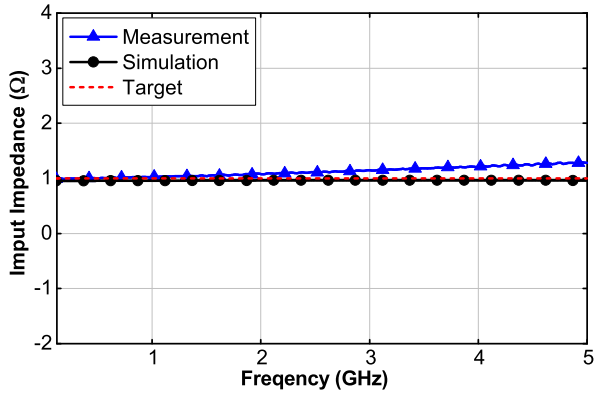


Fig. 10. Input impedance of the active 1-Ω probe.

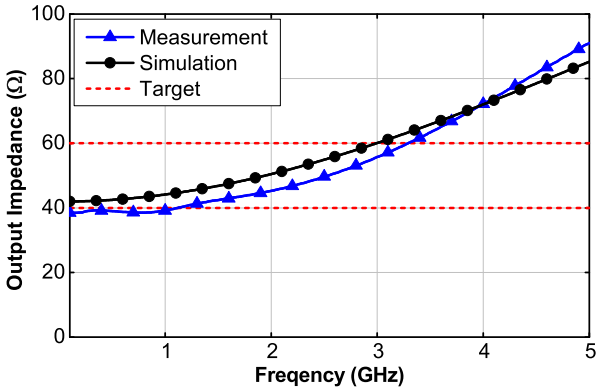


Fig. 11. Output impedance of the active 1-Ω probe.

TABLE II
COMPARISON BETWEEN IEC 1-Ω PROBE AND PROPOSED ACTIVE PROBE

Specifications	IEC standard	Proposed Active Probe
Bandwidth	1 GHz	3 GHz
Insertion loss	32 dB - 36 dB	18.1- 21.1 dB
Input impedance	1 Ω	1 Ω - 1.15 Ω
Output impedance	40 Ω - 60 Ω	38.5 Ω - 55.7 Ω

from Fig. 10, the measured results of input impedance agree well with simulation even up to 5 GHz. Table II lists the comparison of the specifications of the proposed active probe and the traditional passive 1-Ω probe in the IEC standard. The proposed active probe demonstrates a wider bandwidth with an extra gain, which is capable of identifying the low-level interference during EMI testing.

IV. DEMONSTRATION OF ACTIVE PROBE BY MCU TESTING

The experimental results verify that the active probe can effectively reduce the insertion loss compared with the conventional passive probe. To further demonstrate the capability of the proposed probes for identifying low-level conducted emission from the IC, an in-house designed MCU implemented by a standard 90-nm CMOS technology is employed as the DUT. The chip consists of an MC8051 core, in-system programing [26] mechanism, and the peripherals including general purpose IO, timers, communication interfaces, and memory. The 8051 MCU is designed via a cell-based design

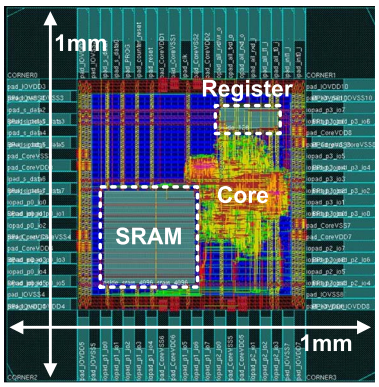
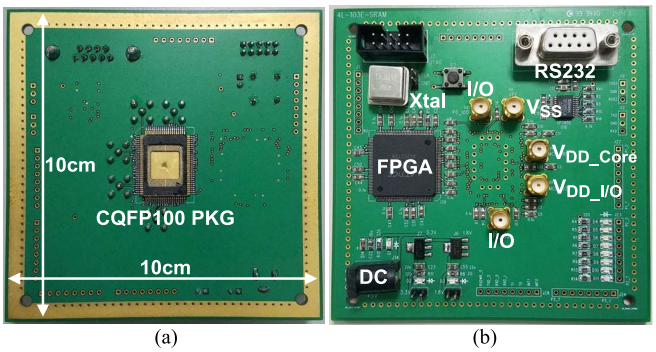


Fig. 12. Layout of the MCU chip.



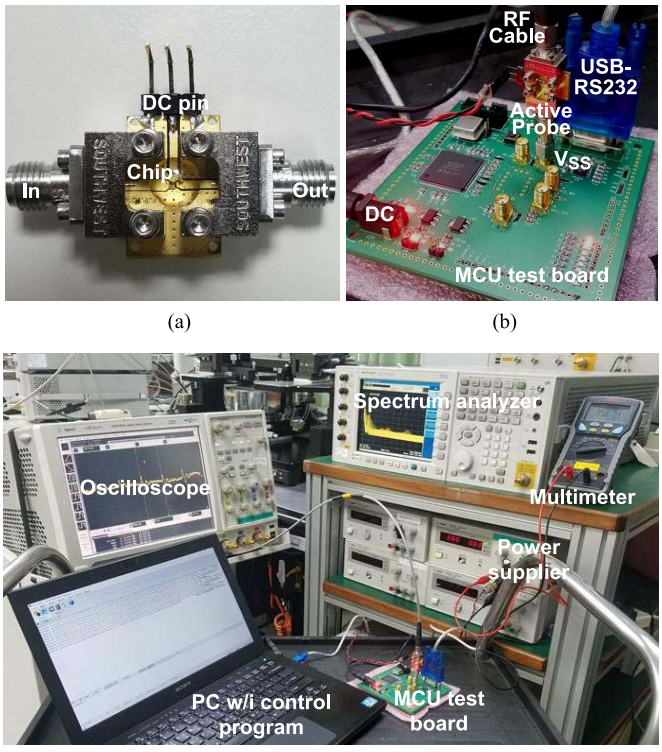
(a) (b)

Fig. 13. Photographs of the implemented MCU test board. (a) Back side with MCU chip for TEM/GTEM cell measurement. (b) Front side with all other needed components/connectors for testing.

flow with Synopsys design compiler and SOC Encounter. The chip layout is pad-limited with 84 I/O pads and the size is 1 mm × 1 mm as shown in Fig. 12. The MCU can be operated under the supply voltages of 1.8 and 3.3 V for core and I/O, respectively, and the maximum operating frequency is about 200 MHz. A test board, as shown in Fig. 13, is designed and fabricated for the MCU measurements.

Not only the functions of running basic instructions such as arithmetic, logic, data transfer, jump, and I/O are verified, but also multiple IC-EMC measurements complied with the IEC standards can be conducted with the same board [27]. To guarantee the validation of measured results, the basic design recommendations described in the standard IEC 61967-1 [28] should be followed. The thickness of test board is 1.6 mm which comprises four metal layers, including a ground layer, a power supply layer, a signal layer, and a layer for routing traces with ground. The packaged 8051 MCU was solely placed on the back side of test board for TEM/GTEM cell measurement as shown in Fig. 13(a), and all the other needed components/connectors were mounted on the front side as shown in Fig. 13(b). The local ground (V_{SS}) under IC was separated from the global ground (GND) and connected to an SMA adaptor for testing the 1-Ω direct coupling method.

Also, the active probe was mounted on a PCB with the dc pins and two SMA adapters as shown in Fig. 14(a) for connection with the V_{SS} port of MCU. The chip of active probe is mounted on the high-frequency PCB (RO4350B). The interconnects including the bondwire, PCB trace, and the SMA connectors (Southwest Microwave 292-04A-5) are designed



(a) (b) (c)

Fig. 14. Photographs of the setup for conducted emission measurement. (a) Active probe, (b) close view of the test board with active probe, and (c) complete measurement setup.

carefully to minimize the impact of parasitics on loss and bandwidth of measurements. In this paper, the interconnects contribute additional loss about 0.4 dB at 1 GHz. Note that, the bandwidth of the probe with the SMA connectors and PCB becomes 2.9 GHz, and the insertion losses are 18.5 dB, 17.5 dB, and 20.7 at 1, 2, and 3 GHz, respectively. The measured results could be further improved by a better package solution. Note that, the interconnects between the probe and IC GND pin(s) are one of the limitations on bandwidth for the 1-Ω EMI test. This paper mainly focuses on achieving a wideband active probe, but does not deal with the bandwidth limitation regarding interconnects in the test setup. Fig. 14(b) shows the close view of the test setup where the dc and RF cables are connected with the USB-RS232 for signal transmission. The active probe collects the EMI signal from V_{SS} port of MCU, and V_{SS} is connected to both a spectrum analyzer (Agilent N9030A) and/or an oscilloscope (Agilent DSA91204A) as the test receivers. Fig. 14(c) shows the photograph of complete setup, which allows performing conducted emission measurement with high reliability.

Fig. 15(a) shows the results of the measured spectrum by using a verified passive 1-Ω probe [11] that complied with the specifications in the IEC standard. The settings of RBW and VBW of spectrum analyzer also follow the IEC standard of 100 and 10 kHz, respectively. As can be seen, the observed interference is mainly below 400 MHz, which leads to a wrong conclusion that the MCU may not generate noise at above 400 MHz. In contrast, Fig. 15(b) shows the results obtained by the proposed on-chip CMOS

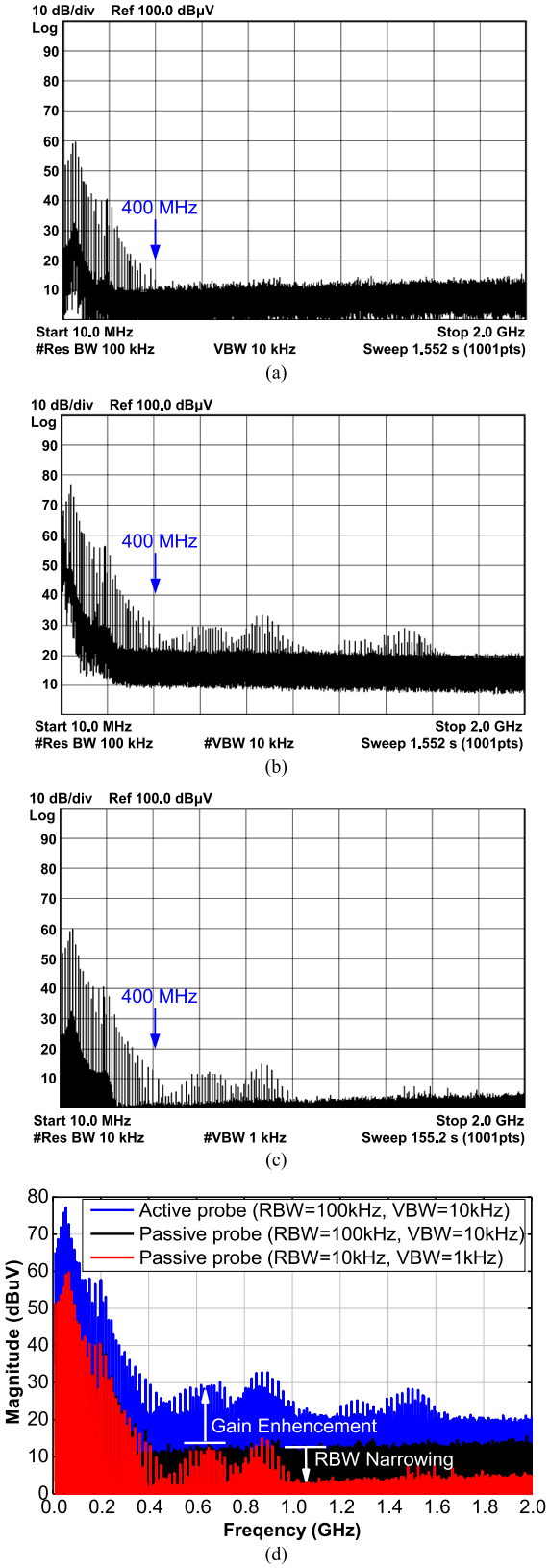


Fig. 15. Measured spectra at V_{SS} port of MCU by (a) passive 1-Ω probe, (b) proposed active probe, and (c) passive 1-Ω probe with narrower RBW and VBW settings of the spectrum analyzer, and (d) stacked spectrum for comparison.

active probe. With the same set of RBW and VBW, it is clear that much more high-frequency interference above 400 MHz can be observed, which could potentially disturb normal

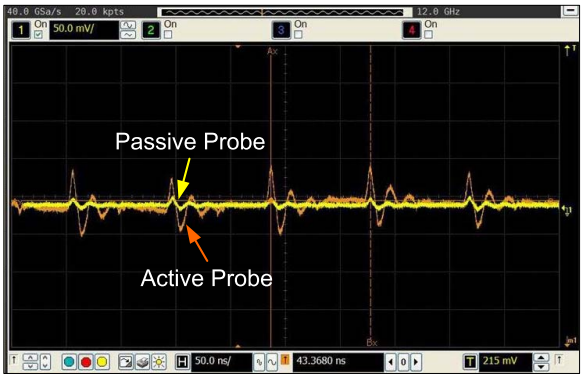


Fig. 16. Measured waveforms at V_{SS} port of MCU by passive and active probes.

system operation. The RBW and VBW are also narrowed down with the passive probe to verify the consistency of results obtained from the active probe. By reducing the RBW and VBW to 10 and 1 kHz, respectively, the noise floor is lowered by 10 dB and the hidden high-frequency interference appears in the spectrum as shown in Fig. 15(c). The results also agree well with that observed in Fig. 15(b). Note that, the sweep time increased by 100× compared with the initial RBW and VBW settings, which makes it impractical for massive product testing.

The experimental results are stacked together in Fig. 15(d) for comparison. As can be seen, the active probe allows observing the interference hidden under the noise floor of test receiver with a reasonable time, which can be employed to identify the source of failure for practically high-speed IC EMI test. It should be emphasized that the noise has the same amplification as the signal after passing through an amplifier, but this can only be observed if both noise and signal levels are higher than the DANL. For example, by observing the spectrum in Fig. 15(a), the noise floor is at 10 dB and no noise harmonics in the 600-MHz range appear. In Fig. 15(b), the noise floor and the 600-MHz harmonics observed become around 20 and 30 dB, respectively, which implies a different increase of the noise floor and signal with the active probe. Note that, DANL is not the actual noise floor. It changes with the RBW of spectrum analyzer, as can be observed from Fig. 15(a) and (c). The signal or noise level below DANL will be concealed. A common situation is that the signal level is higher than DANL, but the actual noise level is lower than DANL. In that case, the signal will be amplified as expected, but the noise level is still under DANL. On the other hand, if the actual noise floor is not much lower than DANL and/or the amplifier gain is high, a new noise floor rather than DANL can be observed, which is shown in Fig. 15(b). Note that, this is the actual noise floor of the whole system. Therefore, the observed increase of signal level and noise floor could be different even with the same amplifier. The time-domain measurements of both passive and active probes were also performed by the oscilloscope. The measured waveforms of conducted emission can be used to build the internal activity of IC electromagnetic model [29]. As shown in Fig. 16, the waveform obtained from the active probe provides much more details than that from the passive probe. These results demonstrate the advantages of proposed active probe, which can help to observe the weak interference on the spectrum efficiently, and provide more detailed information of the interference for further analysis.

V. Conclusion

A fully integrated active probe in a standard CMOS technology for conducted EMI testing up to gigahertz range was demonstrated. The proposed probe showed a significantly reduced insertion loss from 34.2 dB of the conventional passive probe to only 18 dB with a bandwidth up to 3 GHz. A high precision on-chip 1-Ω resistance was achieved by using the techniques of size expansion and shunting multiple resistors. Also, a high gain and wideband amplifier using the pMOS input stage and RGC/inverter gain stages was designed and implemented. Moreover, an MCU IC was employed as the DUT with the customized test board for EMI test. The results demonstrated that the overlooked high-frequency interference signal with the conventional passive probe can be identified successfully by the proposed active probe in the conducted emission measurements.

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Yin-Cheng Chang received the B.S. and M.S. degrees from Feng Chia University, Taichung, Taiwan, in 2003 and 2005, respectively, and the Ph.D. degree in electronics engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2019.

Since 2005, he has been with the National Chip Implementation Center, Hsinchu, where he is currently an Associate Research Fellow. His current research interests include RF/MW circuit design and measurement, signal integrity, power integrity, and electromagnetic compatibility.

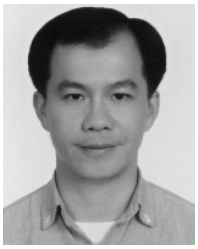
Dr. Chang is a member of the Phi Tau Phi Scholastic Honor Society. He was a recipient of the Best Symposium Paper Award and the Best Poster Paper Award of the 2013 APEMC and 2017 APEMC, respectively, and the Technical Achievement Award from the National Applied Research Laboratories in 2018.

Ping-Yi Wang was born in Kinmen, Taiwan, in 1984. He received the B.S. degree in electronic engineering form Chung Yuan Christian University, Taoyuan, Taiwan, in 2007, and the M.S. degree in electronic engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2009, where he is currently pursuing the Ph.D. degree in electronics engineering.

His current research interests include frequency synthesizers, low-power RF front-end circuits, and mixed-signal circuits.

Da-Chiang Chang was born in Taipei, Taiwan, in 1966. He received the B.S. and M.S. degrees in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1989 and 1991, respectively, and the Ph.D. degree in electronic engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 2001.

From 1991 to 1993, he was an Officer of the Republic of China Air Force. In 1993, he joined the Department of Electronic Engineering, Chinese Institute of Technology, Taipei, as an Instructor and became an Associate Professor in 2001. From 2002 to 2003, he was with the United Microelectronics Cooperation, Hsinchu. From 2003 to 2005, he was with the Acer Laboratories Inc. (ALi), Taipei. In 2005, he joined the National Chip Implementation Center, Hsinchu, where he is currently a Research Fellow and the Division Director in charge of the chip implementation services, and the development of RF system-in-package, millimeter-wave circuit, high-speed data link, and signal integrity design environmental and measurement technologies.



Shawn S. H. Hsu (M'04) was born in Tainan, Taiwan. He received the B.S. degree from National Tsing Hua University, Hsinchu, Taiwan, in 1992, and the M.S. and Ph.D. degrees from the University of Michigan, Ann Arbor, MI, USA, in 1997 and 2003, respectively.

He is currently a Professor with the Institute of Electronics Engineering and the Electrical Engineering Department, National Tsing Hua University, Hsinchu. He has been an appointed Distinguished Professor with National Tsing Hua University since 2014. His current research interests include the design of monolithic microwave integrated circuit and RFICs using Si/III–V-based technologies. He is involved with the design, fabrication, and the modeling of high frequency transistors and interconnects. He is also interested in heterogeneous integration using system-in-package and 3-D integrated circuit technology for high-speed wireless/optical communications.