A K-Band Reconfigurable Pulse-Compression Automotive Radar Transmitter in 90-nm CMOS

Kai-Wen Tan, An-Hsun Lo, Ta-Shun Chu, *Member, IEEE*, and Shawn S. H. Hsu, *Member, IEEE*

***Abstract*—A K-band ultra-wideband (UWB) pulse-compression (PC) automotive radar transmitter in 90-nm CMOS is presented, which is composed of the fully integrated pulse generator, mixer, driver amplifier, phase-locked loop, and timing circuitry. The PC technique with coding gain can effectively enhance the detection resolution and also improve the signal-to-noise ratio (SNR). We propose a PC transmitter allowing fast and precise code generation with small power consumption and chip area, and also offering reconfigurable capability. Compared with previously reported UWB pulse radars with relatively simple coding schemes, the proposed transmitter features a much more challenging 15-bit pseudonoise code design using high-speed shift registers, which can improve SNR up to 23.5 dB. The measured results demonstrate correct output waveforms corresponding to different modulation codes with the spectrum well confined under the regulation mask. With a modulation rate over 3 Gb/s (pulse repeat frequency of 6.125 MHz), a resolution of $\sim$ 5 cm can be achieved.**

***Index Terms*—Automotive radar, CMOS, K-band, pulse compression (PC), transmitter, ultra-wideband (UWB).**

I. Introduction

THE FAST growing market drives the demand for automotive radars with low cost and a small form factor. The automotive radar systems currently available are mostly realized in compound semiconductor technology with a relatively low integration level and a large size. Recent advances of CMOS technology have led to impressive transistor f_{T} and $f_{\max}$, which make CMOS a promising candidate for highly integrated and low-cost automotive radar systems in the microwave frequency range, especially the short-range radar (SRR) applications in K-band. The Federal Communications Commission (FCC) has established the standard in 22–29 GHz (K-band) for SRR applications with a maximum emission power of -41.3 dBm/MHz [1]. Under the strict regulation of emitted power, the ultra-wideband (UWB) radar technology is adopted for such applications. The UWB approach allows operation in a spread spectrum by pulse signals, thus the spectrum can be used much more efficiently with existing systems.

Previous studies have reported good results of integrated K-band UWB systems in SiGe and CMOS technology for automotive radars [2]–[9]. A comprehensive tutorial paper [2] discussed the UWB sensor for SRR applications from different points of view such as the design requirements and system architectures. One issue addressed in this paper is the importance of the ability to assign different codes in the system to improve the resilience to interferences. However, a very fast set of code generators is required to maintain the high-range resolution. A fully integrated 24-GHz UWB radar sensor in 0.13-μm SiGe BiCMOS technology was reported [4]. A binary phase-shift keying (BPSK) modulator was included in the sensor with a control unit for pulse modulation. A dual-band 22–29/77–81-GHz automotive radar transceiver realized in 0.18-μm SiGe BiCMOS was demonstrated [6]. Although not included in the chip, this paper also mentioned that the capability of coding for pulse compression is the solution to meet the spectral limitations and to achieve the same range resolution as a short pulse. More recently, a 24-GHz UWB radar transmitter with pulse compression was reported [7]. A 2-bit bi-phase modulator was employed, and a minimum range resolution of 7.5 cm was achieved. Based on the previous literature review, one can conclude that pulse compression technique with proper coding is of great advantage for UWB automotive radar applications. However, integration of the high-speed coding scheme remains challenging, and only relatively simple design such as 2-bit BPSK was reported. In this study, we report a K-band UWB transmitter in CMOS technology with a fully integrated pulse generator capable of a 15-bit reconfigurable coding scheme.

This paper is organized as follows. Section II explains the principle of pulse compression and the architecture of the proposed transmitter. Section III elaborates the design of reconfigurable pulse generator with high-speed shift registers, and also other important building blocks such as the mixer and phase-locked loop (PLL). Section IV presents the experimental results in both the time domain and frequency spectrum. Finally, Section V concludes this paper.

II. Pulse Compression in UWB Radar

A. Pulse Compression Technique

Fig. 1 illustrates the principle of the pulse compression technique, which allows increasing the range resolution and improving the signal-to-noise ratio (SNR). As shown in the figure, a single pulse with a pulse width T has a main lobe of $2/T$ (sidelobes neglected) in the spectrum. After applying n-bit bi-phase modulation to the pulse, the pulse bandwidth is extended to n times with reduced signal intensity. For a UWB radar transceiver, a long pulse is preferred, which results in an improved SNR. However, the range resolution can be suffered

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The authors are with the Department of Electrical Engineering, National Tsing Hua University, Hsinchu 300, Taiwan (e-mail: shhsu@ee.nthu.edu.tw).

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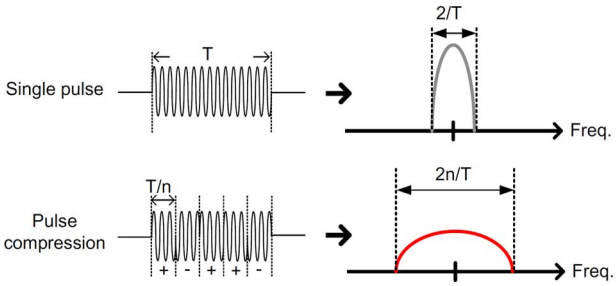


Fig. 1. Waveform and spectrum of the conventional pulse and the bi-phase pulse compression, where T is the pulse width and n is the bit number.

with risk of exceeding the emission power regulation. The pulse compression technique offers the solution to this issue [10], [11]. By properly modulating the signal, a long pulse in the time domain can be effectively spread in spectrum, which is helpful to achieve a high-range resolution and maintain good SNR, while satisfying the FCC standard. In addition, different coding schemes can be inserted in the pulse to enhance further the SNR of the UWB radar.

B. Proposed PC Transmitter Architecture

By using the digital phase modulation, the pseudorandom binary sequence (PRBS) code can be incorporated in the transmission pulse, leading to SNR improvement. Previous studies [2]–[4] use a typical configuration for applying binary phase modulation to the single pulse, as shown in Fig. 2(a). The mixer is connected to the PRBS to change the phase of pulse, and followed by a switch to turn on/off the pulse at the output. However, both the mixer and the switch often need inductive components to enhance the frequency response for K-band operation, resulting in a large chip area. Besides, the mixer still draws a constant dc current even when the pulse is turned off, which increases the total power consumption. In this work, we propose a low-power and area-efficient transmitter architecture, as shown in Fig. 2(b). The compressed pulse is synthesized at the baseband and then up converted to K-band by a mixer. Compared with the conventional design where the PRBS and pulse are processed in a series order, the proposed design completes this step in a parallel manner. By using a high-speed encoder to combine both the phase code and pulse width control, a compressed pulse can be generated. The encoder is realized by static logic gates, meaning there is no extra power consumption of the mixer during the off period of the pulse. Also, the switch is no longer needed and a smaller chip area can be achieved. It should be emphasized that the phase coding and width control of the pulse are both achieved by the high-speed shift registers in this design. Feeding the shift registers with a synchronized clock is critical to ensure correct pulse compression, which is also a very challenging task in practical design. This is discussed in more detail below.

Fig. 3 shows the detailed system block diagram of the proposed PC transmitter, which includes the PLL, timing generator, reconfigurable pulse generator, mixer, and driver amplifier (DA). The PLL provides a K-band local oscillator (LO) signal for the mixer and also serves as a high-speed clock (CLK) for the reconfigurable pulse generator. Note that a frequency of 25.088 GHz, close to the central frequency of

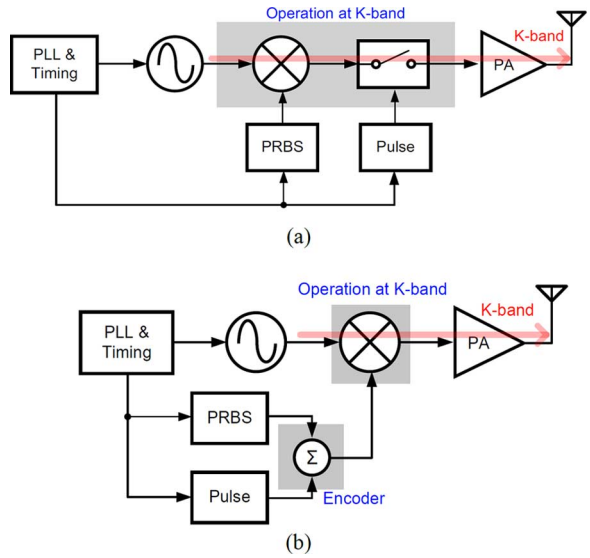


Fig. 2. (a) Typical architecture for radar transmitter with pulse compression. (b) Proposed transmitter architecture in this design.

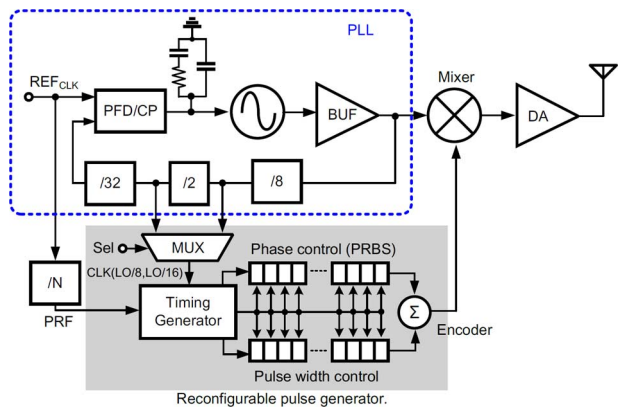


Fig. 3. Proposed K-band pulse compression transmitter.

this band (22–29 GHz), is chosen for PLL operation to fulfill the FCC mask requirement. The reconfigurable pulse generator can provide the baseband pulse including a digital code up to 15 bit, and the output pulse width and coding can be defined by the on-chip serial-to-parallel interface (SPI) with the external software control. The reason for choosing a code length of 15 bits is to use the Barker code in the compressed pulse, which is very suitable for pulse radar applications [2]. In theory, the SNR can be improved by 23.5 dB with 15-bit coding. A shorter code length can also be adopted, depending on the applications. The timing generator can provide proper timing signals for the high-speed shift register. The mixer up-converts the coded baseband pulse to the K-band. Finally, the DA provides the gain and 50-Ω output for measurements.

C. Analysis of Design Parameters

Several design parameters must be considered in the UWB radar systems. One important parameter is the pulse repeat frequency (PRF), which defines the maximum detection range R_{MAX}, as shown in (1), where c is the speed of light,

$$\mathrm{PRF} = \frac{c}{2R_{\mathrm{MAX}}}. \tag{1}$$

A typical R_{MAX} is about 20 m for SRR applications [2], which leads to a PRF of 7.5 MHz. In this design, a PRF of 6.125 MHz is generated from the reference clock of 49 MHz using a divide-by-8 frequency divider. The corresponding R_{MAX} is 24.5 m.

The range resolution is also of a critical importance in the UWB radars. The resolution (ΔR) of UWB pulse radar can be determined as (2), where T is the pulse width, and B is the pulse bandwidth,

$$\Delta R = \frac{(c \times T)}{2} = \frac{c}{2B}. \tag{2}$$

To achieve a resolution of 5 cm in SRR applications, the minimum pulse width should be close to 333 ps ($B = 3$ GHz). Since the width of transmission pulse is defined by the high-speed shift registers, the injected clock should also be able to operate at around 3 GHz. In this design, the high-speed clocks can be generated from the divider chain of the PLL including LO/8 and LO/16 GHz for the multiplexer (LO $=$ 25.088 GHz), where the maximum clock speed can reach 3.136 GHz. The various clock speeds available in the transmitter is flexible for different applications such as blind spot detection (0.1–0.2 m) or parking aid (0.05–0.2 m).

Another important issue is that the emitted power of the transmitter must fulfill the FCC regulation, i.e., the average equivalent isotropically radiated power (EIRP) should be smaller than -41.3 dBm/MHz within 22–29 GHz. The peak value $\mathrm{EIRP}_{\mathrm{PEAK}}$ of the transmitter can be calculated by (3), where D is the duty cycle of PC waveform,

$$\mathrm{EIRP}_{\mathrm{PEAK}} - 10\log(B) - 10\log(D) \leq -41.3\ \mathrm{dBm/MHz}. \tag{3}$$

With the fully integrated PLL to generate the LO, CLK, and PRF signals, D can be expressed as follows:

$$D = \frac{T_{\mathrm{pulse}}}{T_{\mathrm{PRF}}} = \frac{\frac{(D_{\mathrm{CLK}} \cdot \mathrm{bit\_number})}{(D_{\mathrm{total}} \cdot \mathrm{CLK_{REF}})}}{\frac{D_{\mathrm{PRF}}}{\mathrm{CLK_{REF}}}} = \frac{D_{\mathrm{CLK}} \cdot \mathrm{bit\_number}}{D_{\mathrm{PRF}} \cdot D_{\mathrm{total}}} \tag{4}$$

where D_{total} is the total divider number of PLL (512 in this case), D_{CLK} is the divider number of the reconfigurable pulse generator, D_{PRF} is the divider number of the PRF, and bit_number is the enabled modulation bit during operation. Considering the case of the output with a maximum pulse bandwidth (bit_number $=$ 15, D_{CLK} and D_{PRF} are both set to 8), D can be calculated as 0.029, assuming a reasonable bandwidth at RF of (2 $\times$ CLK) GHz. The corresponding $\mathrm{EIRP}_{\mathrm{PEAK}}$ of the PC transmitter is 12 dBm based on (3). With a typical antenna gain of 15 dBi, the output power of the PC transmitter should be around -3 dBm. As can be seen, the required output power with the pulse compression technique is smaller than that in the single pulse radar, which makes the fully integrated transmitter in CMOS technology more practical. The dc power consumption of the system can also be effectively reduced.

III. Pulse Generator and Other Building Blocks

A. Reconfigurable Pulse Generator

It is difficult to obtain a precise pulse width and also synchronize the phase code and pulse width control sequences by using the *RC* time constant delay to generate the baseband pulse [6]. The proposed reconfigurable pulse generator is shown in Fig. 4, which is composed of two parallel 16-bit high-speed shift registers to control individually the binary phase and pulse width of the waveform. Note that the first bit is only used to initialize the pulse generation, and the actual programmable bits are 15.

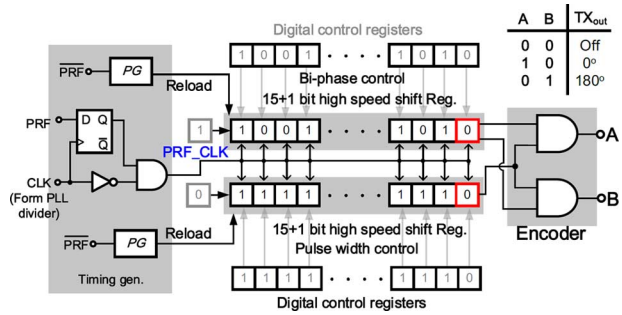


Fig. 4. Proposed reconfigurable pulse compression generator.

As illustrated in Fig. 4, the clocks from the divider of the PLL and the PRF signal are synchronized first in the timing generator. By using an AND logic, the timing signal (PRF $\cdot$ CLK) for driving the high-speed shift register can be generated. The pulse generator (denoted as PG) will enable the reload action from the values stored in the SPI into the high-speed shift registers. Following this step, the clock will then shift the values of registers (parallel-in/serial-out) to the encoder. The encoder consists of two AND logics to archive a tri-state transmitter output including "A $=$ 0, B $=$ 0," "A $=$ 1, B $=$ 0," and "A $=$ 0, B $=$ 1," representing an off state, phase of 0°, and phase 180°, respectively. Note that "A $=$ 1, B $=$ 1" will not appear at the output of the encoder.

Fig. 5 presents the simulated timing sequences and operation details using a PRF of 40 MHz and a CLK of 4 GHz. After the PRF signal falling, the reload signal (denoted as Reload) for the pulse appears, where T_1 is the delay to avoid timing overlap between PRF $\cdot$ CLK and Reload, and the width of T_2 should ensure the initial values can be accurately reloaded from the SPI into the high-speed shift registers. In this design, T_1 and T_2 are 850 ps and 2 ns, respectively. At the PRF signal rising edge, the value of the phase code and pulse width in the high-speed shift register will be shifted to the encoder. Note that the number "1" in the pulse-width-control registers must be identical to the code length in the phase control register. As can be observed in Fig. 5, when the stored value in pulse width control chain is shifted to "0" at the first bit of pulse width control, the PC transmitter will be turned off. On the other hand, when the stored value in pulse width control is "1," the phase of the transmitter output signal is defined by the bi-phase control bit. By further mixing the encoder output signal with the LO, the K-band PC waveform can be generated at the output of DA.

B. High-Speed Shift Registers

The high-speed shift registers for gigahertz operation are usually realized by the current mode logic (CML), but the relatively large power consumption is a major concern [9]. A sense-amplifier-based flip-flop (SAFF) has been proposed [12], which showed excellent high-speed operation capability with reduced power consumption. In this study, the SA-based logic is adopted

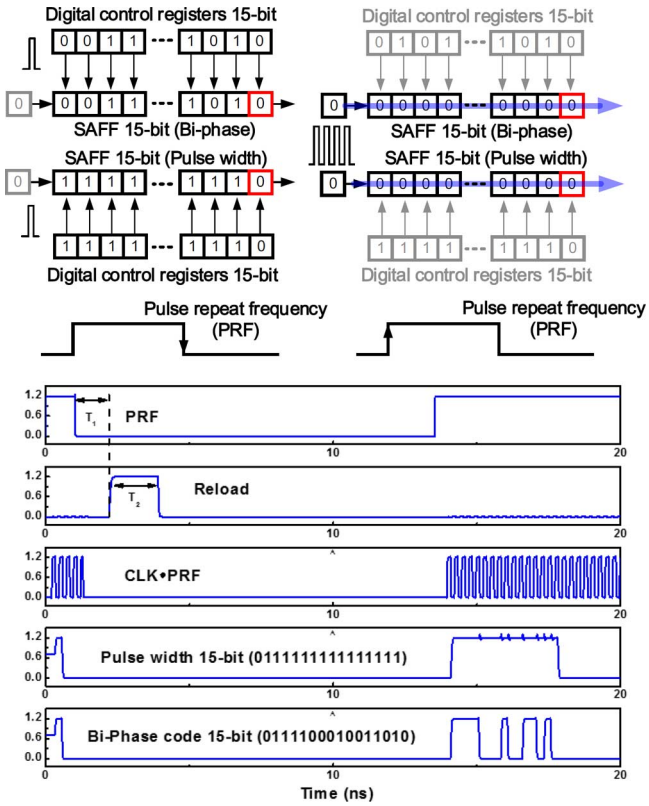


Fig. 5. Simulation results of timing sequence for the reconfigurable pulse generator.

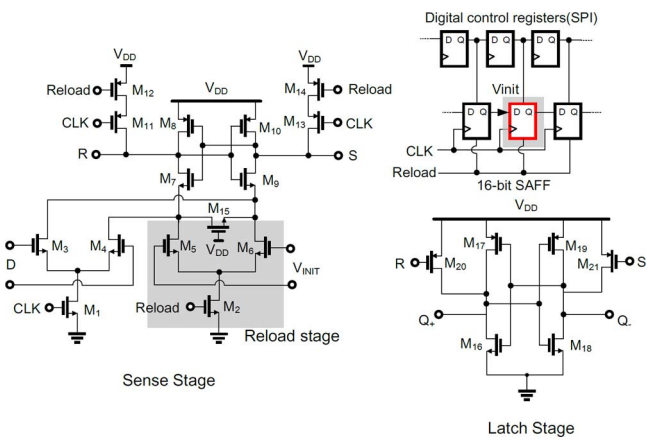


Fig. 6. Proposed parallel-in-serial-out DFF using sense-amplifier-based configuration.

in the high-speed shift register design with a reload stage added to have a parallel-in-serial-out function for pulse compression, as shown in Fig. 6. During the on period of the PRF signal, the input of sense stage M_3 and M_4 (D), connected to the output of the preceding stage, can perform serial data transmission. Also, the reload stage input M_5 and M_6 (V_{INIT}) is connected to the SPI registers to deliver parallelly the initial values into the SAFF at the Reload signal rising. During the CLK and Reload signals off, the latch stage $(M_{16} - M_{21})$ can maintain the value of the sense-amplifier output. The SA-based D-flip-flop should be able to operate up to 3.136 GHz with serial output. Note that the circuit with extra parasitics makes it more challenging for high-speed operation. More specifically, the extra parasitic capacitances from the reload stage increase the loading and reduce

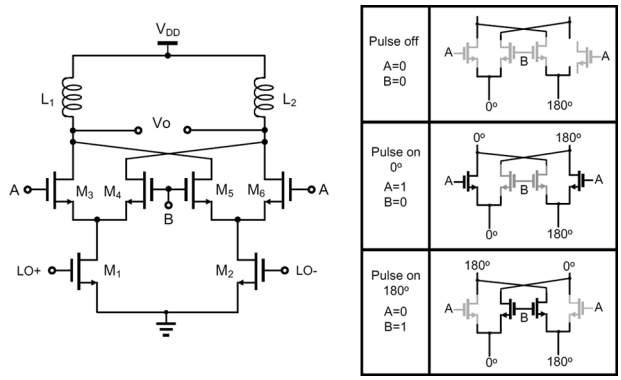


Fig. 7. Mixer in the proposed PC UWB radar and its operating principle.

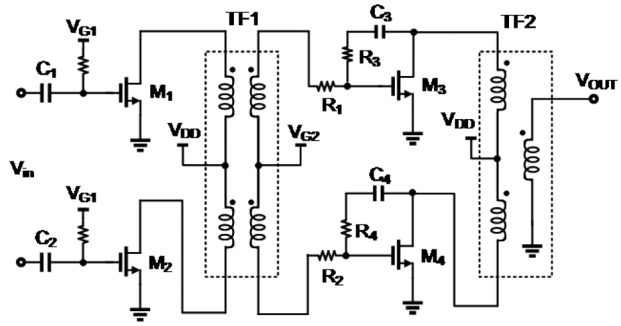


Fig. 8. Proposed two-stage DA.

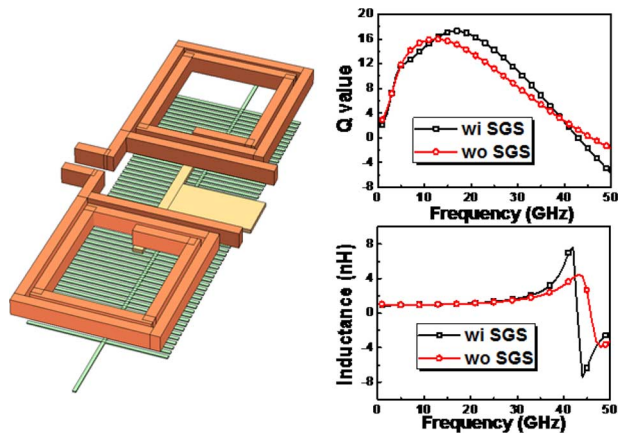
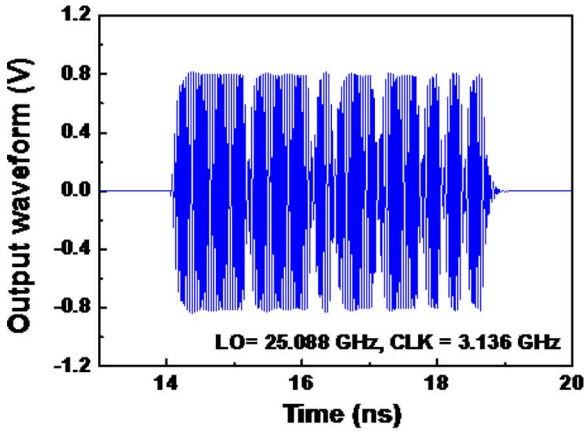


Fig. 9. Inductive components with ground shielding adopted in the mixer.

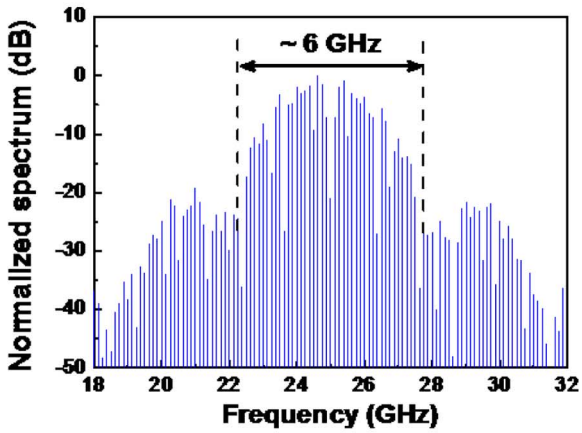
speed of the latch $(M_7 - M_{10})$. In this design, M_3 and M_4 with relatively large sizes are used to eliminate the speed bottleneck at the input stage, whereas M_5 and M_6 are kept small to reduce the parasitics from the reload stage. Although the small M_5 and M_6 will also slow down the reload action, no high-speed operation is required for that. As mentioned previously, the Reload signal T_2 is close to 2 ns, which is sufficient for reloading the signal.

C. Mixer and DA

The function of mixer in the proposed design is twofold: one is to switch on–off the K-band LO and the other is to generate the BPSK modulation signal. Fig. 7 shows the circuit configuration and also the operating principle. When the value of the pulse-width chain becomes "0," the outputs of encoder A and B $(\mathrm{A} = 0, \mathrm{B} = 0)$ can switch the mixer off. When that changes to "1," the bi-phase control chain can control the phase of mixer



(a)



(b)

Fig. 10. Simulated: (a) output waveform and (b) normalized output spectrum of the UWB radar transmitter with 15-bit bi-phase modulation.

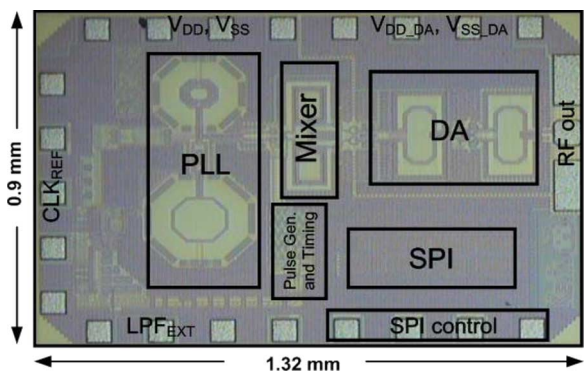
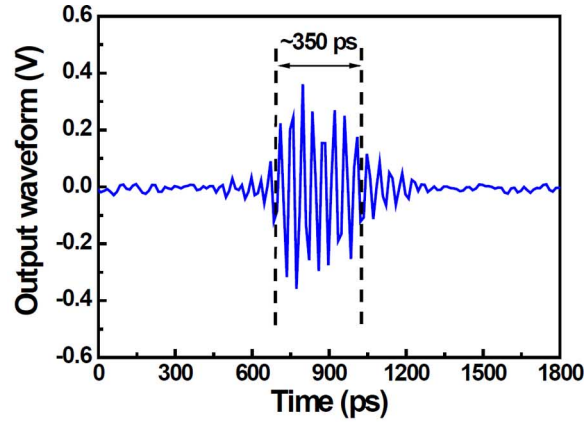


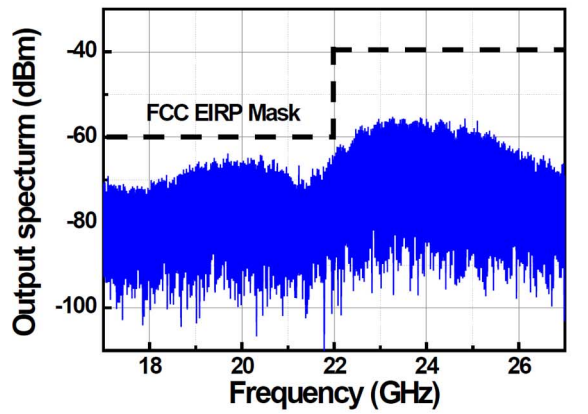
Fig. 11. Chip micrograph of the proposed K-band PC radar transmitter.

output. As illustrated in the figure, the phase can be either unchanged $(\mathrm{A}=1,\mathrm{B}=0)$ or switched $(\mathrm{A}=0,\mathrm{B}=1)$ for the output paths, which generates BPSK modulated signals. Based on the proposed mixer and encoder, the transmitter does not need an additional circuit to switch the LO signal, and the power consumption and chip area can both be reduced effectively.

Fig. 8 shows the DA, which is designed by a two-stage common-source amplifier topology to increase the output power and improve isolation of the mixer. The transformers are employed in the inter-stage and output for matching. A



(a)



(b)

Fig. 12. Single pulse waveform: (a) time domain and (b) frequency domain (RBW = 1 MHz).

stack configuration is used for the transformers TF_1 and TF_2 to increase the coupling factor. By adjusting the gate bias of the deriver amplifier, the output power of the PC transmitter can be tunable in a range from ~ 0 to 10 dBm. In addition, the pattern ground shield (PGS) technique for the inductive components is adopted in both mixer and DA design to reduce the substrate coupling from the voltage-controlled oscillator (VCO). It should be emphasized that the leakage signal from the VCO via the substrate even when the output of the transmitter is switched off can seriously degrade the circuit performance. The PGS technique provides a solution to this issue, resulting in much improved substrate isolation [13] for the individual blocks. The simple ground shield (SGS) technique [14] is adopted here, which is relatively easy for simulation and implementation. The SGS technique can improve Q of the inductor ($L = 1.33$ nH at 25 GHz) by about 27% compared with that without an SGS, as shown in Fig. 9.

D. PLL

The PLL of the transmitter is designed by the integrate-N architecture for high-frequency operation, which includes the LC-tank-based VCO, divider chain by 512, phase-frequency detector (PFD), and charge pump (CP). The off-chip components are used for the loop filter to reduce chip size. Based

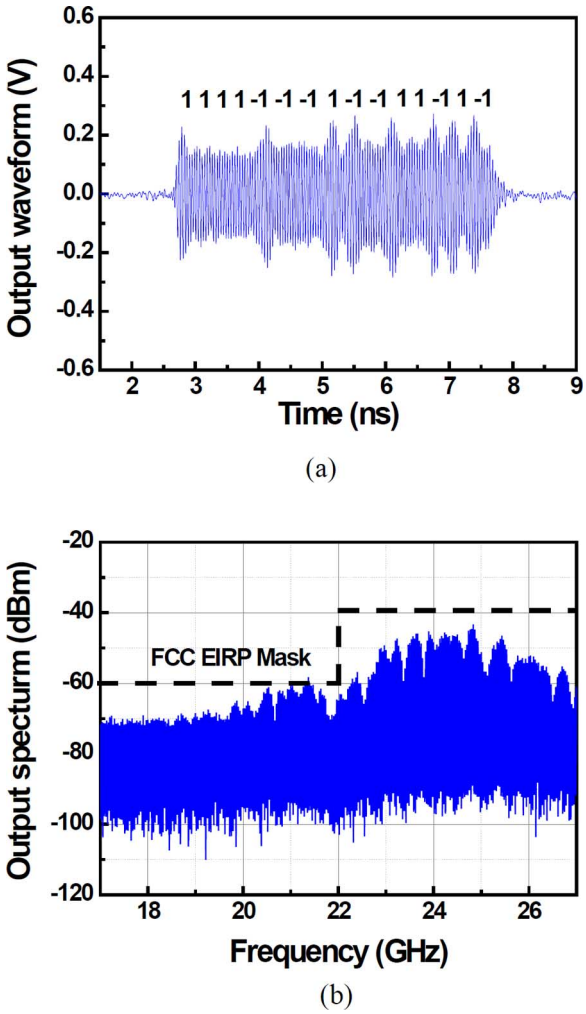


Fig. 13. Output waveform with pulse compression by 15-bit BPSK at clock of 3.136 GHz: (a) time domain and (b) frequency domain (RBW = 1 MHz).

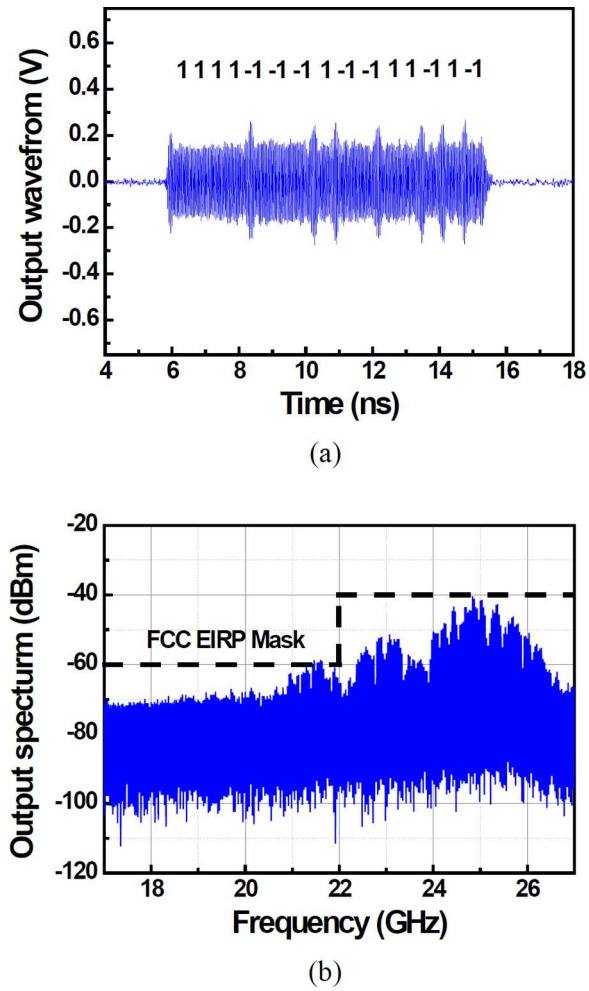


Fig. 14. Output waveform with pulse compression by 15-bit BPSK at clock of 1.568 GHz: (a) time domain and (b) frequency domain (RBW = 1 MHz).

on the simulated results, the tuning range of the VCO is from 24.7 to 27.25 GHz, which can cover the desired operation of 25.088 GHz for the PLL. The ring-based injection-locked /4 divider [15] is employed for the first stage to reduce the area of the PLL. The divider can function in a frequency range from 19 to 27 GHz with a 200-mV signal injection based on the simulation. The second frequency divider is accomplished using the CML, and the low-frequency divider chain is realized by the extended true single-phase clock (E-TSPC). With the reference clock of 49 MHz, the true single-phase clock (TSPC)-based topology is adopted in the PFD design for high-speed operation, and the current steering technique is employed in the CP. In addition, the divider chain in parallel with the current-mode multiplexer provides the clocks for reconfigurable pulse generator at the divider output nodes of LO/8 and LO/16.

Fig. 10(a) and (b) shows the simulated output waveform and spectrum for the UWB radar transmitter, respectively. Note that the ideal signal sources are used for the LO and clock (LO = 25.088 GHz, clock = 3.136 GHz) to keep the simulation time reasonable. The simulated result of a modulated long pulse ($\sim$ 5 ns) indicates the expected bi-phase modulation in the output waveform. Also, the output spectrum shows a main lobe close to 6 GHz, which is the evidence of the extended spectrum due to pulse compression.

IV. Measurement Results

The proposed PC transmitter was realized by a 90-nm 1P9M CMOS process. The chip micrograph is shown in Fig. 11, where the chip size is 1.32 mm $\times$ 0.9 mm (1.188 mm^2) including the probing pads (active area is only 0.66 mm^2). The PC transmitter was mounted on a printed circuit board (PCB) with the dc bias supplied by bond wires using an external power supply. The RF characteristics were obtained on wafer using the probe station. The test chip also includes an SPI to provide the digital control signal. The time-domain transient waveform and frequency-domain characteristics were obtained using an Agilent DSOX92504A 80-GSa/s real-time scope and an Agilent E4440A 26.5-GHz spectrum analyzer, respectively. The loop bandwidth of PLL is close to 100 kHz and the operation range is from 24.37 to 26.98 GHz. With a supply voltage of 1.2 V, the reference clock is 49 MHz and the output frequency of the PLL is 25.088 GHz. Under the PLL locking condition, the phase noise is -96.15 dBc/Hz and the spur level is -44.25 dB. Fig. 12(a) and (b) shows the measured

TABLE I
PERFORMANCE SUMMARY OF THE K-BAND AUTOMOTIVE RADAR TRANSMITTER AND COMPARISON WITH PRIOR WORKS

	This work	[5]	[6]	[7]
Frequency (GHz)	25.088	24.125	25.5	24.18
Process	CMOS 90 nm	SiGe 0.13 μm	SiGe 180 nm	CMOS 130 nm
Phase noise at 1MHz (dBc/Hz)	-96.15	-104	-114	-104.14
Output power (dBm)	1.34 – 9.6*	3	14.5	0
Single pulse width (ns)	0.35	0.5-1	0.3-1	0.5-1.25
Pulse compression	BPSK 15 bit	No	No	BPSK 2 bit
Power consumption (mW)	109.2-182*	160	402.5	63
Integration of PLL	Yes	Yes	Yes	No

* Measured P_{out} and the corresponding P_{DC} the transmitter (calibrated by a cable loss of 9.14 dB at 25 GHz; 9.6 dBm is the maximum P_{out}). Note P_{out} can be adjusted by the gate bias in the driver amplifier.

single pulse in the time and frequency domains, respectively. Note that the resolution bandwidth (RBW) for the spectrum measurement was 1 MHz and the maximum frequency of the spectrum was limited by the measurement equipment. The single pulse is generated by enabling only 1 bit in the pulse width sequence chain. The injected clock frequency from the PLL is 3.136 GHz (25.088 GHz /8), and the pulse width is close to 350 ps. Fig. 13 shows the measured 15-bit BPSK pulse compression waveform, in which the 15 bits of register chain for the pulse-width sequence are all enabled and the maximum length sequence (MLS) code of (1111–1–1–11–1–111–11–1) is used for bi-phase control with a clock speed of 3.136 GHz. The total pulse width is close to 5.25 ns 5.25 ns $(350\ \text{ps} \times 15)$. Fig. 14(a) and (b) shows the measured results when the clock is changed to 1.568 GHz (LO/16). Note that the sidelobes in the two cases are all below the FCC EIRP mask in the measured frequency range. Also, it should be mentioned that the measured results shown in Fig. 13 have a very good agreement with the simulated results (see Fig. 10) regarding both the pulse width and the spectrum extension. Based on the measured results in both the time and frequency domains, the proposed K-band radar transmitter successfully demonstrated reconfigurable output PC waveforms with 15-bit modulation. Table I summarizes the performance of proposed K-band radar transmitter and comparison with prior works.

V. CONCLUSION

A K-band UWB reconfigurable PC radar transmitter in a 90-nm CMOS technology has been demonstrated. The compressed pulse can enhance the detection probability and resolution of radar simultaneously. By using the sense-amplifier-based shift registers with a parallel-in-serial-out function, a high-speed, low-power, and area-efficient pulse generator was realized. Compared with previous studies with only 2-bit BPSK design, the proposed automotive radar transmitter is capable of a 15-bit reconfiguration coding scheme with a modulation rate over 3 Gb/s. The measured results demonstrated correct output waveforms with the spectrum well confined under the FCC regulation. With the on-chip integrated PLL, the proposed K-band automotive radar transmitter can achieve a resolution of 5 cm with a maximum detection range of 24.5 m.

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Kai-Wen Tan (S'10) was born in Taipei, Taiwan, in 1984. He received the B.S degree from National Taipei University of Technology, Taipei, Taiwan, in 2006, and is currently working toward the Ph.D. degree in electronics engineering at National Tsing Hua University, Hsinchu, Taiwan.

In 2008, he was an Intern with the Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, where he was engaged in RF integrated-circuit design. His current research interests include millimeter-wave radar front-end circuit design and RF/analog integrated circuits.

An-Hsun Lo was born in Taoyuan, Taiwan, in 1990. He received the B.S. and M.S. degrees in the interdisciplinary program of sciences and electronics engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2012 and 2014, respectively.

His research interests include radio-frequency and millimeter-wave integrated-circuit designs.

Ta-Shun Chu (S'06–M'10) received the B.S. degree in civil engineering and M.S. degree in applied mechanics from National Taiwan University, Taipei, Taiwan, in 2000 and 2002, respectively, and the Ph.D. degree in electrical engineering from the University of Southern California, Los Angeles, CA, USA, in 2010.

In 2010, he joined the Department of Electrical Engineering, National Tsing Hua University, Hsinchu, Taiwan, as an Assistant Professor. His research interest is mainly focused on CMOS RF mixed-mode integrated-circuit and system design.

Shawn S. H. Hsu (M'04) was born in Tainan, Taiwan. He received the B.S. degree from National Tsing Hua University, Hsinchu, Taiwan, in 1992, and the M.S. and Ph.D. degrees from the University of Michigan, Ann Arbor, MI, USA, in 1997 and 2003, respectively.

He is currently a Professor with the Institute of Electronics Engineering and the Electrical Engineering Department, National Tsing Hua University, Hsinchu, Taiwan. In August 2014, he was appointed a Distinguished Professor with National Tsing Hua University. His current research interests include the design of monolithic microwave integrated circuits (MMICs) and RF integrated circuits (RFICs) using Si/III–V-based technologies. He is involved with the design, fabrication, and the modeling of high-frequency transistors and interconnects. He is also interested in heterogeneous integration using system-in-package (SiP) and 3-D integrated circuit (IC) technology for high-speed wireless/optical communications.