Ultracompact Inductorless Noise-Canceling LNAs in 40-nm CMOS Achieving 2.2-K Noise Temperature for Qubit Readout

Mahesh Kumar Chaubey, Yeke Liu, Yin-Cheng Chang, *Member, IEEE*, Po-Chang Wu, Hann-Huei Tsai, *Member, IEEE*, and Shawn S. H. Hsu, *Member, IEEE*

***Abstract*— This article presents two ultracompact inductorless low-noise amplifiers (LNAs) in 40-nm CMOS for cryogenic qubit readout. Both LNAs utilize an inverter-based input stage as the main amplifier, and LNA-I and LNA-II employ a complementary and common-source (CS) stage, respectively, as the auxiliary amplifier for achieving noise canceling (NC). LNA-I also incorporates self-forward body bias (SFBB) to counter V_{th} reduction and improve r_{out} during cryogenic operation, while LNA-II uses source-follower feedback(SFFB) to enhance gain and noise figures (NFs) without compromising input impedance matching. At room temperature (RT), LNA-I achieves a measured gain (S_{21}) of 25.6 dB and a minimum NF of 0.63 dB at 2 GHz. At 4 K, it demonstrates a measured gain of 29 dB and a minimum NF of 0.033 dB (corresponding to a noise temperature T_N of 2.2 K), along with a 3-dB bandwidth $f_{3\,dB}$ from 10 MHz to 3 GHz, while consuming 19.4 mW. LNA-II achieves a measured gain of 27 dB and a minimum NF of 1.16 dB at 0.5 GHz at RT. At 4 K, it demonstrates a measured gain of 30.2 dB and a minimum NF of 0.29 dB (T_N of 20 K), accompanied by a $f_{3\,dB}$ from 20 MHz to 4 GHz and with a total power consumption of 10.8 mW. The circuit only occupies an active area of 0.018 and 0.0072 mm^2 for LNA-I and LNA-II, respectively.**

***Index Terms*— CMOS, cryogenic, inductorless, low-noise amplifier (LNA), noise canceling (NC), quantum computing.**

I. Introduction

THE potential of quantum computing holds the promise to address intractable challenges widely recognized within the scientific community, such as molecular simulation, drug and material synthesis, and quantum cryptography [1], [2]. To enable the operation efficiency and reduce the system complexity of large-scale quantum computing platforms, it has been proposed to utilize the CMOS-based technology for the qubits [3], [4], [5]. CMOS-based technology promises to realize a large number of qubits on a single chip, a high level of integration with peripheral control readout circuitry, and cost effectiveness. However, the primary advantage of employing CMOS lies in its capacity to achieve complex circuits with the low power consumption and a compact footprint to meet the requisite system specifications for practical gate-based quantum computing. Furthermore, the system fidelity could be enhanced significantly by being physically closer to qubits and reducing the need for bulky RF cables, minimizing delay times, and reducing the requirement for filters and isolators [6], [7]. It has been demonstrated that the CMOS-based circuits can control 128 spin qubits on a single chip [8].

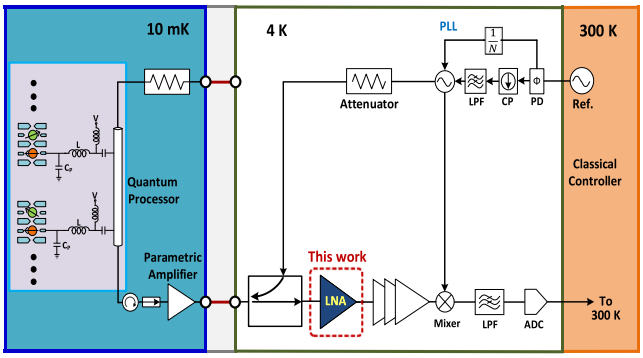

Fig. 1. Simplified block diagram of the readout system for qubits.

In the receiver chain for the qubits readout system, the low-noise amplifier (LNA) is the most critical front-end block to interact with qubits and amplify the weak RF readout signal. For optimal signal readout fidelity, the LNA must operate at deep cryogenic temperature with the lowest possible noise temperature, and also meet high power gain for suppressing noise from the subsequent receiver stage. Fig. 1 depicts the simplified block diagram of a typical qubit readout system. To detect an exceedingly weak modulated receiver signal, a parametric amplifier is essential, operating at the base temperature in proximity to qubits. The noise temperature T_N of the parametric amplifier can reach below 0.1 K with power consumption smaller than 1 mW [9], [10]. Nonetheless, the linearity of the parametric amplifier typically cannot attain the necessary level for amplifying the weak readout signal with the required gain. As illustrated in Fig. 1, it becomes

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Mahesh Kumar Chaubey, Yeke Liu, and Shawn S. H. Hsu are with the Department of Electrical Engineering and Institute of Electronics Engineering, National Tsing Hua University, Hsinchu 300, Taiwan (e-mail: shhsu@ee.nethu.edu.tw).

Yin-Cheng Chang, Po-Chang Wu, and Hann-Huei Tsai are with the Taiwan Semiconductor Research Institute (TSRI), National Applied Research Laboratories, Hsinchu 300, Taiwan.

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imperative to introduce an additional LNA for further amplifying the readout signal with a high gain and operating at higher temperate, typically 4 K. Owing to the superior RF characteristics, particularly at the cryogenic temperatures, this LNA for further signal amplification is primarily achieved by III–V compound semiconductors high-electron-mobility transistors (HEMTs) as reported in [11], [12], and [13] or using silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) [14], [15].

The cryogenic CMOS LNAs have attracted much attention recently. They have the potential to be fully integrated with CMOS-based qubits to realize practical quantum computers with an increased number of qubits. A Cryo-CMOS LNA in 14-nm FinFET technology, presented in a recent publication, showed a narrowband noise matching and achieved a relatively modest gain (S_{21}) of 13.4 dB at 4.1 K [16]. Utilizing 0.16-μm CMOS technology, an LNA can attain remarkable noise performance with a cryogenic noise figure (NF) close to 0.1 dB, but the circuit has a considerable power consumption of 54.9 mW [3]. Also, Sheldon and Belostotski [17] show an LNA realized in 65-nm CMOS with relatively large off-chip components, and the power dissipation is 125 mW at 20 K. A 40-nm CMOS LNA achieved a 3-dB bandwidth of 4.6–8.2 GHz with a low NF of 0.23–0.65 dB, consuming 39 mW at 4.2 K [18]. Note that most of the published papers employ inductors to augment RF characteristics, but the area consumption poses a significant challenge, particularly when considering qubit scalability. To achieve good input impedance matching with a wide bandwidth, LNAs can be designed using a common-gate (CG) configuration [19]. Nevertheless, this topology suffers from a relatively large NF for wideband design since the NF and input impedance are inversely proportional to transconductance g_m. The noise canceling (NC) configuration has been proposed, yielding low NF and high gain as demonstrated in [20] and [21]. This technique allows the nullification of channel thermal noise from the main amplifier using a second-path auxiliary amplifier.

Based on the concept of NC, this article proposes two inductorless LNAs in 40-nm CMOS and focuses on spin-qubit RF reflectometry of the receiver readout stage, covering the sub-gigahertz (GHz) frequency range for quantum signal processing. LNA-I features a complementary input stage employing self-forward body bias (SFBB) and an NC technique. Similarly, LNA-II is designed with a complementary input stage and leverages source-follower feedback (SFFB) to enhance gain and NFs without compromising input and noise-matching characteristics. The proposed cryogenic CMOS LNAs demonstrate excellent NF, gain, and bandwidth while operating under low power consumption with very compact footprints, which is beneficial in addressing the signal amplification challenges associated with qubit scaling. Notably, LNA-I attains a measured minimum noise temperature of only 2.2 K (at 4-K ambient temperature), while LNA-II occupies an active area of only 0.0072 mm^2. The obtained results are among the best compared with previously reported CMOS LNAs for quantum computer applications.

The rest of this article is organized as follows. Section II discusses the LNA design specifications for the spin qubits-based RF reflectometry readout receiver and design considerations with the device testkey under cryogenic operations. Sections III and IV provide insights into the circuit topology and in-depth analysis for LNA-I and LNA-II, respectively. Section V shows the measured and simulated frequency response and noise characteristics for both LNAs at room temperature (RT) and cryogenic temperature. Finally, a conclusion is drawn in Section VI. Note that a part of this article presents the extended work of the LNA-I originally presented in [22].

II. Design Considerations

A. LNA Specifications for Spin Qubit Readout

Fig. 1 depicts a conceptual plot of a spin qubit-based RF reflectometry receiver. A gate-based dispersive technique with simultaneous frequency multiplexing is a promising candidate for large-scale qubits readout. For qubit readout, by injecting an RF signal in the sub-GHz range to the gate of a quantum device with a notably high impedance, the capacitance at the gate will change depending on the state of a qubit [18], [23]. A high-quality factor matching network is essential to be well coupled to the high-impedance qubit input for 50-Ω impedance matching. The reflected signal from qubit is first amplified by the parametric amplifier operating in the range as low as tens of millikelvin. An additional LNA operating at 4 K is applied to further amplify the output RF signal of the parametric amplifier to identify the state of the qubits. Note that the typical frequency range used for spin qubit readout is 200–600 MHz [5]. The required overall receiver noise temperature T_{RX} can be estimated by the following Friis equation:

$$T_{\mathrm{RX}} = T_{\mathrm{Par}} + \left[\frac{T_{\mathrm{Phy}}}{G_{\mathrm{Par}}}\right] + \left[\frac{T_{\mathrm{LNA}}}{G_{\mathrm{Par}}G_{\mathrm{LNA}}}\right] \tag{1}$$

where T_{Par} and G_{Par} are the noise temperature and gain for the parametric amplifier, respectively, T_{phy} is the physical temperature of the circulator/isolator, and T_{LNA} and G_{LNA} are the required noise temperature and gain of the LNA at 4 K, respectively. Based on the parametric amplifier reported in [24], T_{Par} and G_{Par} at sub-1 GHz are 105 mK and 20 dB, respectively [24]. At a cryogenic temperature of 4 K, noise is mainly contributed by LNA and insertion loss of the circulator and isolator (∼0.3 dB) at sub-3 GHz [25]. Assuming a target receiver noise temperature T_{RX} is approximately 200 mK [23], T_{LNA} operating at 4 K can be estimated as approximately 3.5 K (corresponding NF of 0.05 dB). Also, the targeted gain of the CMOS LNA design is set to 30 dB to overcome the noise of the receiver stage. Note that the proposed LNA topologies can reach a very wide bandwidth, much larger than the required sub-GHz range, which is beneficial for reading out a large number of qubits in a frequency multiplexing system [26].

B. Noise-Canceling Topology of Inductorless LNAs

Fig. 2 depicts a simplified block diagram of an NC amplifier topology, including two signal paths of the main and auxiliary amplifiers, which are subsequently combined to achieve NC [27], where R_{S} is the input source resistance and R_{F} is

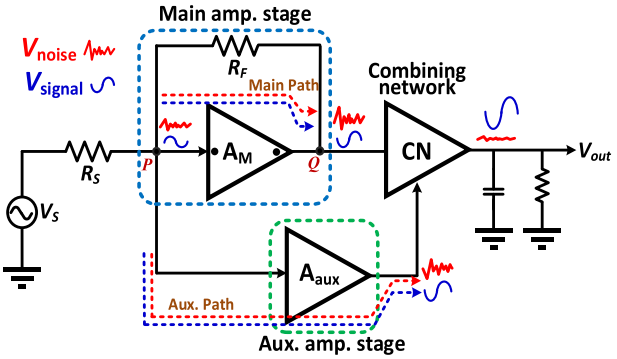


Fig. 2. Conceptual plot of the NC topology used for the proposed inductorless LNA.

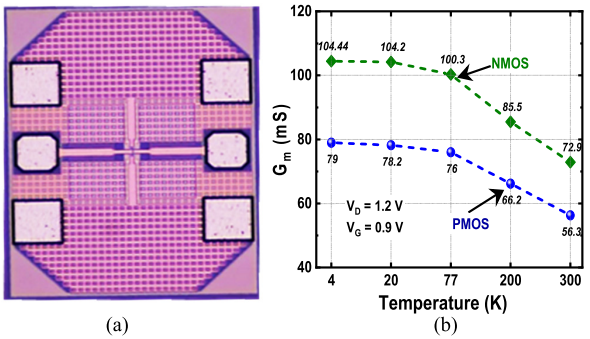


Fig. 3. (a) Micrograph of device testkey. (b) Measured transconductance g_m of transistors in saturation region at different temperatures.

the feedback resistance. Both of the inductorless CMOS LNAs are designed based on this concept.

As illustrated in Fig. 2, NC can be attributed to the signals from the main amplifier and auxiliary amplifier being in phase, and the noises from the two paths being out of phase. The out-of-phase signal and in-phase noise in the main amplifier can be accomplished by an inverting amplifier with a feedback resistor. As a result, in-phase signals are added while out-of-phase noise is canceled via the CN. Note that the noise current of the main amplifier (A_M) flows through R_F directly due to the high input impedance of the inverting amplifier, which creates in-phase noise voltages and out-of-phase signal voltages at nodes P and Q. In practical design, the main amplifier (A_M) could be a common-source (CS) configuration, which is an inverting amplifier with a large input impedance. The auxiliary amplifier (A_{aux}) could also be a CS stage. After being amplified, the signal and noise are both inverted since there is no alternative feedback resistor path for the input noise current.

The main function of CN is to add the signals from the two paths, which will not change the phase of either signal or noise in both paths. In practical design, this is often realized by a source follower, where the signal of the main amplifier is connected to the gate, while the signal of the auxiliary amplifier is connected to the source directly [21]. In the proposed design, the two LNAs have a similar complementary inverting input stage with a feedback resistor R_F, which functions as the main amplifier. The auxiliary amplifier in LNA-I also is with a complementary configuration, while that is a CS stage in LNA-II. The source follower is used for signal combing in both LNAs. More details will be described in Sections III and IV.

C. Design Considerations at Cryogenic Temperatures

The field of cryogenic electronics for quantum computing applications continues to advance rapidly, despite the absence of available compact CMOS models for the characterization of dc and RF behaviors at cryogenic temperatures. The proposed LNA design employs the standard process design kit (PDK) models provided by the foundry. However, certain concerns have been taken into account in circuit design to ensure proper operation at cryogenic temperatures. To investigate the transistor characteristics, three device testkeys have been implemented, including nMOS and pMOS transistors, and also an n-well poly resistor R_F. Fig. 3(a) shows the micrograph of an nMOS testkey with the G–S–G probing pads. Note that the transistor sizes for both the nMOS and pMOS are 90/0.12 μm, identical to those employed in the input inverter stage of LNA-I and LNA-II. Also, the resistor is around 1.2 kΩ, which is close to the feedback resistor R_F for the inverter input stage in both designs. At cryogenic temperatures, the threshold voltage (V_{th}) of the transistor increases due to the rise in the fermi potential, which is a consequence of incomplete ionization and the widening gap between semiconductor bands [28]. This increase in V_{th} leads to a change in expected biasing voltage and less headroom for the LNA. In the case of 40-nm nMOS with a size of 1.2 μm/40 nm (W/L), V_{th} exhibits an increase from 0.38 to 0.5 V as the temperature reduces from 300 to 4 K [29]. A similar trend can be observed from the implemented testkeys. The measured results indicate that V_{th} of nMOS increases from 0.32 to 0.42 V, while the pMOS exhibits an increase from 0.34 to 0.46 V as the temperature changes from RT to 4 K. It should be emphasized that the SFBB technique [30] is adopted for LNA-I to mitigate the impact of V_{th} increase at the cryogenic temperatures on circuit operation.

Fig. 3(b) illustrates the temperature-dependent transconductance g_m of both nMOS and pMOS transistors. g_m noticeably increases as the temperature decreases toward cryogenic levels. This can be attributed to a decrease in phonon scattering, which in turn elevates the transistor mobility by approximately a factor of 2 [29]. The results provide information to estimate the increase of overall transconductance $g_{m1} + g_{m2}$ (nMOS + pMOS) of the input inverter stage for both LNAs. The value increases from 129.3 to 183.4 mS as the temperature transitions from RT to 4 K. This explains the observed increase of gain at 4 K in the measured results, as will be shown later. Furthermore, Fig. 4(a) shows the measured output conductance (G_{ds}) of both transistors in the inverting input stage, maintaining a nearly consistent value between RT and 4 K. Fig. 4(b) shows the temperature-dependent variation of the resistance using n-well poly without silicide. A reduction of less than 10% is observed from RT to 4 K due to the relatively small change in the metal sheet resistance and poly at cryogenic temperatures.

Thermal noise is the main noise source in typical RF circuits, which reduces with the ambient temperature [31].

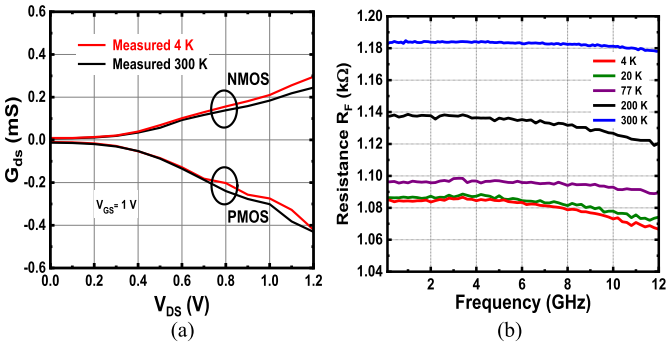


Fig. 4. (a) Output conductance (G_{ds}) of nMOS and pMOS at RT and 4 K. (b) Measured results of R_F testkey at different temperatures.

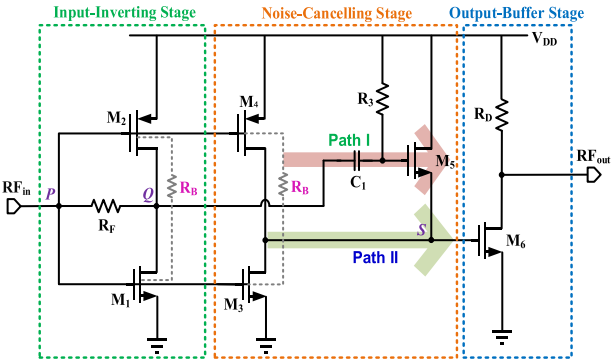


Fig. 5. Circuit topology of the proposed NC LNA-I [22].

However, the shot noise in CMOS could also play an important role at cryogenic temperatures. The results reported in [3] show an improvement in the noise temperature around eight times at 4.2 K, in [18] around three times at 4.2 K, and in [32] around six times at 4.2 K. Caglar et al. [32] and Hart et al. [33] suggest that this can be mainly attributed to shot noise and self-heating. In short-channel CMOS devices, shot noise becomes more predominant at cryogenic temperatures. It has been reported that shot noise primarily originated from the discrete nature of carrier transport across a potential barrier near the source within the short-channel devices [34]. This effect can be mitigated by selecting a longer channel length for the transistor, which reduces the quasi-ballistic carrier transport that contributes to shot-like noise in the channel [32]. Instead of using the minimum length of 40 nm, to mitigate shot noise, the proposed LNAs employ a channel length of 120 nm for the input stage for both LNA-I and LNA-II, while 60 and 100 nm are used for LNA-I and LNA-II, respectively, for the NC stage.

III. Design of Inductorless SFBB LNA (LNA-I)

A. Circuit Topology

Fig. 5 illustrates the circuit topology of the proposed LNA-I. This LNA encompasses three amplifier stages: the inverting input stage, the NC stage, and the postamplifier stage (output buffer stage). As shown in the figure, an inverter-based topology is employed as the input stage to mitigate the power dissipation with current reuse because power dissipation is crucial in quantum computing applications. It also helps to increase circuit linearity. Note that the nMOS and pMOS can be viewed as two stacked CS stages, with the drain nodes connected together, both functioning as the main amplifier in the NC topology (see Fig. 2). With the optimum sizes of the active devices, simultaneous noise, and input matching can be achieved using this topology. As depicted in Fig. 5, M_1 and M_2 constitute a complementary current reuse inverting input stage, and R_F can provide dc bias at point P through Q. To maintain V_{th} at cryogenic temperature, LNA-I is designed with an SFBB technique to compensate for the increased V_{th} at cryogenic temperature, keeping a similar V_{th} at RT to achieve low power operation at 4 K. That is by connecting the body bias resistor (R_B) between bodies of the complementary transistors M_1 (90 μm), M_2 (90 μm), M_3 (96 μm), and M_4 (144 μm) to form a voltage divider self-bias loop for the body-source p-n junction. With the properly designed value of R_B, the current I_B in this loop between the two body terminals of nMOS and pMOS can be controlled [35]. Using SFBB also allows for the alleviation of the output impedance reduction due to the cryogenic temperature and short-channel effect, which helps to provide more headroom for circuit gain and reduces the requisite value of V_{GS} for biasing. The simulated results in Fig. 6 indicate that r_{out} increases and I_B reduces with increased R_B of both transistors. R_B used in LNA-I is 1 kΩ in the actual design. The selection of size ratio of the input transistors M_1 and M_2 (for both LNAs) is 1:1 for simultaneous input and noise matching, which can also improve g_m to bias current ratio (g_m/I_d) for low power operation while keeping the bias voltage at node P as the desired value. However, the drawback of body biasing is increased power consumption due to leakage current I_B via the body nodes of the two transistors. Also, the degraded reliability is a concern due to the hot-carrier effects of the transistor [36].

The second stage is formed by current reuse NC inverting M_3 and M_4 for eliminating channel thermal noise of the inverting input stage, and M_5 (15 μm) is a source follower for combing the signal from the two paths. The noise after being amplified by the complementary transistors M_1 and M_2 (inverting operation), creates in-phase noise voltage and out-of-phase signal voltage at node P and node Q, respectively, through the feedback resistor R_F. The out-of-phase noise and signal voltage of node Q then enter the source follower M_5, appearing at node S (path I). On the other hand, the noise and signal voltages with the same phase at node P follow path II and are both amplified and inverted through the complementary transistors M_3 and M_4. As a result, the out-of-phase noise voltages cancel out at node S while the signal voltages are added up. Note that the size optimization of transistors in the NC stage is crucial for completely nullifying the channel thermal noise on the input stage. Without using an additional biasing circuit, the output buffer stage, employing M_6 as a CS amplifier stage, serves as the postamplifier stage to enhance gain and for 50-Ω output impedance matching.

B. Input Matching and Gain Analysis

The simplified small-signal equivalent circuit of the input stage is shown in Fig. 7. The input impedance Z_{in} of the proposed LNA while neglecting C_{gd} of the complementary

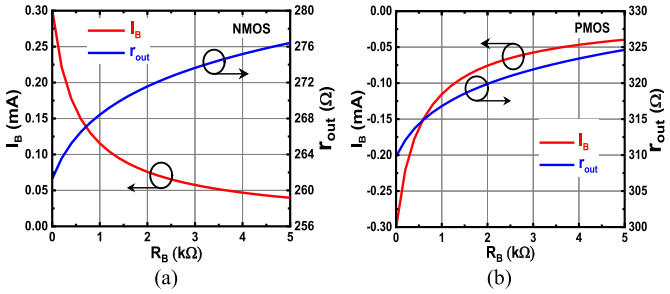


Fig. 6. Simulated results of substrate current I_B and output resistor r_{out} versus R_B. (a) nMOS. (b) pMOS [22].

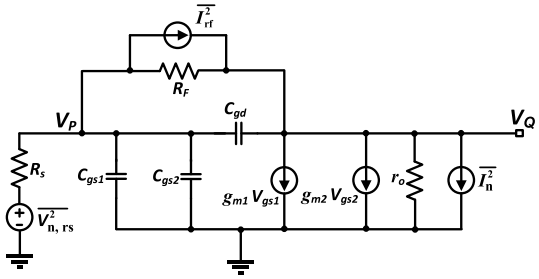


Fig. 7. Simplified small-signal equivalent circuit model of the input stage for LNA-I.

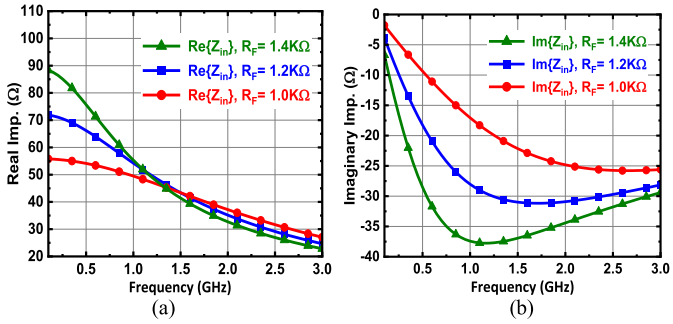


Fig. 8. Simulated input impedances of LNA-I with different feedback resistances R_F at RT. (a) Real impedance. (b) Imaginary impedance.

stage can be approximately expressed as follows:

$$Z_{\text{in}} = \left[\frac{(r_{01} \| r_{02}) + R_{\text{F}}}{\{1 + (g_{m1} + g_{m2})(r_{01} \| r_{02})\}} \middle\| \frac{1}{s(C_{gs})} \right] \tag{2}$$

where $C_{gs} = C_{gs1} \| C_{gs2}$. Note that the gate-to-source capacitance C_{gs} of complementary MOS limits the impedance matching at higher frequencies, whereas with the proper design of the feedback resistor and transistor sizing, good input matching can be achieved at low frequencies using the inverting configuration with a feedback resistor. Fig. 8 shows the simulated Re$\{Z_{\text{in}}\}$ and Im$\{Z_{\text{in}}\}$ of the proposed inductorless LNA-I with different values of the feedback resistor R_F. From (2), the real and imaginary parts of input impedance can be calculated as follows:

$$\text{Re}[Z_{\text{in}}] = \left\{ \frac{(r_0 + R_{\text{F}})(1 + G_{m1} r_0)}{(1 + G_{m1} r_0)^2 + \omega^2 (C_{gs})^2 (r_0 + R_{\text{F}})^2} \right\} \tag{3}$$

$$\text{Im}[Z_{in}] = -\omega \left\{ \frac{C_{gs} (r_0 + R_{\text{F}})^2}{(1 + G_{m1} r_0)^2 + \omega^2 (C_{gs})^2 (r_0 + R_{\text{F}})^2} \right\} \tag{4}$$

where $r_0 = r_{01} \| r_{02}$ and $G_{m1} = g_{m1} + g_{m2}$. Equation (3) indicates that Re$\{Z_{\text{in}}\}$ is positive and sensitive to R_{F} at low frequencies, which agrees well with Fig. 8(a). Equation (4) shows that Im$\{Z_{\text{in}}\}$ is negative which is consistent with the simulated results, as shown in Fig. 8(b). Furthermore, Im$\{Z_{\text{in}}\}$ changes obviously with different sizes of a feedback resistor R_{F} at low frequencies. The results imply that R_{F} is an important design parameter for input impedance. With a higher R_{F}, gain and NF can be improved but with the cost of input matching. The total voltage gain at low frequencies of LNA-I can be expressed as follows:

$$A_{\text{Total}} = A_{v,\text{core}} \times A_{v,\text{buffer}} \tag{5}$$

where $A_{v,\text{core}}$ and $A_{v,\text{buffer}}$ are

$$A_{v,\text{core}} = \left[g_{m5} \{1 - (g_{m1} + g_{m2}) R_{\text{F}}\} - (g_{m3} + g_{m4}) \right] R_{\text{out}} \tag{6}$$

$$A_{v,\text{buffer}} = g_{m6} (R_D \| R_L) \tag{7}$$

$$R_{\text{out}} = \frac{1}{\left[g_{m5} \| r_{o3} \| r_{o4} \right]} \approx \frac{1}{g_{m5}} \tag{8}$$

where R_{L} is the 50-Ω load and R_{out} is the output resistance at node S.

Note that the two LNAs have a similar complementary input stage with a feedback resistor R_{F}. A wideband 50-Ω matching can be achieved mainly by optimizing the value of R_{F}. As can be seen in the simulated results of LNA-I in Fig. 8. Also, LNA-II shows a similar trend. Different from conventional impedance noise matching, NF optimization is obtained by designing the size of the NC stage and feedback resistor R_{F}, as it will be shown in the following analysis. The NC condition can be obtained if the resistance and transconductance values satisfy the results of (13).

C. Noise Analysis

The main noise sources of LNA-I are the core MOS devices and feedback resistor (R_{F}). The channel thermal noise of the input stage and NC stage can be expressed as follows:

$$\overline{I_{n,\text{input}}^2} = 4 k_B T \frac{\gamma}{\alpha} (g_{m1} + g_{m2}) \tag{9}$$

$$\overline{I_{n,\text{NC}}^2} = 4 k_B T \frac{\gamma}{\alpha} (g_{m3} + g_{m4}) \tag{10}$$

where k_B is Boltzmann's constant, T is the absolute temperature, γ is the noise parameter of the transistor, and $\alpha = g_m / g_{d0}$. The simplified total noise-factor F of the core LNA (excluding the buffer stage) is

$$F = 1 + \frac{\frac{\gamma}{\alpha}(g_{m1} + g_{m2})}{R_S G_T^2} \left\{ \frac{g_{m5}\left(\frac{R_{\text{F}}}{R_S} + 1\right) - (g_{m3} + g_{m4})}{(g_{m1} + g_{m2}) + \frac{1}{R_S}} \right\}^2 + \frac{\frac{\gamma}{\alpha}(g_{m3} + g_{m4})}{R_S G_T^2} + \frac{\frac{\gamma}{\alpha}(g_{m5})}{R_S G_T^2} + \frac{R_{\text{F}} g_{m5}^2}{R_S G_T^2} \tag{11}$$

where G_T is the total transconductance of the core LNA

$$G_T = g_{m5} \{1 - (g_{m1} + g_{m2}) R_{\text{F}}\} - (g_{m3} + g_{m4}). \tag{12}$$

From Fig. 5, LNA-I can achieve the NC condition when [37]

$$\frac{R_S + R_{\text{F}}}{R_S} \approx \frac{g_{m3} + g_{m4}}{g_{m5}} \tag{13}$$

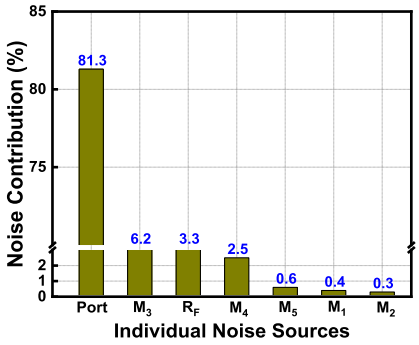


Fig. 9. Simulated noise contribution from source resistance and core transistors for LNA-I at 0.5 GHz.

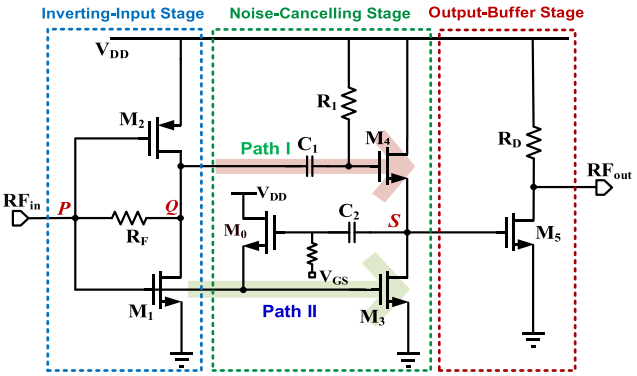


Fig. 10. Circuit topology of the proposed NC LNA-II.

where R_S is the source impedance (50 Ω) and g_{m3}, g_{m4}, and g_{m5} are the transconductance of transistors M_3, M_4, and M_5, respectively. From (13), the left-hand side (LHS) is the ratio of noise voltages at nodes P and Q, whereas the right-hand side (RHS) is the transconductance ratio of the NC stage. When the NC condition is satisfied with the required ratio and size of the NC stage, LNA-I achieves minimum NF. Fig. 9 shows the simulated noise contribution of the core transistor and feedback resistor of LNA-I at 0.5 GHz. The noise percentage contribution of the inverting input transistor (M_1 and M_2) is reduced due to the NC topology. The results indicate that the NC technique is effective, and the proposed LNA can achieve sub-1-dB NF at RT.

IV. Design of Inductorless SFFB LNA (LNA-II)

A. Circuit Topology

Fig. 10 illustrates the inductorless NC LNA-II using SFFB. The input inverting stage resembles that of LNA-I. However, unlike LNA-I which employs both nMOS and pMOS transistors (M_3 and M_4) in its auxiliary amplifier to cancel the input stage noise, LNA-II features a relatively simple CS auxiliary amplifier (M_3) as an NC auxiliary amplifier. In addition, the SFFB with transistor M_0 is incorporated. In contrast to LNA-I, LNA-II achieves notably reduced power consumption. This can be mainly attributed to the CS auxiliary amplifier with a single nMOS transistor instead of the complementary topology used in LNA-I. The size of M_3 in LNA-II (30 μm) is ~3× smaller than that used in LNA-I (96 μm). Furthermore, LNA-II does not have to body bias current due to the SFBB in LNA-I. On the other hand, LNA-II has higher NF compared with

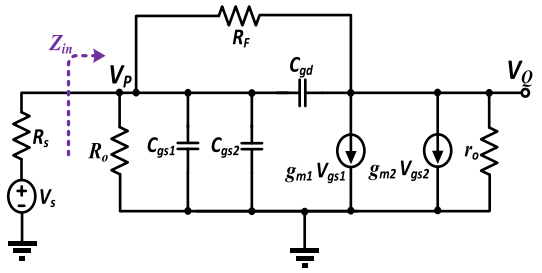


Fig. 11. Simplified small-signal equivalent circuit of LNA-II.

LNA-I since the complementary NC stage is more effective than the single CS stage in canceling channel thermal noise of input inverting transistors. However, with the SFFB technique, gain and NFs can be improved without the degradation of input impedance matching. Moreover, the active area is less as compared with LNA-I due to less active components.

B. Input Matching and Gain Analysis

The input stage is formed by inverting CS transistors M_1 (90 μm), M_2 (90 μm), and shunt feedback resistor R_F (1.0 kΩ) for self-bias between input and output. The transistor sizes of the inverting input stage are kept the same with LNA-I for achieving low NF. Note that R_F is slightly smaller than that employed in LNA-I for noise and input matching optimization due to the additional SFFB connected to the gate of M_1. Fig. 11 shows the simplified equivalent circuit model of the input stage for LNA-II, where $r_0 = r_{01} \| r_{02}$. Z_{in} can be expressed as follows by neglecting C_{gs} and C_{gd}:

$$Z_{in} = \left[\frac{\{r_0 + R_F\}R_0}{\{(g_{m1} + g_{m2})r_0 + 1\}R_0 + r_0 + R_F} \right] \tag{14}$$

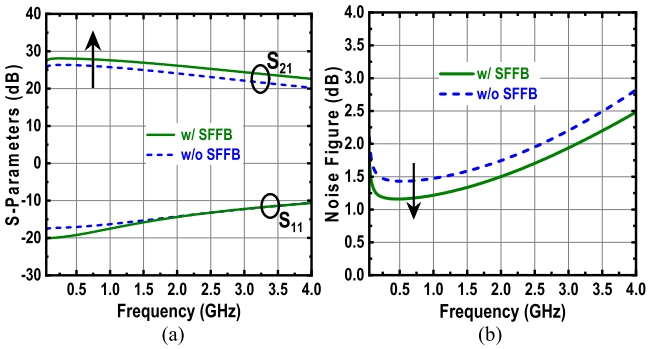
where R_0 is

$$R_0 = \frac{1}{g_{m0}\left(1 - \frac{V_Q}{V_P}\right)} \cong \frac{1}{g_{m0}} \tag{15}$$

where V_P and V_Q are the voltages at nodes P and Q, respectively. From (14), it can be seen that R_0 is added in parallel with the inverting input stage so that input impedance (Z_{in}) decreases without changing in transconductance of the inverting stage.

The second stage is the NC stage for eliminating channel thermal noise of the input main amplifier using the complementary topologies (M_1 and M_2) by the CS auxiliary amplifier M_3. From Fig. 10, the noise of the main amplifier after being amplified, creates in-phase noise and out-of-phase signal voltage at nodes P and Q with different amplitudes through the feedback resistor R_F. Noise and signal voltages at node P are (Path II) also amplified and inverted through the CS transistor M_3. Whereas, the noise and signal voltage of node Q enter the source follower M_4 (Path I) and appear at node S. Noise voltage is then canceled out due to the opposite polarity of noise voltage at node S, while the signal voltage is added up.

With an inverting input stage, as the feedback resistor R_F increases, gain, and NF can be improved effectively but with the cost of input matching due to the trade off between



(a) (b)

Fig. 12. (a) Simulated gain of LNA-II with and without SFFBs. (b) Simulated NF with and without SFFBs.

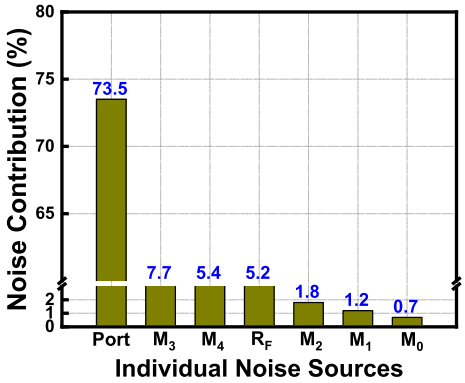


Fig. 13. Simulated noise contribution from source resistance and core transistors for LNA-II at 0.35 GHz.

the transconductance (g_m) of the inverting stage and input reflection coefficient S_{11} [27]. To mitigate input matching degradation with a large feedback resistor (R_F), SFFB is used in LNA-II to improve gain and NF while keeping desired input matching. The voltage signal at node S is feedback to the input of M_3 through transistor M_0(10 μm). Consequently, the overall gain is enhanced. As indicated in Fig. 11, the SFFB can improve the feedback resistance by adding a shunt load R_0 at the gate of the inverting input stage to mitigate the impact on input matching degradation when using a larger R_F to achieve high gain and low NF. Fig. 12 shows the comparison of the LNA-II with and without employing the SFFB configuration. The gain and NFs can be improved by 1.1 and 0.3 dB, respectively, than those without using the feedback stage in the LNA. The approximate calculation of the overall voltage gains from (5) is given by

$$A_{v,\text{core}} = \left[g_{m4}\{1-(g_{m1}+g_{m2})R_F\}-g_{m3}\right]R_{\text{out}} \tag{16}$$

$$A_{v,\text{buffer}} = g_{m5}(R_D \| R_L) \tag{17}$$

$$R_{\text{out}} = \frac{1}{\left[g_{m4}\|r_{o3}\right]} \approx \frac{1}{g_{m4}} \tag{18}$$

where R_L is the 50-Ω load and R_{out} is the output resistance at node S.

C. Noise Analysis

The noise of the proposed LNA-II is mainly contributed by the core MOS devices and feedback resistor (R_F), as shown in Fig. 13. By neglecting the noise contribution of SFFB transistor M_0 due to the very small transistor size, the simplified total noise factor (F) of the core circuit can be calculated by [also see (9) and (10)]

$$F = 1 + F_{M1} + F_{M2} + F_{R_F} \tag{19}$$

where F_{M1}, F_{M2}, and F_{RF} are

$$F_{M1} = \frac{\frac{\gamma}{\alpha}(g_{m1}+g_{m2})}{R_S G_{\text{core}}^2}\left\{\frac{g_{m4}\left(g_{m0}R_F+\frac{R_F}{R_S}+1\right)-g_{m3}}{(g_{m1}+g_{m2})+\frac{1}{R_S}+g_{m0}R_F}\right\}^2 \tag{20}$$

$$F_{M2} = \frac{\frac{\gamma}{\alpha}(g_{m3}+g_{m4})}{R_S G_{\text{core}}^2} \tag{21}$$

$$F_{R_F} = \frac{R_F g_{m4}^2}{R_S G_{\text{core}}^2} \tag{22}$$

where G_{core} is given by

$$G_{\text{core}} = g_{m4}\{1-(g_{m1}+g_{m2})R_F\}-g_{m3}. \tag{23}$$

From Fig. 10, the noise voltage at node S of opposite polarity cancels each other if LNA-II satisfies the following NC condition:

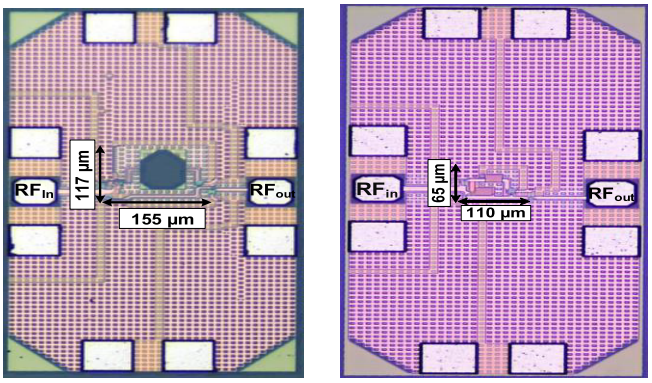
$$1+\frac{R_F}{R_S} \approx \frac{g_{m3}}{g_{m4}} \tag{24}$$

where g_{m3} and g_{m4} are the transconductance of transistors M_3 and M_4, respectively. From (24), the LHS is the ratio of noise voltages at nodes P and Q, whereas the RHS is the transconductance ratio of the NC stage. Fig. 13 shows the simulated results of the noise contribution at the maximum gain frequency of 0.35 GHz when LNA-II satisfies the condition of (24). Similar to LNA-I, the percentage of thermal noise contribution of the inverting input transistor (M_1 and M_2) is quite small due to the NC topology. However, the values are relatively higher compared with those observed in LNA-I. The results indicate that the complementary auxiliary topology is more effective for NC, which is consistent with the lower NF observed of LNA-I in both the simulated and measured results. Note that the noise contribution of SFFB transistor M_0 is only 0.7%, which suggests that neglecting M_0 in noise calculation in (19) is reasonable.

V. Measured Results and Discussion

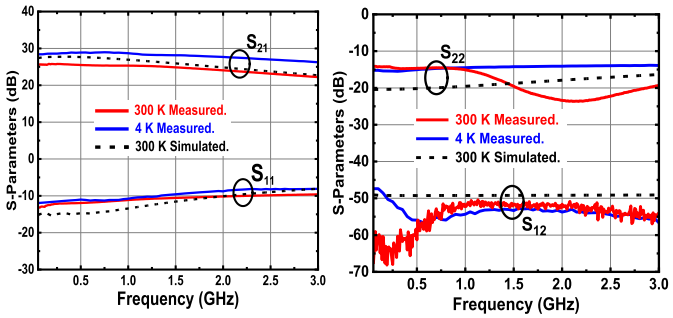
The proposed cryogenic inductorless LNAs were implemented in 40-nm CMOS technology. The chip micrographs are shown in Fig. 14(a) and (b) with an active area of only 0.018 and 0.0072 mm^2 for LNA-I and LNA-II, respectively. The S-parameters of both LNAs at RT were measured by on-wafer probing using the Keysight (N5247B PNA-X) vector network analyzer and NF using an Agilent N8975A NF analyzer.

Calibration up to the probe tip is critical to the cryogenic on-wafer measurements. Special designed microwave GGB Picoprobes were used for S-parameters and noise measurements in the cryogenic probe station. Each probe includes a pair of copper braids anchoring to the sample stage to cool down the probe. After probing, we waited for at least 10–15 min to ensure the probe's thermal stability before each measurement. The LNAs were measured on-wafer



(a) (b)

Fig. 14. Chip microphotographs of the inductorless LNAs in 40-nm CMOS. (a) LNA-I. (b) LNA-II [22].

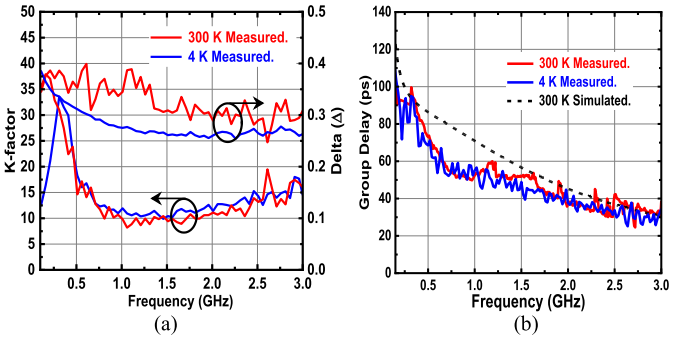


(a) (b)

Fig. 15. Measured and simulated results of LNA-I at RT and 4 K. (a) S_{21} and S_{11}. (b) S_{22} and S_{12} [22].

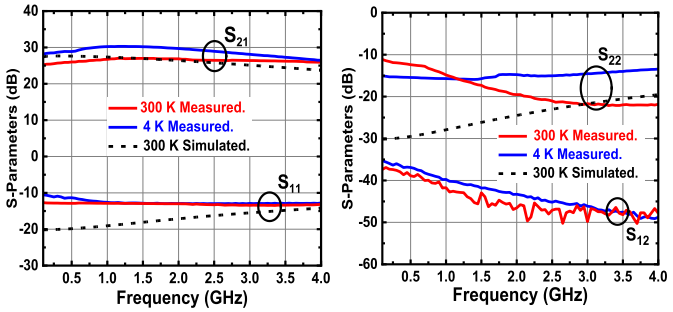
using a Lake Shore CRX-4K cryogenic probe station with the Keysight N5227B PNA-X for the S-parameters measurements. The on-wafer NF measurement was conducted by the Keysight N5242B PNA-X vector network analyzer with a built-in noise receiver using a vector-error-corrected cold-source method [38], [39]. The short-open-load-through (SOLT) calibration was performed using a GGB CS-5 calibration substrate to move the reference plane to the probe tips as proposed by Lake Shore [40], and the experimental results demonstrate the accuracy of SOLT calibration at cryogenic temperatures. A similar SOLT calibration approach was also reported for the cryogenic LNA measurement [18]. Note that the Lake Shore probe station was also used to measure S-parameters at 300 K in a vacuum chamber to verify the results obtained using the typical on-wafer measurement setup at RT. The LNA-I consumes a power of 43.4 mW from a 1.2-V power supply at RT and 19.4 mW at 4 K, while the LNA-II consumes power of 22.6 mW from 1.2-V power supply at RT and 10.8 mW at 4 K. It should be mentioned that one reason for the relatively high-power consumption for LNA-I at RT can be attributed to the SFBB technique, which can mitigate the impact of increased V_{th} and improve r_{out} under cryogenic operation. However, it also increases the power consumption due to the additional current flow in the body.

Fig. 15(a) and (b) shows the measured and simulated S-parameters of LNA-I at both RT and 4 K. At RT, LNA-I attains measured maximum $S_{21,max}$ of 25.6 dB at 0.8 GHz, f_{3dB} of a 10 MHz–2.7 GHz with S_{11} is better than −9.6 dB. At 4 K, the total bias current of input and the NC stage is



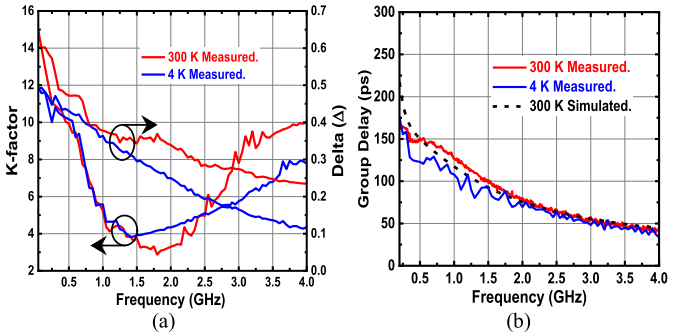
(a) (b)

Fig. 16. LNA-I. (a) Measured K-factor and delta at 300 and 4 K. (b) Measured and simulated GD [22].



(a) (b)

Fig. 17. LNA-II measured and simulated results at RT and 4 K. (a) S_{21} and S_{11}. (b) S_{22} and S_{12}.



(a) (b)

Fig. 18. LNA-II. (a) Measured K-factor and delta at 300 and 4 K. (b) Measured and simulated GD.

12.2 mA while the buffer stage consumes 4 mA. The circuit attains measured $S_{21,max}$ of 29 dB at 1 GHz, and with an excellent flatness in a 3-dB bandwidth of 10 MHz–3 GHz, and the corresponding S_{11} is in a range of −11.2 to −8.3 dB. Also, S_{22} is better than −15 dB and S_{12} is better than −50 dB in the 3-dB bandwidth. Fig. 16(a) shows the measured stability factor (K-factor) greater than 8 for both RT and 4 K, which indicates that the LNA is unconditionally stable. The overall measured group delay (GD) within the passband of LNA-I as shown in Fig. 16(b) is less than 90 ps for both 300 and 4 K, which agrees very well with the simulated results.

Fig. 17(a) and (b) shows the measured and simulated S-parameters of LNA-II at both RT and 4 K. At RT, it attains measured $S_{21,max}$ of 27 dB at 1.3 GHz, with S_{11} better than −12.6 dB over the 0.05–3.8 GHz 3-dB bandwidth. Whereas at 4 K, the total bias current of the input and NC stage is 5.8 mA while the buffer stage consumed 3.2 mA to keep a voltage gain higher than 30 dB. The LNA-II attains a measured $S_{21,max}$ of 30.2 dB at 1.2 GHz, within a 3-dB

TABLE I
PERFORMANCE COMPARISON SUMMARY WITH THE STATE-OF-THE-ART CRYOGENIC LNAS

Ref.	Technology	Topology	Frequency (GHz)	Inductor	Meas. Temp. (K)	Power (mW)	Gain (dB)	NF (dB)	S_{11} (dB)	Area (mm^2)
JSSC'18 [3]	160-nm CMOS	Noise-canceling	0.1 ~ 0.5	No	300	80	35 ~ 40	0.8 ~ 0.125	-9 ~ -5	0.249#
					4.2	91	50 ~ 58	0.1 ~ 0.85	-7 ~ -3	
TMTT'18 [12]	100-nm InP HEMT	3 Stage cascade	0.3 ~ 14	Yes	300	100	39.8 ~ 41.6	0.7 ~ 1.4	-22 ~ -1	1.5
					4	12	40.2 ~ 43	0.04 ~ 0.14	-22 ~ -6	
IMS'21 [14]	180-nm SiGe HBT	RC-feedback + CE	0.1 ~ 3	Yes	300	8	30	N/A	< -7	0.63
					15	1	27 ~ 32	0.07	< -7	
MWCL'22 [17]	65-nm CMOS	CS Folded-cascode	0.9 ~ 1.8	Yes	20	125	37.2	0.03 ~ 0.13	< -10	1
JSSC'21 [18]	40-nm CMOS	Cascode +R-C loading + XFMR load	4.1 ~ 7.9	Yes	300	51.1	35.5 ~ 36.5	0.75 ~ 1.3	-22 ~ -12	0.72
			4.6 ~ 8.2		4.2	39	39.2 ~ 44.8	0.23 ~ 0.65	-26 ~ -5.8	
JSSC'23 [32]	28-nm CMOS	Cascoded inverter + C-feedback + gate L	6 ~ 8	Yes	300	3.5	54*	2.5 ~ 3.5	< -6	0.2#
					4.2	4.2	N/A	0.4 ~ 0.7	< -4	
This Work	40-nm CMOS	Noise canceling + current reuse + SFBB	0.01 ~ 3	No	300	43.4	25.6 ~ 22.3	0.63 ~ 1.4	-13.1 ~ -9.6	0.018#
					4	19.4	29 ~ 26.1	0.033 ~ 0.8	-11.2 ~ -8.3	
This Work	40-nm CMOS	Noise canceling + current reuse + SFFB	0.02 ~ 4	No	300	22.6	27 ~ 25.2	1.16 ~ 2.2	-13.3 ~ -12.6	0.0072#
					4	10.8	30.2 ~ 26.9	0.29 ~ 0.91	-12.8 ~ -10.5	

*Simulated gain; #Core chip area.

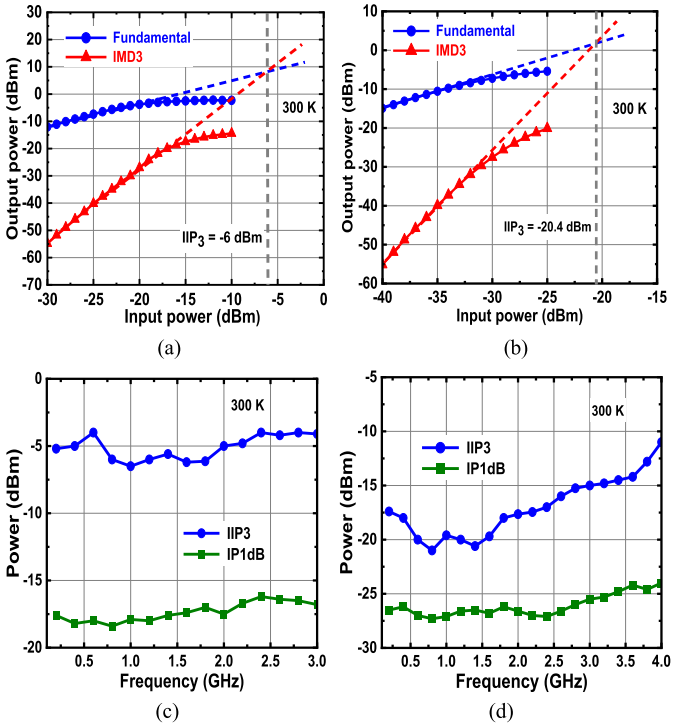


Fig. 19. Measured IIP3 at 10-MHz frequency spacing at 300 K. (a) LNA-I at 0.8 GHz. (b) LNA-II at 1.3 GHz. Measured IIP3 and P1dB versus frequency at 300 K. (c) LNA-I. (d) LNA-II [22].

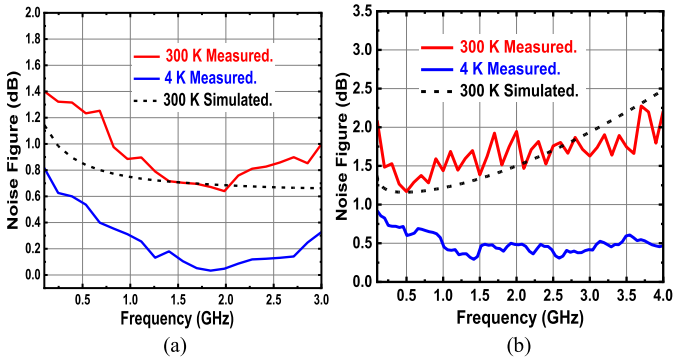


Fig. 20. Measured and simulated NF at 300 and 4 K. (a) LNA-I. (b) LNA-II.

bandwidth of 20 MHz–4 GHz. The input return loss (S_{11}) is <-10.5 dB, and the output return loss (S_{22}) is <-14.2 dB within this frequency range. Note that within the passband, the S-parameters also show excellent flatness both at RT and 4 K.

Fig. 18(a) shows the K-factor is greater than 3.1 for both RT and 4 K, which indicates unconditional stability at both temperatures. Fig. 18(b) presents the measured GD within the passband, which is found to be less than 170 ps for both 300 and 4 K. Fig. 19(a) and (b) shows the RT measured results of two-tone linearity (IIP3) for both LNAs at the frequencies of highest gain (LNA-I at 0.8 GHz and LNA-II at 1.3 GHz) with a two-tone spacing of 10 MHz. Fig. 19(c) and (d) shows the two-tone linearity and 1-dB compression point versus frequency sweep at RT for both LNAs. LNA-I shows better linearity compared with LNA-II, which can be mainly attributed to the complementary configuration used for the NC stage. It should be emphasized that the linearity level for both LNAs should be sufficient for the weak reflected RF power for the qubit readout.

Fig. 20 shows the measured NF for both LNAs at RT and 4 K. At RT, LNA-I attains NF of 0.63–1.4 dB with a

minimum value of 0.63 dB at 2 GHz, across 10 MHz–2.7 GHz, while LNA-II achieves NF between 1.16 and 2.2 dB with a minimum NF of 1.16 dB at 0.5 GHz, across 50 MHz–3.8 GHz. Both LNAs show good agreement between simulation and measurement results at RT. As frequency increases, matching becomes not as good for LNA-I since the parasitic capacitances of the transistors affect the matching at higher frequencies. At 2 GHz, the measured input return loss (S_{11}) of LNA-I is -8.7 dB at 4 K and -10.1 dB at RT, which is still reasonably good. It should be emphasized that S_{11} is not very critical for qubit readout due to the large isolation provided by the isolator between the parametric amplifier and LNA. At 4 K, the NF for LNA-I is lower than 0.4 dB from 0.7 to 3 GHz, and a minimum NF of 0.033 dB can be obtained at $\sim$1.8 GHz, corresponding to a noise temperature of only 2.2 K. On the other hand, at 4 K, for LNA-II achieves an NF smaller than 0.52 dB from 1 to 4 GHz, and the minimum NF is 0.29 dB at $\sim$1.4 GHz, which is equivalent to a noise temperature of 20 K. Note that, NF is increased for both LNAs at low frequencies due to the flicker noise ($1/f$ noise).

Table I shows the performance comparison of the cryogenic CMOS LNAs with the published LNAs. The proposed inductorless LNAs achieve a remarkable performance among the best compared with previously reported cryogenic LNAs. LNA-I attains a measured minimum noise temperature of only 2.2 K (0.033-dB NF), while LNA-II occupies an active area of only 0.0072 mm^2.

VI. Conclusion

In this article, we proposed two inductorless NC LNAs in the 40-nm CMOS technology with a very compact area. The inverter-based input stage was used as the main amplifier, while the complementary and CS stages were employed as the auxiliary amplifier for NC for LNA-I and LNA-II, respectively. LNA-I also incorporated the SFBB configuration to compensate for the threshold voltage increase and alleviate the degradation of output impedance at cryogenic temperatures. Furthermore, LNA-II utilized an SFFB stage to enhance gain and NF without degradation of input impedance matching. At 4 K, LNA-I achieved 0.033–0.8-dB NF, and a 29-dB gain from 10 MHz to 3 GHz with 19.4 mW of power consumption, while LNA-II attended 0.29–0.91-dB NF, and a 30.2-dB gain from 20 MHz to 4 GHz with 10.8-mW power consumption. The proposed ultracompact inductorless LNA design for spin qubit readout is promising to fulfill the demands of practical quantum computing applications with scaleup qubit numbers.

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Mahesh Kumar Chaubey received the M.Tech. degree (Hons.) in microwave electronics from the University of Delhi, New Delhi, India, in 2016. He is currently pursuing the Ph.D. degree in electronic engineering at the National Tsing Hua University, Hsinchu, Taiwan.

In 2016, he joined the MEMS and Microsensors Group CSIR-Central Electronics Engineering Research Institute (CEERI), Pilani, India, as a Project Research Fellow. His research interests include low-noise cryogenics CMOS receivers for qubit readout, design and modeling of microwave passive components, and RF MEMS-based filter design.

Yeke Liu received the B.S. degree in measurement and control technology and instruments from Hunan University, Changsha, China, in 2015. He is currently pursuing the Ph.D. degree in electronics engineering at National Tsing Hua University, Hsinchu, Taiwan.

His current research interests include the design and fabrication of GaN-on-Si microwave transistors, modeling and analysis of GaN-based devices, and cryogenic measurement.

Yin-Cheng Chang (Member, IEEE) received the Ph.D. degree in electronics engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2019.

He joined the National Chip Implementation Center, Hsinchu, in 2005. He is currently a Research Fellow and the Deputy Director of the Electronic Measurement Division, Taiwan Semiconductor Research Institute (TSRI), Hsinchu. His current research interests include monolithic microwave integrated circuit (MMIC) design in Si/GaN technologies, RF/mmW measurement techniques, signal integrity, power integrity, and IC electromagnetic compatibility.

Dr. Chang is a member of the Phi Tau Phi Scholastic Honor Society. He was a recipient of the Best Symposium Paper Award and the Best Poster Paper Award at Asia-Pacific International Symposium on Electromagnetic Compatibility (APEMC) in 2013 and 2017, respectively, and the Technical Achievement Award from the National Applied Research Laboratories in 2018.

Po-Chang Wu received the M.S. degree in communication engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1998, and the Ph.D. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2015.

In 2006, he joined the National Chip Implementation Center (CIC), National Applied Research Laboratories (NARLabs), Taipei, Taiwan, where he was an Associate Researcher and became a Principal Engineer in 2023. Since January 2019, he has been with the Taiwan Semiconductor Research Institute (TSRI), NARLabs, where he was the Leader of the Mixed-Signal Design Group, Heterogeneous Chip Integration Division. His research interests include low-power high-resolution data converters for wireless and wire-line communications, cryogenic circuit designs, and heterogeneous integration.

Hann-Huei Tsai (Member, IEEE) was born in Taipei, Taiwan, in 1970. He received the B.S. and M.S. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 1992 and 1994, respectively.

In 1996, he joined Taiwan Semiconductor Manufacture Company (TSMC), Hsinchu, Taiwan, as a Process Integration Engineer and became a Section Manager in 2002. In September 2006, he joined the National Chip Implementation Center (CIC), National Applied Research Laboratories (NARLabs), Taipei, Taiwan, where he was an Associate Researcher and he became a Research Fellow in 2009. Since January 2019, he has been with the Taiwan Semiconductor Research Institute (TSRI), NARLabs, where he was the Director of the Heterogeneous Chip Integration Division. He has authored or coauthored over 50 journals and conference papers and owns 38 patents. His current research interests include MEMS, bio-MEMS, silicon photonics, GaN power IC, heterogeneous integration, mixed signal, and power management circuits.

Mr. Tsai was a member of the Phi Tau Phi Scholastic Honor Society of Taiwan, in 1994. He received the First Prize in the Graduate Student Thesis Contest for the year from the Chinese Institute of Electrical Engineering.

Shawn S. H. Hsu (Member, IEEE) was born in Tainan, Taiwan. He received the B.S. degree from National Tsing Hua University, Hsinchu, Taiwan, in 1992, and the M.S. and Ph.D. degrees from the University of Michigan, Ann Arbor, MI, USA, in 1997 and 2003, respectively.

In 2003, he joined the Electrical Engineering Department, National Tsing Hua University, Hsinchu, as an Assistant Professor. In August 2014, he joined National Tsing Hua University, as a Distinguished Professor. He is involved in the design, fabrication, and modeling of high-frequency transistors and interconnects. He is also interested in heterogeneous integration using system-in-package and 3-D integrated circuit technology for high-speed wireless/optical communications. He is currently a Professor with the Institute of Electronics Engineering and the Electrical Engineering Department, National Tsing Hua University. His current research interests include the design of monolithic microwave integrated circuits (MMIC) and RF integrated circuits (RFIC) using Si-/III–V-based technologies.