Design of a Compact GaN MMIC Doherty Power Amplifier and System Level Analysis With X-Parameters for 5G Communications

Sih-Han Li, Shawn S. H. Hsu, *Member, IEEE*, Jie Zhang, and Keh-Ching Huang

***Abstract*— This paper presents a monolithic microwave integrated circuit Doherty power amplifier (DPA) operating at sub-6 GHz for 5G communication applications by a 0.25-μm gallium nitride high-electron mobility transistor process. A compact impedance inverter and output matching of the DPA are achieved using a transmission line network and shunt capacitors. Also, the size ratio of power cells in the main and auxiliary amplifiers is optimized for a high efficiency at output power backoff (OPBO). The measured peak output power (P_{out}) and the 1-dB compression point ($P_{1\,\text{dB}}$) are 38.7 and 32.1 dBm, respectively, at 5.9 GHz. The power-added efficiency at 6-dB OPBO is up to 49.5%. Without digital predistortion (DPD), the DPA can deliver an average P_{out} of 23.5 dBm with error vector magnitude (EVM) <-28 dB and 21.5 dBm with EVM <-32 dB for 64-quadrature amplitude modulation (QAM) and 256-QAM signals, respectively. The measured X-parameters are employed to further investigate the DPA nonlinear characteristics and verify the accuracy of conventionally used power amplifier characterization/measurement methods for system-level design and testing applications. The simulated results based on the X-parameters also indicate that the average output power can be enhanced up to 25.7 dBm with DPD for 256-QAM.**

***Index Terms*— 5G communication, Doherty, gallium nitride (GaN), monolithic microwave integrated circuit (MMIC), power-added efficiency (PAE), power amplifier (PA), X-parameters.**

I. Introduction

THE exponential growth of data communications over wireless networks is foreseen to continue into the next decade. The development of 5G communications is critical in the roadmap, and one of the main frequency spectrums is allocated at sub-6 GHz [1]. Compared with the current 4G local thermal equilibrium architecture, a major difference in the 5G blueprint is the widely deployed small cells such as femtocell and picocell for achieving ultradense networks. With numerous wireless transmitting devices, the power efficiency of these devices becomes a very important issue. One critical consideration to realize high-efficiency small cells is the power amplifier (PA) of the transmitter. The gallium nitride (GaN)-based transistors are excellent for such applications due to high-electron saturation velocity, high-channel carrier density, and large breakdown voltage [2].

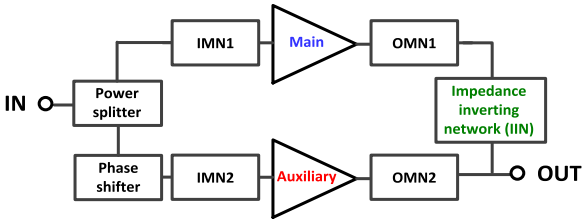

Fig. 1. Function blocks of the proposed DPA. The extra impedance converter connected at output (from 25 to 50 Ω) of traditional DPA can be removed using the 100-Ω system characteristic impedance in the output network.

The Doherty power amplifier (DPA) has proven to be an effective choice for achieving a high efficiency at output power backoff (OPBO) [3]–[9]. With the load impedances modulated by combining the main and auxiliary amplifiers via an impedance inverting network (IIN), this configuration allows obtaining a high-signal amplification efficiency with modulation schemes of high peak-to-average power ratio (PAPR). Note that these high PAPR schemes are widely employed in modern wireless communication systems [10]–[12].

In this paper, we design a sub-6 GHz MMIC DPA using 0.25-μm GaN high-electron mobility transistor (HEMT) technology provided by WIN semiconductor for small cell applications in 5G communications. We also perform in-depth system-level analysis to investigate the DPA nonlinearity by the measured X-parameters, which is different from the most reported results using the conventional approach with compact nonlinear transistor models [13]–[17]. Note that the design of the IIN and output matching network (OMN) is critical for achieving a compact size of DPA, as shown in Fig. 1. Compared with the traditional 50-Ω system, the 100-Ω design is used in the initial design phase to remove the extra impedance converter (from 25 to 50 Ω) at the output. Using the proposed impedance conversion technique and combine with the properly designed power cells, the limitation of the transmission line (TML) characteristic impedance Z_0 from the process can be overcome to simplify the output network. In addition to the design procedure partially presented in [18], more detailed system-level analysis is included in this

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extended version to verify the capability of proposed DPA. Both small-signal and large-signal S-parameters, and the measured results with the QAM quadrature amplitude modulation (QAM) modulated signal are presented. Also, more details about the simulation setup and methodology of X-parameters, and the comparison of system-level simulations based on X-parameters with and without digital predistortion (DPD) is included to enhance the correlation of X-parameters and the design and characterization of DPA. This paper is organized as follows. Section II describes the circuit design of the proposed DPA, including the input–output network and power cell selection. The simulated and experimental results including small-signal and large-signal are presented in Section III. Section IV provides measurements with modulated signal and detailed system-level analysis for the DPA based on the measured X-parameters. Section V concludes this paper.

II. Circuit Design and Analysis

The function blocks of the proposed DPA are shown in Fig. 1, including the power splitter, phase shifter, main and auxiliary amplifiers, input matching network (IMN)/OMN, and the IIN. To achieve a high-OPBO efficiency, the main amplifier is operated at class AB, while the auxiliary amplifier is biased at class C in a typical design. The auxiliary amplifier is turned OFF at low-power levels to maintain the efficiency during operation. In addition, the effective load can be modulated as a function of power level via the impedance inverter for high-power backoff power-added efficiency (PAE).

One of the challenges remains for MMIC DPA design is to obtain a compact on-chip output network design. In a typical design, the impedances of both main and auxiliary amplifiers are matched to 50 Ω at high-input power levels, and the IIN together with an additional impedance converter is essential to change the overall impedance back to 50 Ω for output terminal [19]. This methodology may introduce two issues in practical design. First, the TML-based impedance conversion elements could occupy a considerable chip area. Also, the available metal layers in IC process often cause limitations of the characteristic impedance Z_0 and current density for TML. In the proposed design, an IIN different from the typically used 50-Ω TML system is employed to solve these problems. With the 100-Ω TML system in the initial design, the extra impedance converter can be removed. Using the Δ–Y conversion, the network is further simplified by combining the IIN with OMN of the amplifier. In addition, the TML impedance is optimized to more practical values with the consideration of current density in the final design. Another critical point is the GaN power cell design in the main and auxiliary amplifiers, which is considered together with the IIN to achieve a compact and high-efficiency DPA. Note that the adopted 0.25-μm GaN technology is fabricated on a 4-mil (100 μm)-thick SiC substrate with the maximum drain current density and transconductance of 1040 mA/mm and 390 mS/mm, respectively. The suggested operation voltage is 28 V. An over 45% PAE was demonstrated in a continuous-wave mode at 10 GHz with output power density of 4 W/mm [20].

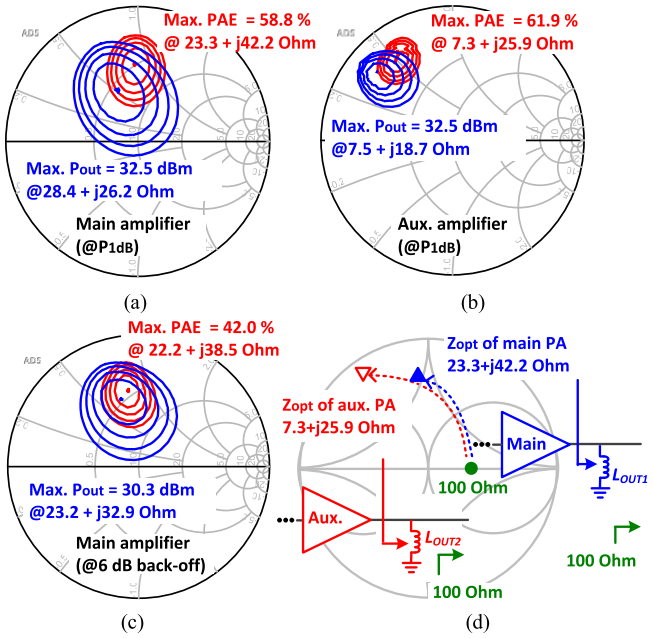

Fig. 2. PAE (solid line) and output power (dotted line) contours at $P_{1\,\mathrm{dB}}$ for (a) main amplifier and (b) auxiliary amplifier. (c) Contours at power back-off for the main amplifier. (d) Optimal loads and matching trajectories for the main and auxiliary amplifiers.

A. Design of Power Cells

The maximum output power level of the proposed DPA is aimed at about 10 W (40 dBm) for 5G small cell applications, and the transistor peripheries of the power cells are determined mainly based on this target. Also, obtaining high gain and high PAE simultaneously is an important design consideration of the DPA. It should be mentioned that a relatively large size ratio of the transistors in the auxiliary to main amplifier is necessary for high backoff PAE in DPA design [21]. The power cells selected in the main and auxiliary amplifiers are 6×100 μm and 12 100 μm with the corresponding f_T/f_{max} of 27/49 and 25/43 GHz, respectively. The load–pull simulation is performed under a certain power compression level to determine the large-signal optimal load impedance Z_{opt}. Note that the main design consideration is to find Z_{opt} for achieving maximum PAE. Thesimulated load contours for output power and PAE of the main and auxiliary amplifiers at P_{IN} of 20 dBm ($\sim$ corresponding to output $P_{1\,\mathrm{dB}}$) at 6 GHz are shown in Fig. 2(a) and (b), respectively. This is consistent with the actual operating condition as P_{IN} split by the 3-dB power divider, the actual input power for both amplifiers are equal, assuming the phase shifter has a negligible loss. The load–pull simulation is also performed under the OPBO condition for the main amplifier at P_{IN} of 14 dBm (6-dB backoff) as shown in Fig. 2(c). The corresponding Z_{opt} for maximum PAE is 22.2 + j38.5 Ω, which is very close to that of the output $P_{1\,\mathrm{dB}}$ condition [see Fig. 2(a)]. As a result, the optimum load impedances of the main and auxiliary amplifiers are chosen as 23.3 + j42.2 and 7.3 + j25.9 Ω, respectively, in our final design for maximum PAE at output $P_{1\,\mathrm{dB}}$, as shown in Fig. 2(d). As mentioned previously, the 100-Ω TML system

TABLE I
SIZE ESTIMATION OF PASSIVE TML ELEMENTS IN PROPOSED DPA

Network	TML (Z_0, θ_0)	Width/Length (μm/μm)
Phase shifter	50 Ω, 90 degree	100/4915
Wilkinson power splitter	70.7 Ω, 90 degree	40/5080
IIN	100 Ω, 90 degree	11/5230

is used to simplify the impedance conversion design. Based on the targeted output power level, the transistor size and bias are carefully selected to have proper Z_{opt} for both the main and auxiliary amplifiers. Therefore, Z_{opt} can be achieved by moving 100 Ω along the constant g circle with only two shunt inductors L_{OUT1} (OMN1) and L_{OUT2}(OMN2) as illustrated in Fig. 2(d). There is no need for extra LC components to compensate the real part and a compact OMN with high PAE can be obtained. More details about the codesign of IIN and OMN will be carried out after the discussion of TML design and input network in the adopted GaN technology.

B. Design of Input Network

As shown in Fig. 1, the power splitter and phase shifter are essential components in a DPA. The chip size becomes the main concern for MMIC implementation at sub-6 GHz if TML is used in the design. For example, the length of a 90° TML for the power combiner and phase shifter is around 5000 Ωm at 6 GHz, which occupies a considerable chip area and causes issues in the practical layout. More detailed size estimation for the main blocks of the proposed DPA in conventional TML design is summarized in Table I, based on the adopted GaN technology with a double-metal microstrip line structure.

The lump-type network is employed for the input network, which can significantly reduce the chip size of the proposed DPA. The conversion between TML and lump-type network is applied to design the input network for improving the area efficiency. A TML with an electrical length θ_0 and a characteristic impedance Z_0 at the operating frequency ω_0 can be converted to a lumped π network by two shunt capacitors C_{T} and one series inductor L_{T} [22]

$$L_{\text{T}} = \frac{Z_0 \sin(\theta_0)}{\omega_0} \tag{1}$$

$$C_{\text{T}} = \frac{\tan\left(\frac{\theta_0}{2}\right)}{\omega_0 Z_0} \tag{2}$$

$$Z_0 = \sqrt{\frac{L_{\text{T}}}{C_{\text{T}}} \frac{1}{2 - \omega_0^2 L_{\text{T}} C_{\text{T}}}} \tag{3}$$

$$\theta_0 = \cos^{-1}\left(1 - \omega_0^2 L_{\text{T}} C_{\text{T}}\right). \tag{4}$$

With this conversion method, the power splitter and phase shifter can be transformed into lumped networks, as illustrated in Fig. 3(a) and (b), respectively. The networks can be combined with the IMNs to effectively reduce the circuit size. Note that the IMNs are L-type matching networks in the proposed design.

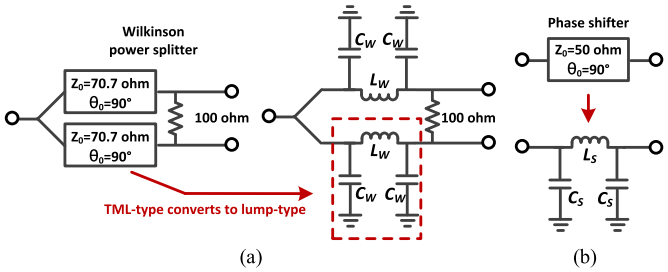

Fig. 3. TML to lumped element conversion (a) Wilkinson power splitter. (b) Phase shifter.

TABLE II
METAL LAYER RESISTIVITY AND MAX. CURRENT DENSITY [20]

Metal Layer	Resistivity (Ω/square)	Max. Current Density (mA/μm)
Metal 1	25×10^{-3}	6.2
Metal 2	5×10^{-3}	23.4
Double-metal	4.167×10^{-3}	29.6

C. Design of IIN and OMN

As illustrated in Figs. 1 and 2, the output network in the initial DPA design employs the 100-Ω Z_0 and 90° TML to simplify the design. However, in addition to the problem of low area efficiency, the narrow linewidth of 100-Ω TML becomes another key issue in the adopted GaN technology due to the high current density of DPA. Table II provides the related information for the metal layer resistivity and current densities in the adopted technology.

Based on Table I, the width of a 100-Ω TML is only around 11 μm. With the maximum dc current density of 30 mA/μm in a double-metal microstrip structure according to Table II, the total current can be supported by the 100-Ω TML is much lower than the desired current level (around 650 mA at high-power operating region). Based on the compact design method reported in [23], we propose a different solution to solve this issue with more flexibility, as shown in Fig. 4. First, the IIN is equivalent to a π network (L_{T} and C_{T}) as shown in Fig. 4(a), where C_{OUT1} and C_{OUT2} represent the equivalent output capacitances for the power cells, and L_{OUT1} and L_{OUT2} are the shunt inductors for the OMN of amplifiers [see Fig. 2(d)].

The π-type inductor network (L_{T}, L_{OUT1}, and L_{OUT2}) is then transformed to a Y-type network (L_{A}, L_{B}, and L_{C}) by the Δ–Y conversion [see Fig. 4(b)]. Next, two shunt capacitors (C_{ADJ1} and C_{ADJ2}) are added to the output nodes of the amplifiers, which allow implementing the TML with a lower characteristic impedance, and hence, a wider linewidth for the consideration of current density. Note that this also allows a compact MMIC layout, considering the adopted GaN technology, as shown in Fig. 4(c). Finally, the lumped network is converted back to TML-type design. As shown in Fig. 4(d), Z_{A} and Z_{B} are 75 Ω and Z_{C} is 60 Ω in the final design, corresponding to the linewidths of 35 and 65 μm, respectively. The electrical lengths of the TMLs are 23.4°, 11.9°, and 7.7°. The corresponding physical lengths of the TMLs are 1328, 673, and 430 μm for θ_{A}, θ_{B}, and θ_{C}, respectively. Different from the input network designed by the lumped elements, it should

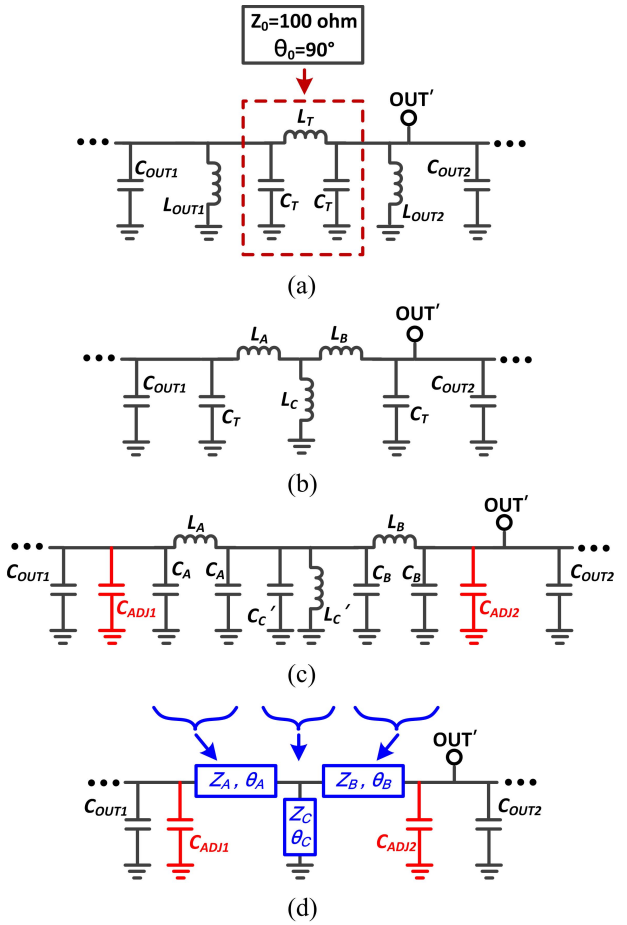

Fig. 4. Design of IIN and OMN by different impedance conversion techniques. (a) Equivalent IIN to a π network. (b) Use Δ-Y conversion to obtain Y-type inductor network. (c) Add two shunt capacitors to adjust the TML impedance in the next step. (d) Convert the lumped network back to TML-type design.

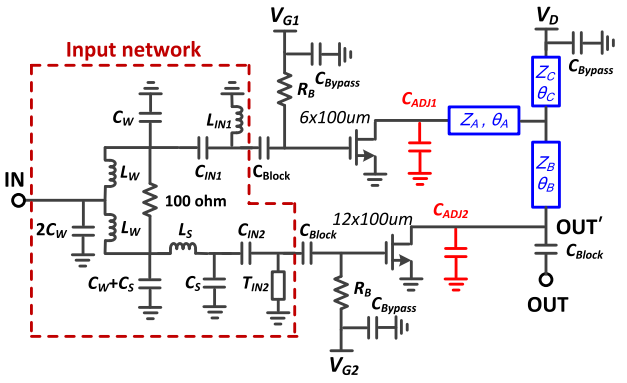

Fig. 5. Circuit schematic of the proposed DPA.

be emphasized that the main consideration of using the TML-type design for the output network is the current density. The metal width of spiral inductors with the desired values cannot meet the requirement. Also, the relatively low Q of spiral inductors will degrade the amplifier performance, especially the PAE. Fig. 5 shows the details of the overall circuit topology for the proposed DPA in the final design. Note that the bias resistances and bypass capacitors are added for gate voltage supply and circuit stability. The dc block capacitors are also

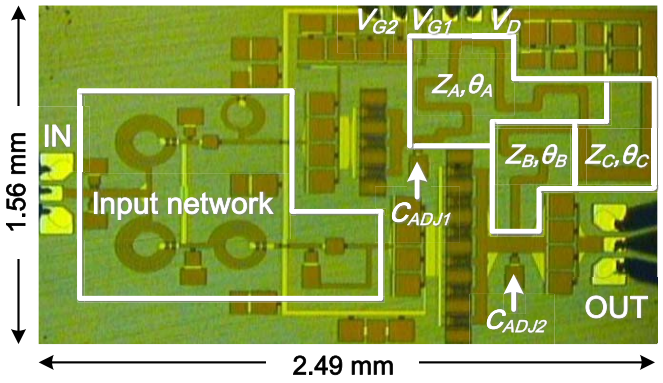

Fig. 6. Chip micrograph of the fabricated DPA in WIN 0.25-μm GaN technology.

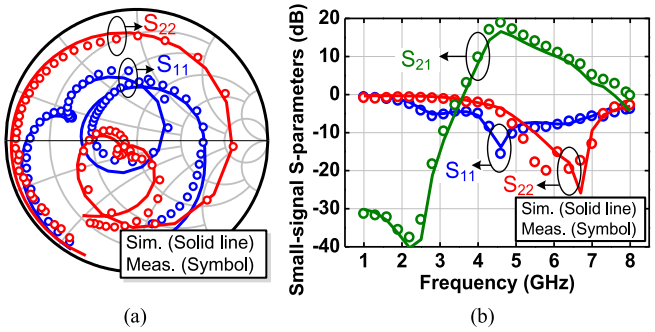

Fig. 7. Comparison of simulated and measured small-signal S-parameters of the fabricated MMIC DPA. (a) S_{11} and S_{22} in the Smith chart. (b) S_{11}, S_{22}, and S_{21} in the rectangular plot.

inserted for blocking dc bias path and coupling the ac signal. Note that these elements are all considered as a part of the DPA in electromagnetic (EM) simulation.

III. Measured Results and Discussion

Fig. 6 shows the chip micrograph of the fabricated DPA by 0.25-μm GaN technology with a chip size of 2.49 mm $\times$ 1.56 mm. The DPA is biased from a 28-V dc supply with a total dc current of 142 mA. Fig. 7(a) and (b) compares the measured and simulated small-signal S-parameters of the circuit from 1 to 8 GHz at an input power of -20 dBm. The input return loss of around 10 dB is obtained in a range of 4.3 to 4.9 GHz and the output return loss is larger than 10 dB from 5.1 to 7.0 GHz. The small-signal gain S_{21} of larger than 10 dB is achieved from 4.0 to 6.2 GHz. The measured results show excellent agreement under the small-signal condition, which demonstrates the accuracy of the nonlinear circuit model at a relatively low signal level. The results shown in Fig. 7 also prove that the EM simulation is accurate in our design.

It should be mentioned that the auxiliary amplifier is turned OFF at low-input power levels, thus the flatness of S_{21} is relatively poor due to mismatch. The large-signal S-parameters simulation in the simulation tool, Advanced Design System (ADS), is employed to investigate the S-parameters at different input power levels. The simulations are conducted in an input power range from -10 to 30 dBm, as shown in Fig. 8. As can be seen, the auxiliary amplifier gradually turns ON with the increased input power, and the

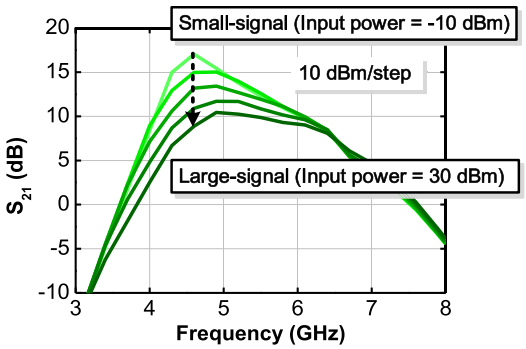

Fig. 8. Simulated S_{21} at the input power from −10 to 30 dBm.

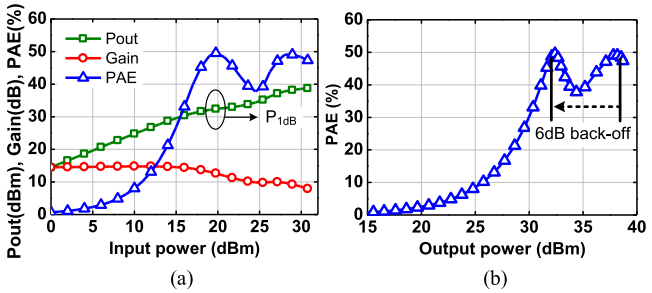

Fig. 9. Measured results of (a) P_{out}, gain, and PAE versus input power, and (b) PAE versus output power at 5.9 GHz.

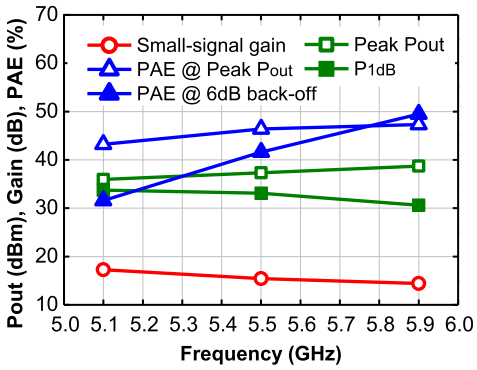

Fig. 10. Measured results of peak output power, $P_{1\,\text{dB}}$, small-signal gain, PAE at peak power, and 6-dB back-off PAE versus operating frequency.

flatness of S_{21} becomes better owing to improved matching condition. A flat linear gain S_{21} of around 10 dB is obtained from 4.6 to 6.0 GHz at an input power level of around 30 dBm. More results of large-signal measurements and analyses based on the measured X-parameters will be presented in Section IV.

Fig. 9(a) shows the measured DPA characteristics as a function of input power level at 5.9 GHz. A peak output power of 38.7 dBm with a PAE of 47.3% can be achieved. Also, the amplifier shows a $P_{1\,\text{dB}}$ of 32.1 dBm with an associated PAE of 48.8%. An excellent PAE up to 49.5% is obtained at 6-dB backoff output power, as shown in Fig. 9(b). Fig. 10 shows the measured results at different operating frequencies with high-output power levels. Over the frequency range from 5.1 to 5.9 GHz, the peak output power and $P_{1\,\text{dB}}$ remain above 35 and 31 dBm, respectively. The PAE at peak power is around 45% and PAE at 6-dB backoff is in the range of 32%–49%. The small-signal gain is around 15 dB in this frequency range.

IV. X-Parameters for System-Level Analysis

Circuit simulation with the nonlinear transistor model or direct chip measurement allows investigating the characteristics of PA operating with the modulated input signal. However, it is difficult to perform system-level analysis accurately during the design or testing phase of a system with the PA characteristics obtained by these two approaches. The pure simulation approach will encounter precision and time-consuming issues, whereas limitations exist for system-level analysis with the typical PA measurements such as $P_{\text{IN}}/P_{\text{OUT}}$, PAE, and error vector magnitude (EVM). In this paper, the X-parameters of proposed DPA are measured to obtain more complete nonlinear properties of the circuit, which can solve the above-mentioned issues. The X-parameters represent a set of nonlinear network parameters, which allow overcoming a key challenge of RF circuit design and analysis, such as nonlinear reflection effects, nonlinear impedance difference, and harmonic mixing under large-signal operation [24], [25]. The system-level simulations are performed by the measured X-parameters of the proposed DPA. In addition, the results are compared with those based on typical circuit simulation (nonlinear transistor model with EM simulation) and direct chip measurement with the modulated input signal. Since the X-parameters contain the characteristics of distorted amplitude and phase vectors, the interaction of the DPA and other circuit blocks in the system can be predicted based on these characteristics. With the X-parameters, not only the adjacent channel power ratio (ACPR) of the DPA can be predicted accurately but also how the ACPR changes as other components inserted into the signal path can be estimated [26]–[28]. As long as the X-parameters of the constituent nonlinear elements in the signal path are known, the overall nonlinear characteristics of the system can be accurately calculated during the design phase, which provides an efficient and accurate assessment for system design with nonlinear PA [25]–[28].

Three methods are employed to verify the characteristics of the proposed DPA with the modulated input signal, including: 1) nonlinear transistor model with EM simulation in ADS Verification Test Bench (VTB); 2) direct chip measurement with the vector signal generator and analyzer; and 3) measurement-based model of the DPA established by the X-parameters in ADS VTB. The measurement setup and system simulation based on X-parameters is illustrated in Fig. 11. Note that the static model is adopted without considering memory effect in the X-parameters measurements for simplicity. Also, the fundamental frequency is set from 5.1 to 5.9 GHz with the input power level from −10 to 25 dBm (1 dBm/step). The maximum harmonic tone is set to three limited by the preamplifier bandwidth, and the number of phase offset extraction tones is 4 (0°, 90°, 180°, and 270°). Also, a 30-Hz intermediate frequency bandwidth is used, and a 10-dB gain at maximum input power is adopted to use the gain-based setting for autogeneration of the extraction tone level by the VNA instrument (N5242A). Note that a preamplifier is added before the input of the DPA and attenuators are also used after the output to obtain the desired power levels for the measurements, and these components are all taken into consideration in the calibration procedure.

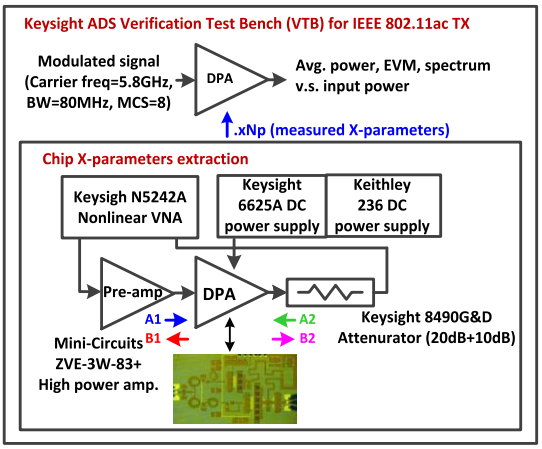

Fig. 11. Measurement setup of X-parameters and configurations of system simulation based on X-parameters in VTB for the proposed DPA.

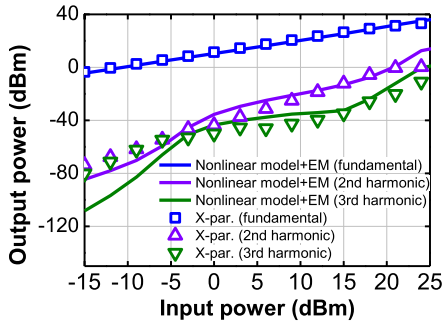

Fig. 12. Measured output power at fundamental and harmonic frequencies at 5.8 GHz.

Fig. 12 compares the output power as a function of P_{IN} between methods (1) and (3), including fundamental (5.8 GHz), second-, and third-harmonic frequencies. As can be seen, a good agreement can be obtained for the fundamental tone. In contrast, noticeable discrepancies exist for the second and third harmonics, especially when the input power is less than about −3 dBm and greater than 20 dBm. The trend observed here is consistent with the EVM simulation based on the QAM input signal as will be shown later.

The system-level characterization is performed by method (2) (direct chip measurement) to verify the capability of the proposed DPA operating with the modulated signal over a certain bandwidth. The input signal with a frame format of 802.11ac (64- and 256-QAM with an 80-MHz bandwidth) at 5.8 GHz is applied without using any DPD techniques. The average output power levels with the path loss compensated are about 23.5 dBm (EVM <−28 dB) for 64-QAM, and about 21.5 dBm (EVM <−32 dB) for 256-QAM, respectively. Fig. 13 shows the measured output spectrum with the 256-QAM input signal and EVM performance at an input power of 10 dBm. Note that the higher order QAM modulation exhibits larger PAPRs and requires more rigorous EVM; therefore, the average output power with the 256-QAM modulated signal is lower than the 64-QAM modulated signal.

Based on the measured X-parameters, the input signal with a frame format of 802.11ac (256-QAM, 80-MHz bandwidth,

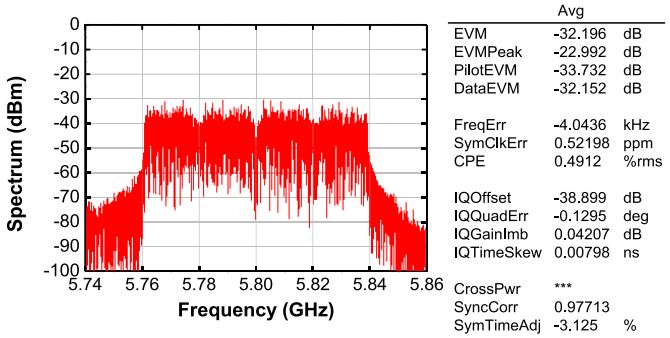

Fig. 13. Measured results with the 256-QAM input signal (802.11ac format and an 80-MHz bandwidth) at 5.8 GHz. The output spectrum is with an average output power level of 21.5 dBm (EVM <−32 dB).

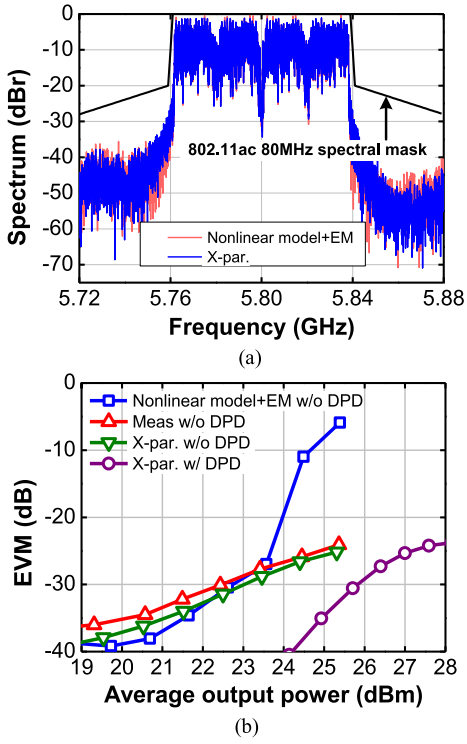

Fig. 14. System-level characterization results at 5.8 GHz (256-QAM). (a) Normalized spectrum at EVM < −30 dB and average output power around 22.5 dBm. (b) EVM versus average output power.

MCS index = 8, coding rate = 3/4, and data rate = 351 Mb/s) at 5.8 GHz is applied for simulation without using any DPD. With EVM increased to −30 dB for 256-QAM, Fig. 14(a) shows the comparison of the obtained output spectrums between the nonlinear model with EM [method (1)] and X-parameters [method (3)], where the average output power are about 22.5 dBm. As can be seen, the two spectrums both pass the 802.11ac spectral mask. Note that the relative constellation error must be less than −30 dB as MCS index = 8 in the IEEE 802.11ac protocol. Fig. 14(b) shows the EVM as a function of average output power with the three methods, which suggests that the results based on X-parameters are consistent with the direct chip measurements. On the other hand, the EVM by the pure simulation using nonlinear transistor model with EM postsimulation shows an obvious discrepancy

TABLE III
COMPARISON WITH PRIOR WORKS OF GAN MMIC

Ref.	Tech.	Freq. (GHz)	Small-signal gain (dB)	Peak P_{out} (dBm)	P_{1dB} (dBm)	PAE at Peak P_{out} (%)	PAE at 6dB back-off (%)	P_{out} with 256 QAM (dBm)	Chip-Size (mm×mm)
[13]	GaN 0.25 μm	5.8–8.8	7.5–10	36	30	28–44	31–45	--	2.9 × 2.9
[14]	GaN 0.25 μm	2–6	12.8–13.7	41	--	27–34	--	--	4.0 × 1.9
[15]	GaN 0.25 μm	6–18	13.5–19.1	35.7–37.5	--	13–21	--	--	3.3 × 2.5
[23]	GaN 0.25 μm	6.8–8.5	13.5	35	22	38–50	35	--	2.1 × 1.5
[29]	GaN 0.25 μm	14.6	7	36	30	40[#]	28[#]	29.0*	3.1 × 1.6
[30]	GaN 0.25 μm	6.6–7.3	10	38	27	47.5	41	--	5 × 5
[31]	GaN 0.15 μm	10	9.2	36	35	47	42	--	3.8 × 2.3
This Work	GaN 0.25 μm	5.1–5.9	14.4–17.3	36.0–38.7	33.8–32.1	43.2–47.3	31.6–49.5	25.7[+]	2.49 × 1.56

[#]Drain efficiency; *only pass spectral mask; [+]pass spectral mask and RCE at 5.8 GHz

in both relatively low and high P_{out} ranges. The trend agrees very well with that shown in Fig. 12. The error in low-power level may be attributed to the difficulties to accurately model the relatively weak nonlinear behavior of transistor under such low-power conditions. In addition, the transistor becomes very nonlinear in the high-output power region, and both the harmonic distortion and thermal effect make precise modeling by equivalent circuits very challenging. One point should be emphasized is the thermal effect. The thermal parameters in the model were extracted by the transistors measured on the whole 4-in SiC wafer as consulted with the foundry (WIN semiconductor), which can serve as an excellent heat sink. However, the MMIC PA was measured on-wafer directly with a small die size. The ambient thermal conductivity is quite different, and hence, the actual thermal effect deviates from the model prediction. In contrast, the X-parameters are measured based on the actual PA chip, not only the thermal effect of a single-power cell but also the thermal interaction between the main and auxiliary power cells are taken into account. Compared with the results using a nonlinear model with EM [method (1)], the system-level simulation based on X-parameters [method (3)] shows much better agreement with the direct measurement results, especially at high output power levels as shown in Fig. 14(b).

Based on the measured X-parameters, simulations are performed for the proposed DPA to investigate the enhancement in circuit linearity with DPD. There are different options for using the DPD function in the software. The commonly used approaches are based on polynomials derived from Volterra series or lookup table (LUT). The main considerations are the fast convergence and low complexity for actual implementation. The LUT approach has generally lower complexity and is suitable for PAs with relatively more linear characteristics. In contrast, using the polynomials allows modeling the more complex behaviors for highly nonlinear PAs and obtaining more enhanced performance with DPD [32]. The LUT approach is adopted here for simplicity in the simulation tool (Keysight SystemVue). The DPD was set to use eight times oversampling, 512 LUT size, 1-ms sample length, 0.25-dB LUT step, and the input signal was clipped at 10-dB PAPR. As shown in Fig. 14, the results indicate that the average output power can be enhanced from 23.0 to 25.7 dBm with EVM <-30 dB for the simulated results based on X-parameters with DPD. Fig. 15 compares the spectrums with and without applying DPD by the measured X-parameters using a 256-QAM signal of 80-MHz bandwidth at a 5.8-GHz carrier frequency.

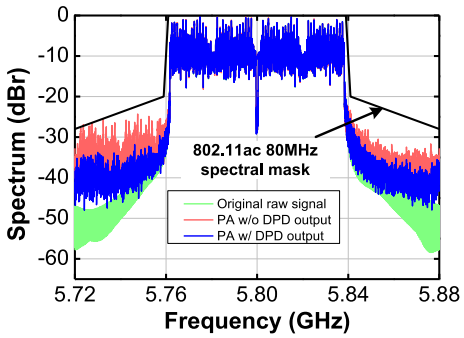

Fig. 15. Simulated normalized spectrums with and without DPD by X-parameters using a 256-QAM signal of 80-MHz bandwidth at a 5.8-GHz carrier frequency (EVM <-30 dB; average output power = 25.7 dBm).

By these circuit- and system-level characterization results, the performance of the proposed DPA has been investigated in detail. The features of proposed DPA are summarized in Table III. As can be seen, the DPA can support applications requiring linear amplification at sub-6 GHz. Compared with previously reported results in a similar GaN technology, this paper shows the highest 6-dB OPBO PAE and the highest PAE at $P_{1\,dB}$ with a very compact area. Also, the output power level and gain are among the highest.

V. CONCLUSION

A high-performance sub-6 GHz MMIC DPA for 5G communications was demonstrated in 0.25-μm GaN HEMT technology. Using the proposed design techniques, a very compact TML output network can be achieved and the limitation of TML characteristic impedance and current density in the adopted technology can be overcome successfully. The measured results showed a maximum output power up to 38.7 dBm and the PAE at a 6-dB backoff P_{out} can achieve 49.5%, which is among the highest compared with previous works in a similar GaN technology. The system-level characterization was also performed in detail by different approaches including the X-parameters. Without DPD, the average output power levels

with sufficient EVM quality are about 23.5 and 21.5 dBm for 64- and 256-QAM modulated signal, respectively. With DPD, the average output power levels can be enhanced up to 25.7 dBm for 256-QAM. In addition, the simulation based on measured X-parameters showed excellent consistency with the direct chip measurement for EVM. The results indicate that extraction of X-parameters is a powerful tool for effective and accurate system level codesign with nonlinear circuit blocks such PAs.

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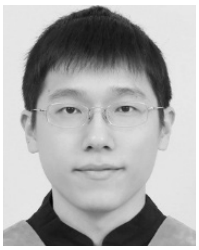

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