A Multi-ESD-Path Low-Noise Amplifier With a 4.3-A TLP Current Level in 65-nm CMOS

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***Abstract*—This paper studies the electrostatic discharge (ESD)-protected RF low-noise amplifiers (LNAs) in 65-nm CMOS technology. Three different ESD designs, including double-diode, modified silicon-controlled rectifier (SCR), and modified-SCR with double-diode configurations, are employed to realize ESD-protected LNAs at 5.8 GHz. By using the modified-SCR in conjunction with double-diode, a 5.8-GHz LNA with multiple ESD current paths demonstrates a 4.3-A transmission line pulse (TLP) failure level, corresponding to a $\sim$ 6.5-kV Human-Body-Mode (HBM) ESD protection level. Under a supply voltage of 1.2 V and a drain current of 6.5 mA, the proposed ESD-protected LNA demonstrates a noise figure of 2.57 dB with an associated power gain of 16.7 dB. The input third-order intercept point (IIP3) is -11 dBm, the input and output return losses are greater than 15.9 and 20 dB, respectively.**

***Index Terms*—CMOS, electrostatic discharge (ESD), low-noise amplifier (LNA), radio frequency (RF), silicon-controlled rectifier (SCR), transmission-line pulse (TLP).**

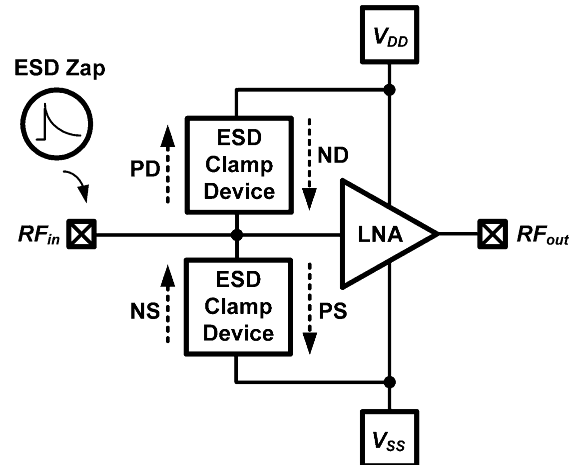

Fig. 1. General RF LNA configuration with ESD protection networks showing four ESD testing modes: PD, ND, NS, and PS.

I. INTRODUCTION

ELECTROSTATIC discharge (ESD) is one of the most critical reliability issues as the feature size in CMOS technology shrinks rapidly [1]–[5]. The gate-oxide thickness reduces down to the range of 1–2 nm in the 90-nm node and beyond, making the ESD protection a real challenge in integrated circuit (IC) design [6]. A good ESD design should provide sufficient immunity to the ESD stress, but not affect the signal under normal operation conditions. However, it is inevitable that the ESD protection devices introduce additional parasitic capacitances and resistances to the signal path, especially when a high ESD robustness is required. This could affect the RF front-end circuits and degrade RF performance [7]–[9]. For RF receivers, the low-noise amplifier (LNA) is the first stage, and it is often exposed to the risk of electrostatic charge directly. Fig. 1 shows a general configuration of an RF LNA together with ESD protection networks. The figure also illustrates the four ESD testing modes under different pin combinations, including positive ESD pulse with $V_{\rm DD}$ grounded (PD), positive ESD pulse with $V_{\rm SS}$ grounded (PS), negative ESD pulse with $V_{\rm DD}$ grounded (ND), and negative ESD pulse with $V_{\rm SS}$ grounded (NS) modes [3].

The double-diode scheme often employed for RF ESD protection has a simple configuration with low parasitic capacitance [10], [11]. The diodes together with a power clamp connected between $V_{\rm DD}$ and ground can provide a complete ESD protection network. However, this ESD network suffers from a large IR voltage drop between the input pad and the power clamp for the PS and ND modes due to an extra voltage drop across the supply path during ESD zapping. Consequently, the thin gate oxide is exposed under a high clamping voltage and may cause ESD damages. To improve the ESD protection robustness, it is highly desirable to have the direct discharge paths to ground to minimize the parasitic resistances in the ESD current path [12], [13].

The silicon-controlled rectifier (SCR) with high current capability is also widely used as the ESD protection block [14]–[18], which provides a direct discharge path for the PS mode. However, the high switching voltage and the transient-induced latch-up issues need to be overcome, especially for the nanometer CMOS technology [15]. Previously published results proposed various approaches to improve these problems [16], [17]. A substrate-triggered SCR can be quickly turned on when a current is applied [16]; for a gate-grounded nMOS (GGNMOS) triggered SCR, the nMOS transistor is used as an external trigger device to quickly trigger the SCR [17]. In these studies, the ESD current still needs to propagate through long paths in the PD, ND, and NS modes, and the parasitic resistance

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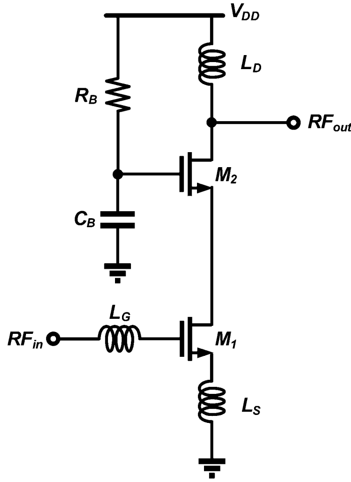

Fig. 2. Core circuit of the proposed ESD-protected LNAs.

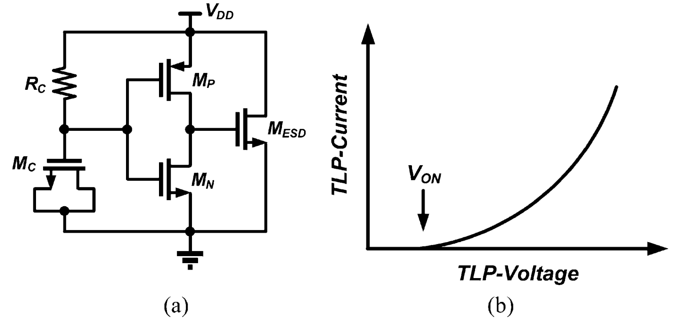

Fig. 3. (a) Circuit topology of the gate-driven power clamp. (b) High current I–V curve of the power clamp.

of the ground buses causes a large IR voltage drop leading to the thin gate oxide exposed under high stress. It is also highly desirable to have the ESD design with direct discharge paths to minimize the parasitic effects. Similar to the double-diode configuration, a power clamp is usually used here to provide the complete ESD paths of different ESD pin combinations during ESD testing.

In this study, ESD-protected LNAs at 5.8 GHz are realized in 65-nm CMOS. The idea of multipath ESD design including direct/indirect paths is emphasized and analyzed, and three different ESD topologies are designed and compared. The LNA using the proposed modified-SCR combined with double-diode provides multipath ESD protection with direct ESD discharge paths and achieves Human-Body-Mode (HBM) ESD levels up to ~6.5 kV for all of the four testing modes. This paper is organized as follows. Section II discusses the core LNA configuration and the power clamp. Both blocks are used in all three designs. In Section III, details of the ESD protection circuits in the three LNAs are presented. The experimental results including both RF and ESD measurements are shown in Section IV, and Section V concludes this work.

II. General Design Considerations

A. LNA Configuration

Fig. 2 shows the core circuit of the LNAs (without ESD), which is a cascode configuration with the inductive degeneration applied in the common-source stage. The cascode design cannot only improve the reverse isolation but also eliminate the Miller effect. The input impedance of the LNA is matched to 50 Ω by selecting the source-degeneration inductor L_S with the chosen transconductance g_m of M_1 and the corresponding gate–source capacitance C_{GS}. The gate inductor L_G is used to resonate out C_{GS} and set the imaginary part of Z_{opt} (the source impedance for optimum noise figure) to zero at the center frequency. It is also necessary to choose the dimension of M_1 such that the real part of Z_{opt} is equal to the source impedance of 50 Ω for simultaneous noise and power matching [19], [20]. The inductor L_D functions as the inductive peaking and also the output matching to 50 Ω. The gate of common-gate transistor M_2 is connected to V_{DD} through R_B to provide dc gate potential. The shunt capacitor C_B is used to provide a good ac ground for the common-gate stage.

The parasitic capacitances of the ESD blocks are considered in the matching network using the co-design approach. The ESD blocks are viewed as a part of the input matching to be optimized simultaneously. In practical design, the size of M_1, and the value of g_m are determined first with the considerations of power dissipation, gain, and noise. The ESD blocks are then selected based on the estimated protection levels and parasitic capacitances. The shunt parasitic capacitances introduced by the ESD blocks are co-designed with L_G and L_S to achieve simultaneous noise and power matching. If the obtained noise and/or gain are not satisfied, the design procedure is repeated by selecting M_1 and/or the ESD components with different sizes. By using the co-design approach, the parasitic capacitances of the ESD blocks provide additional design freedom of the matching network and relax the tradeoff between the ESD level and circuit performance.

B. Gate-Driven Power Clamp

In this study, the same power clamp is employed in all three ESD designs to complete the ESD paths and for a fair comparison. The power clamp provides a low-impedance path from the power supply to ground during an ESD zap. Different designs of the ESD power clamp were reported, such as the gate-grounded nMOS (GGNMOS) and diode string [18], [21] for various applications. The GGNMOS has the disadvantage of a large trigger voltage, and the diode string has the drawback of a large substrate leakage. The gate-driven power clamp employed here has a low turn-on voltage, high turn-on speed, and relatively small leakage current, which is suitable for ESD design in advanced technology nodes with a small gate-oxide breakdown [21]. Fig. 3(a) shows the circuit configuration of a gate-driven power clamp. The MOS capacitor M_C and P-type poly resistor R_C produce an *RC* time delay to ensure M_{ESD} functions correctly during an ESD event. The transistor M_{ESD} with a multi-finger topology has a total gate width up to ~2000 μm to sustain a high ESD current level. The large size of M_{ESD} with a low on-resistance also allows the power clamp to consume less voltage budget under a certain current level and thus relaxes the ESD design requirement for other ESD elements. The parasitic resistances and capacitances introduced by the power clamp are

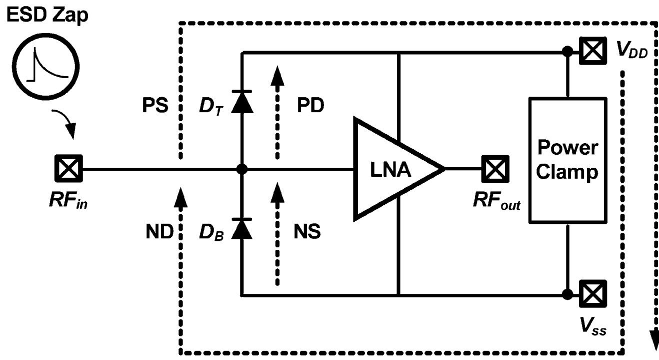

Fig. 4. ESD-protected LNA consists of double-diode and power clamp.

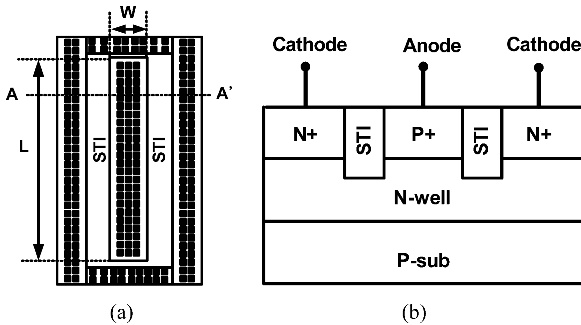

Fig. 5. (a) Layout view of the STI diode (the dots indicate a large number of vias and contacts). (b) Cross section of the P + /N-well STI diode D_T.

not that critical for the RF characteristics since this block is connected between the power rails only. Fig. 3(b) illustrates the typical high-current I–V curve of the gate-driven power clamp. In this design, the power clamp has a small turn-on voltage of ~0.7 V and can be quickly switched on by the *RC* trigger circuit.

III. Design of ESD Protection Networks

A. Double-Diode ESD Topology

Fig. 4 illustrates the LNA using the double-diode (D_T and D_B) ESD protection configuration. The figure also indicates the discharge paths for the four different ESD testing modes. It can be seen that the direct ESD paths are not available for the PS and ND modes. Fig. 5 shows the layout and cross section of the P + /N-well shallow-trench-isolation (STI) diode used for the top diode D_T. The anode (P+) of the STI diode connected to the RF input port $(\mathrm{RF_{in}})$ is surrounded by the STI, and the cathode (N+), enclosing the STI and P+, is connected to V_{DD}. The bottom diode D_B has a similar structure but with N+/P-sub, and the N+ and P+ nodes are connected to $\mathrm{RF_{in}}$ and V_{SS}, respectively. This configuration has the advantage regarding the parasitic capacitance variation versus the input pad dc voltage. For example, as the pad bias increases, the junction capacitance of D_B decreases due to the increased reverse bias, which could be compensated by the increased capacitance of D_T to maintain an overall small parasitic capacitance variation [11].

A single-finger layout with a large length/width ratio ($L=$ 30 μm and $W=0.8$ μm) is employed to maximize the overall perimeter of the diode. Under a fixed chip area, as the total perimeter increases, the current handling capability is enhanced by reduced parasitic resistances. The parasitic and electromigration (EM) effects introduced from the metal lines, contacts, and vias are also critical to the on-resistance and failure current of the ESD diodes. In practical design, the number of contacts and vias are both maximized (~300 each) under the design rule to achieve a small on-resistance and sustain an ESD current level up to several amperes. In addition, a large total width of ~30 μm for the metal lines of each ESD path is used to increase the current handling capability. The single-finger STI diode consumes a chip area of 129 $\mu\mathrm{m}^2$ (intrinsic area of 24 $\mu\mathrm{m}^2$) with an associated parasitic capacitance of ~40 fF. The diode size is chosen to achieve the desired ESD level. As mentioned earlier, the ESD block is co-designed with the matching network to reduce its impact on circuit performance. With a larger ESD diode, the ESD level could be further increased but with slightly degraded noise figure (NF) and gain.

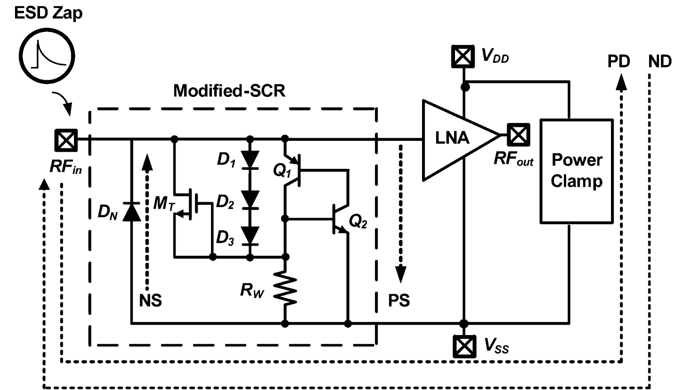

Fig. 6. ESD-protected LNA consists of modified-SCR and power clamp.

B. Modified-SCR ESD Topology

The SCR-based topology is another candidate for RF ESD protection design with the advantages of small on-resistance and large current capability per unit area [1]. Fig. 6 shows the ESD-protected LNA using the proposed modified-SCR, which consists of an embedded PNPN structure, a trigger diode chain (D_1, D_2, and D_3), a trigger nMOS M_T, a bottom diode D_N, and an embedded parasitic resistance R_W. The figure also indicates that the modified-SCR and power clamp both provide bi-directional ESD bypass paths, forming the complete ESD paths for the four testing modes. Note D_N here is used as the direct ESD path for the NS mode.

The basic SCR is a PNPN structure with a parasitic resistance, R_W, embedded in CMOS [13]. During an ESD event, the collector-base junction of Q_2 goes into avalanche breakdown generating electron current, which forward biases the emitter-base junction of the Q_1. The SCR will latch and provide a low impedance path to bypass the ESD current to ground. The major drawback of the conventional SCR is the high trigger voltage. In this design, the trigger voltage was reduced by adding two current paths of the diode chain (D_1, D_2, and D_3) together with the trigger nMOS (M_T). The current injecting into the base of Q_2 is greatly increased leading to fast trigger on of SCR. The number of trigger diodes n is a critical design parameter. The

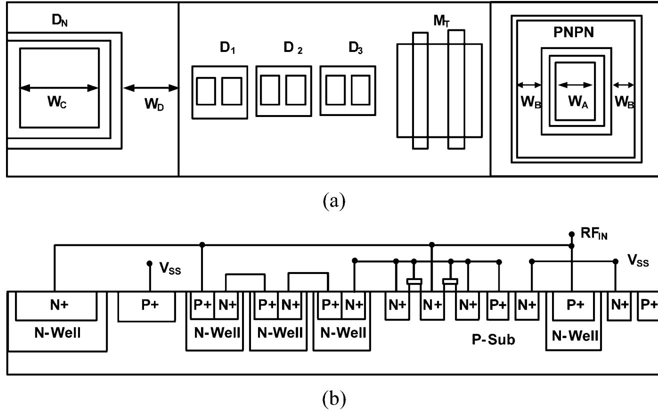

Fig. 7. (a) Layout view of the modified-SCR. (b) Corresponding cross section of the structure.

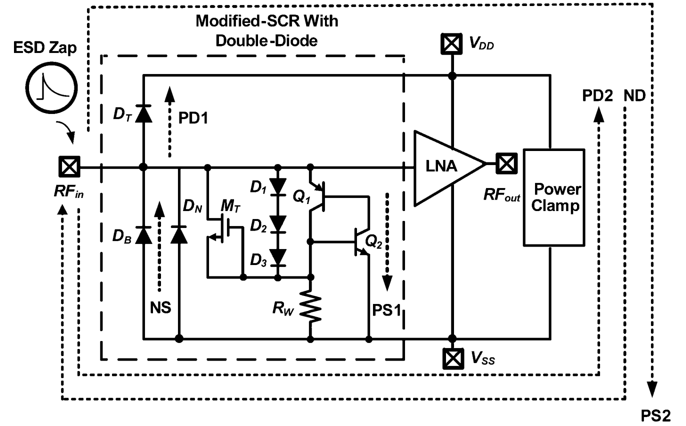

Fig. 8. LNA with the proposed multipath ESD protection network consisting of modified-SCR, double-diode, and power clamp.

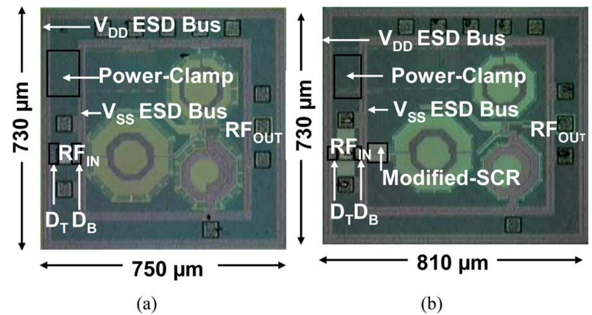

Fig. 9. Chip micrographs of LNAs with: (a) double-diode ESD protection (ESD-LNA_A) and (b) the modified-SCR with double-diode (ESD-LNA_C).

increased n reduces the voltage across each diode leading to reduced leakage current. On the contrary, a low V_T associated with a smaller n can speed up the turn on of ESD [15].

Fig. 7(a) and (b) shows the detailed layout of the proposed modified-SCR and the corresponding cross section, respectively. The PNPN structure is formed by the $P+$/N-well/P-sub region together with the N+ contacts connecting to V_{ss}, as shown on the right-hand side of the figure, which should have a sufficiently large area to sustain a large ESD current. However, a large area also introduces considerable parasitic capacitive loading and degrades circuit RF performance. In this design, the sizes of W_A and W_B are 7.6 and 1.4 μm respectively. The parasitic resistance of the P-substrate is described by R_W, as indicated in Fig. 6. The diode string D_1, D_2, and D_3 is constructed by the P+/N-well region with the N+ contact for the cathode. Since these diodes are only for the SCR trigger, without the need to sustain a large current, a relatively small size ($L = 0.4$ μm and $W = 1.4$ μm of each) of the diodes is used. The trigger nMOS M_T designed with two fingers ($L = 0.15$ μm and $W = 8$ μm of each finger) is employed to further improve the trigger capability. Although not shown in the figure, two diode chains are placed symmetrically around the PNPN region and four trigger transistors M_T are arranged surrounding the PNPN square to improve the uniformity of the ESD current distribution. In addition, the areas of the P-sub/N-well (D_N), defined by W_C and W_D, should also be sufficiently large to handle a large ESD current; the size of W_C is 7.6 μm and W_D is 1.4 μm. Note the design of the metal width ($\sim$30 μm), and the number of vias and contacts ($\sim$300 each) is similar to that in the double-diode configuration for EM and parasitic resistances considerations. The ESD design using a modified-SCR increases the parasitic capacitance by about 75 fF at the RF input.

C. Modified-SCR With Double-Diode ESD Topology

Fig. 8 shows the circuit topology of the proposed ESD-protected LNA with multipath ESD protection, including the direct paths for the PS, PD, and NS modes and the auxiliary paths for the PS and PD modes. This ESD topology can be viewed as the core of the modified-SCR together with a double-diode configuration; it can also be seen as an extra P+/N-well D_T with the modified-SCR since the parallel connected D_B and D_N can be equivalent to one diode. Compared with the double-diode topology, this design provides an extra direct ESD path of the PS mode; compared with the conventional SCR topology, this design provides extra direct paths of both the PD and NS modes. As shown in Fig. 8, there are two ESD current paths for the PS mode, PS1 and PS2, including a direct path PS1 through the modified-SCR and an auxiliary path PS2 through D_T followed by the power clamp. Similarly, there are also two ESD current paths, PD1 and PD2, for the PD mode. With the proposed multipath ESD network design, both of the PS and PD modes find the direct and auxiliary paths to the ground resulting in excellent ESD protection capability. This point can be verified from the measurement results. The topology of modified-SCR with double-diode increases the parasitic capacitance by about 150 fF at the RF input.

IV. Results and Discussion

The ESD-protected LNAs were fabricated using a 65-nm CMOS low-power process with one poly and six metal layers (1P6M), provided by Taiwan Semiconductor Manufacturing Company (TSMC). This process features a gate-oxide thickness of $\sim$2 nm and a minimum channel length of 60 nm for the core devices with a top metal thickness of 3.4 μm. The typical nMOS transistor presents f_T and $f_{\rm MAX}$ of $\sim$90 and 130 GHz, respectively [22]. The proposed ESD-protected LNA using three different topologies (double-diode, modified-SCR, and modified-SCR with double-diode denoted as ESD-LNA_A,

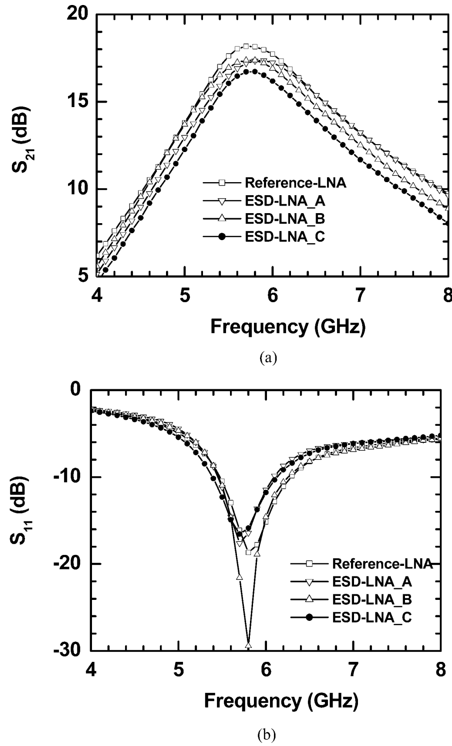

Fig. 10. (a) Measured S_{21} and (b) measured S_{11} of LNAs with/without ESD protection circuits.

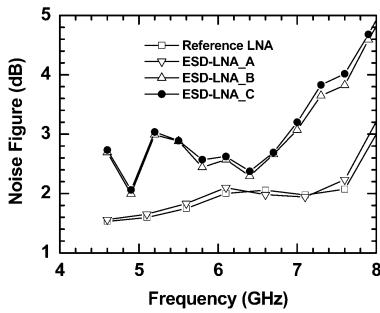

Fig. 11. Measured noise figures of different LNAs with/without ESD protection circuits.

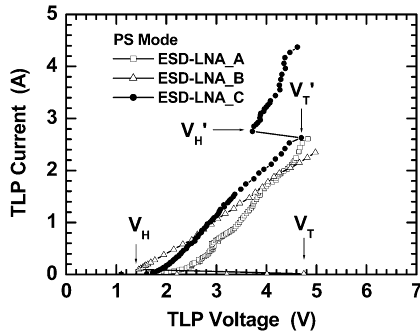

Fig. 12. Measured TLP current–voltage (I–V) characteristics of different ESD protection schemes in the PS mode.

ESD-LNA_B, and ESD-LNA_C, respectively), along with the power clamp were realized in the 65-nm CMOS process. Fig. 9(a) and (b) shows the chip micrographs of ESD-LNA_A and ESD-LNA_C with chip sizes of 0.55 and 0.59 mm^2, respectively. Note the ESD-LNA_B with the modified-SCR also has a chip size of 0.59 mm^2.

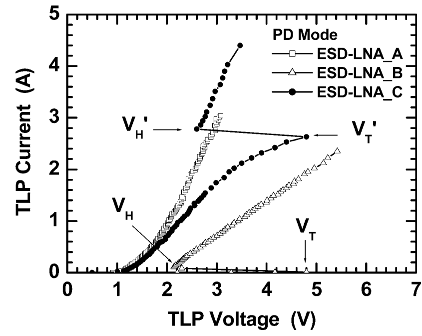

Fig. 13. Measured TLP current–voltage (I–V) characteristics of different ESD protection schemes in the PD mode.

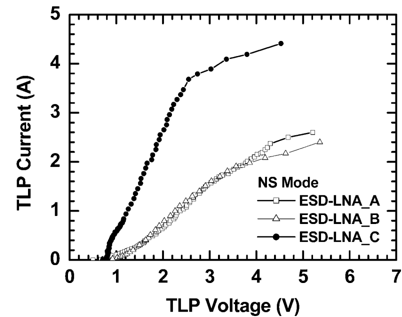

Fig. 14. Measured TLP current–voltage (I–V) characteristics of different ESD protection schemes in the NS mode.

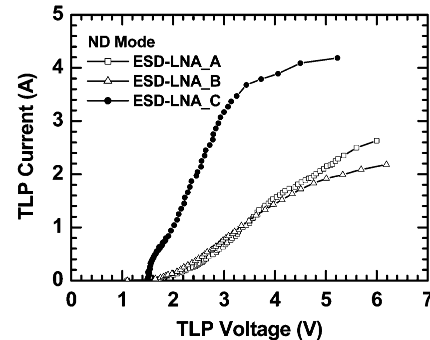

Fig. 15. Measured TLP current–voltage (I–V) characteristics of different ESD protection schemes in the ND mode.

TABLE I
ESD PERFORMANCE COMPARISON OF DIFFERENT ESD PROTECTION NETWORKS

ESD-Protected LNA	PS		PD		NS		ND	
	It_2 [A]	HBM [kV]	It_2 [A]	HBM [kV]	It_2 [A]	HBM [kV]	It_2 [A]	HBM [kV]
ESD-LNA_A	2.6	~ 3.9	3.0	~ 4.5	2.6	~ 3.9	2.6	~ 3.9
ESD-LNA_B	2.4	~ 3.6	2.4	~ 3.6	2.4	~ 3.6	2.2	~ 3.3
ESD-LNA_C	4.3	~ 6.5	4.4	~ 6.6	4.4	~ 6.6	4.3	~ 6.5

* HBM levels are estimated based on the TLP measurements.

A. RF Measurements

The RF characteristics were measured on-wafer using Cascade G-S-G microwave probes with a 100-μm pitch. The S-pa-

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED ESD-PROTECTED RF LNAS WITH PRIOR ARTS

Ref.	Unit	This Work				[8]		[25]		[26]				[27]	[28]	
Tech.	nm	65				90		90		90				130	150	
Freq.	GHz	5.8				5.5		2.4		5.5				5.5	2.4	2.46
		Ref-LNA	ESD-LNA_A	ESD-LNA_B	ESD-LNA_C											
NF	dB	1.85	1.93	2.44	2.57	2.7	2.9	2.56	3.2	3.4	3.2	3	3.5	2.5	2.77	2.36
Power	mW	7.8	7.8	7.8	7.8	9.72	9.72	12.9	12.9	9	9	9	9	6.6	4.65	4.65
S_{21}	dB	18.1	17.3	17.4	16.7	12.3	13.3	22.1	21.9	12	12.6	13	16.2	12.4	12.1	14
S_{11}	dB	-18.7	-16.4	-29.4	-15.9	-10.3	-14.4	-12.6	-10.9	-24	-18	-18	-11.5	<-10	-19	-18.5
IIP3	dBm	-10	-11	-11	-11	-3	-3	-10.8	-11	0.4	-0.5	-0.4	-5	-9	2.4	-2.2
HBM	kV	--	~ 3.9	~ 3.3	~ 6.5	--	2	--	4	5.5	2.5	0.5	1.9	5	2	--

rameters and noise measurements were performed by the Agilent E8361A PNA network analyzer and the Agilent N8975A noise figure analyzer, respectively. The short-open-load-thru (SOLT) calibration and loss compensation have been done before the measurements. The LNAs operate from a 1.2-V supply and draw a current of 6.5 mA. The measured S_{21} and S_{11} of the LNAs are shown in Fig. 10(a) and (b), respectively. With the well-designed ESD circuits, the peak power-gain frequencies are all at 5.8 GHz, and the frequency responses are almost identical. The input return loss is greater than 15 dB for all cases. The power gains at 5.8 GHz are 17.3, 17.4, and 16.7 dB for the three cases, respectively, which reduce by 0.8, 0.7, and 1.4 dB, compared with the reference LNA of 18.1 dB. Fig. 11 shows the measured NF of 1.93, 2.44, and 2.57 dB at 5.8 GHz, and the NF of the reference design is 1.85 dB. For the LNAs with the SCR device (ESD-LNA_B and ESD-LNA_C), the matching networks are adjusted accordingly using the co-design approach, and the expected noise figure should be only slightly higher (~0.2–0.3 dB based on simulation) than that of the ESD-LNA_A. The measured results showed more pronounced degradation of noise figure, which could be attributed to the inaccurate SCR circuit model used for simulation. A two-tone test using 5.8025 and 5.7975 GHz is performed to measure the input third-order intercept point (IIP3). The measured IIP3 of ESD-protected and reference LNAs are -11 and -10 dBm, respectively.

B. ESD Testing Results

The transmission-line pulse (TLP) measurement technique is widely used to provide precise, high-voltage, and high-current waveforms for ESD characterization [23]. The ESD testing was performed on-wafer by dc probes using a Barth 4002 TLP test system. The pulse of a 10-ns rise time with a 100-ns pulsewidth was used to simulate the HBM ESD condition. The relation between the TLP second breakdown current (It_2) and the HBM ESD level $(V_{\rm HBM})$ can be approximated as $V_{\rm HBM}$ (V) $\sim It_2$ (A) * $R_{\rm HBM}(\Omega)$, where $R_{\rm HBM}(= 1.5\ {\rm k}\Omega)$ is the equivalent resistance of human body resistance [24]. For example, a TLP current level of 1.3 A corresponds to a ~2-kV HBM ESD level.

Fig. 12 shows the TLP test results of different ESD-protected LNAs in the PS mode. The results of ESD-LNA_A presents a linear characteristic, indicating that the ESD bypass current enters from the RF input pad, flows through D_T to $V_{\rm DD}$, and then reaches $V_{\rm SS}$ via the power clamp (without a direct ESD bypass path). A sudden increase of the leakage current suggests that a second breakdown current It_2 up to 2.6 A can be achieved corresponding to an HBM ESD level of ~3.9 kV. The pure snapback turn-on behavior of ESD-LNA_B indicates the ESD bypass current travels from the RF input pad to $V_{\rm SS}$ directly, and the trigger voltage (V_T) is about 4.7 V, which is lower than the gate-oxide breakdown voltage of about 7 V (measured from the TLP tester with a stress time of 100 ns). An It_2 up to 2.4 A corresponds to an HBM ESD level of ~3.6 kV. The figure also shows that the snapback holding voltage (V_H) is about 1.47 V, which is higher than $V_{\rm DD}$ (1.2 V) to avoid latch-up during normal RF operation. The I–V characteristic of ESD-LNA_C suggests that D_T turns on first in the linear mode, followed by the trigger of the modified-SCR together with the power clamp in the snapback mode also at a V_T' of about 4.7 V. Consequently, a snapback characteristic appears at V_H' about 3.72 V, and then an It_2 of 4.3 A can be achieved, corresponding to an HBM ESD level of ~6.5 kV. Compared with ESD-LNA_A (or ESD-LNA_B) with a single ESD path in the PS mode, ESD-LNA_C with multiple ESD paths can enhance the corresponding HBM ESD level from ~3.9 kV (or ~3.6 kV) to ~6.5 kV.

Fig. 13 shows the TLP test results of the PD mode. Similarly, the linear behavior of ESD-LNA_A indicates that the ESD current goes through D_T to $V_{\rm DD}$ directly, and an It_2 up to 3.0 A is obtained, corresponding to a HBM ESD level of ~4.5 kV. For ESD-LNA_B, the snapback turn-on behavior with a trigger voltage V_T of 5 V and a holding voltage V_H of 2.1 V, and an It_2 up to 2.4 A can be achieved, corresponding to a HBM ESD level of ~3.6 kV. The design of ESD-LNA_C presents a linear mode turn-on behavior first, followed by the trigger of a modified-SCR together with the power clamp in the snapback mode at a V_T' of about 4.8 V. A snapback characteristic appears at V_H' about 2.6 V, and an It_2 of 4.4 A is achieved, corresponding to a HBM ESD level of ~6.6 kV. The clearly enhanced HBM ESD level can be attributed to the multiple ESD paths of both PD1 and PD2.

Fig. 14 shows the TLP results of the NS mode. For ESD-LNA_A, an It_2 of 2.6 A is obtained, corresponding to an HBM ESD level of ~3.9 kV. The almost identical TLP

curves for ESD-LNA_A and ESD-LNA_B indicates that the on-resistance and current bypass capability of D_B and D_N are similar. For ESD-LNA_C, the on-resistance is reduced by about half due to the parallel connected D_B and D_N, and the HBM ESD level is increased up to $\sim$6.6 kV.

Fig. 15 shows the TLP test results of the ND mode. The curves have similar characteristics with the NS mode, but the curves shift toward higher voltage under the same current level due to an extra voltage drop of the power clamp in the ND mode. It should be mentioned that the TLP test with only the power clamp indicates a $>$8-kV HBM ESD failure level, suggesting the diodes are the limiting factors of the ESD performance. With the same bottleneck of the diodes, both the ND and NS modes have a $\sim$6.5-kV HBM ESD level. However, the increased voltage drop in the ND mode due to the power clamp induces a higher stress on the gate oxide. In contrast, the stress is smaller in the NS mode owing to the direct ESD path, which is still of advantage in terms of ESD design considerations.

Table I summarizes the HBM ESD results of the three LNAs for the four testing modes. Table II compares this work with other published ESD-protected RF LNAs. The proposed ESD-protected LNA achieves a highest HBM ESD level with a comparable NF by the 65-nm CMOS technology with the thinnest gate oxide. The ESD protection only increases the noise figure from 1.85 to 2.57 dB in our design.

V. Conclusion

In this paper, we studied the ESD-protected RF LNAs in 65-nm CMOS technology with three different ESD designs. The proposed multi-ESD-path LNA using the modified SCR in conjunction with double-diode and a gate-driven power clamp presented TLP currents greater than 4.3 A, corresponding to HBM ESD levels to $\sim$6.5 kV for all four testing modes. This design provided direct ESD discharge paths to both $V_{\rm DD}$ and $V_{\rm SS}$ and auxiliary ESD paths for the PS and PD modes. Under a supply voltage of 1.2 V and a drain current of 6.5 mA, the LNA presented a NF of 2.57 dB with an associated power gain of 16.7 dB at 5.8 GHz.

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