Wideband Conducted Electromagnetic Emission Measurements Using IPD Chip Probes

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***Abstract*— A novel on-chip measurement technique for characterizing conducted electromagnetic emission of integrated circuits in the gigahertz frequency range is proposed. The International Electrotechnical Commission (IEC) direct coupling method is reviewed, and the considerations on improving the applicable bandwidth of the testing probes are discussed. Design of the most critical resistive components for the probes is elaborated to achieve the required accuracy and bandwidth. With the compact chip probes realized by the integrated passive device (IPD) technology, the measurement bandwidth can be significantly extended compared with the conventionally used surface mounted device resistors. The probes are verified to comply with the IEC 61967-4 standard, and an excellent bandwidth up to 15 GHz can be achieved. By connecting the flipped die under test with the probes embedded in IPD substrate (core sizes of the 1-Ω current probe and 150-Ω voltage probe are 0.55 mm × 0.77 mm and 0.83 mm × 1.49 mm, respectively), the conducted emission measurement of a 58-MHz oscillator integrated circuit is demonstrated up to 3 GHz.**

***Index Terms*— 1-/150-Ω probe, conducted electromagnetic (EM) emission, EM compatibility (EMC), integrated passive device (IPD), on-chip measurements.**

I. Introduction

ELECTROMAGNETIC compatibility (EMC) becomes an increasingly important issue for integrated circuits (ICs) owing to the rapid scaling of transistor feature size with a high integration level. The advanced technology allows ICs to achieve high-speed performance under low power dissipation. However, the circuits also generate more noise and become more vulnerable to interference. As a result, understanding and characterizing the behaviors of electromagnetic (EM) emission and immunity of ICs, especially at increased operating frequencies, become a crucial topic for system integration.

A set of IC level test methods on EM interference [International Electrotechnical Commission (IEC) 61967] [1] and EM susceptibility (IEC 62132) [2] was released by the technology subcommittee 47A of IEC to investigate EMC problems. Depending on the transfer types of EM wave, the test methods can be classified into radiated or conducted ones. Investigation of the EM emission issue mainly relies on the measurements owing to the complexity of analytical equations and modeling. The radiated emission measurements typically used include the transverse EM (TEM) cell method [3]–[5] and the surface scan method [6], [7]. With the advantage of contactless nature, the TEM cell utilizes the shielded enclosure to receive the coupled signal from a device under test (DUT). On the other hand, the surface scan method relies on the electric (E)/magnetic (H) probes to evaluate the near-field E/H components at the surface of the DUT. Compared with the radiated measurement approach, the conducted method allows the physical link between probes and the DUT to guarantee the results with better repeatability and correlation [8], [9].

The ICEM model [10] is considered to be relatively accurate for describing the EMC behavior of ICs. Built from both simulated and measured results, the ICEM is composed of two main macromodels including the internal activity (IA) and power distribution network (PDN). The IA is considered as the source of noise, whereas the PDN represents the transmission media. The PDN modeling techniques are quite mature nowadays, while modeling of IA remains challenging. In general, the IA modeling by transistor level simulation is not practical due to tedious data processing. The most commonly used solution for IA modeling is to convert the measured waveform back to an equivalent noise current source. This black box approach uses piecewise linear description to serve as the current generator in the simulator directly [11]. Some works also use the transfer function of testing facility with the known PDN to obtain an equivalent current source from the measured data in either frequency or time domain [12]. As can be seen, measurements play an essential role in the characterization and modeling of the EM emission behavior.

With the EM emission caused by the fast changes of currents/voltages in the ICs, the resulting interference in the radio frequency (RF) range could distribute via the on-chip passive PDN, interconnection of package (solder bump, bond wire, and IC pins), and the off-chip PDN (traces on PCB and cable harness). The EMC strategies [13]–[15] are essential to suppress the noise and ensure the reliability of the circuit and system operation. The measurements using the 1-Ω current probe and 150-Ω voltage probe are standardized as IEC 61967-4 [16], as known as the direct coupling method to investigate the conducted EM emission in the RF range. Using probes typically built by lumped components with PCB, the EM emission characteristics of ICs can be observed.

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The direct coupling method is concise and popular among various testing techniques of EM emission. Although accuracy concern of the 150-Ω method was reported with some comparative experiments [17], [18] in the early period, the issue has been improved and this method is widely used nowadays. In contrast, even with the details depicted in the standard, very few works were reported based on the measurement method with the 1-Ω current probe [19], [20]. The main challenge is to meet the specifications of the 1-Ω current probe in practice [21]. It should be emphasized that the specification of the 1-Ω current probe in most of the published papers was not verified, which may lead to a measurement error, especially at high frequencies.

Most released standards such as the IEC series have the frequency range below 1 GHz, which becomes insufficient to evaluate the EM emission behaviors for modern high-speed ICs operating in the gigahertz or even up to tens of gigahertz range. A model for predicting the conducted emission has been validated by means of measurement up to 3 GHz [22]. Based on the radiated emission measurement, the gigahertz TEM cell [23] method was proposed with a frequency range up to 18 GHz. Similarly, the measurement bandwidth of the direct RF power injection method [24] had been extended up to 18 GHz for evaluating IC immunity [25]. As a trend, the conducted EM emission measurement is also expected to have the capability of a much wider bandwidth with the new standards under development.

In this paper, an aggressive testing technique is demonstrated for the conducted EM emission at the bare die level based on the direct coupling method. The miniature chip probes realized by the integrated passive device (IPD) technology are employed for the test. By embedding the 1-/150-Ω network for the chip probes in IPD substrate with the flipped DUT connected, the intrinsic noise from the IC can be collected directly without the parasitic effects introduced by the package, PCB traces, and testing facilities. The measurement bandwidth can be expanded up to 15 GHz. This paper is organized as follows. Section II reviews the direct coupling method briefly with the principles emphasized. Also, the proposed on-chip testing method is described. Section III discusses the challenge of obtaining the chip probes with high precision resistance in microfabrication process. The IPD chip probes of both 1 and 150 Ω are verified to comply with the specification in Section IV. Also, the measured results of an oscillator IC prove that the proposed methodology can perform the conducted emission measurement with a bandwidth well above the IEC standard of 1 GHz for the need of modern and future high-speed ICs.

II. On-Chip Conducted EM Emission Measurements

A. IEC 61967-4 Direct Coupling Method

Fig. 1 illustrates the measurement setup using the direct coupling method with 1- and 150-Ω probes for the conducted EM emission of the IC. The1-Ω probe provides a low impedance path, which is inserted between the V_{SS} pin of the IC and the ground of PCB to measure the RF voltage across the 1-Ω resistance, resulting from all the RF currents return to

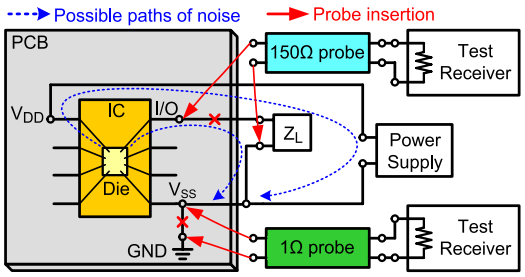


Fig. 1. Direct coupling method using 1- and 150-Ω probes to measure the conducted EM emission of IC.

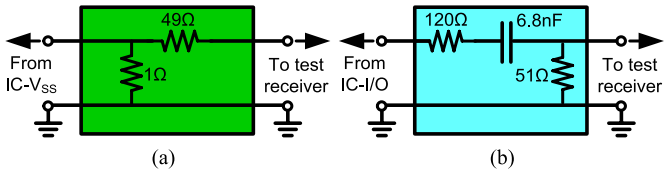


Fig. 2. Configuration of the conducted EM emission probes. (a) 1-Ω current probe. (b) 150-Ω voltage probe.

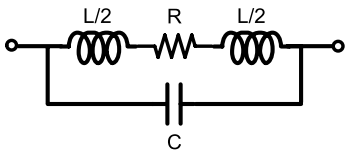


Fig. 3. Equivalent circuit model of an SMD resistor at high frequencies.

the IC. Note the return paths in ICs are mostly via the ground or the power plane, which makes the V_{SS} pin of IC suitable for measuring the RF return current. Details of the two-port 1-Ω probe are shown in Fig. 2(a), which is composed of 1 and 49-Ω resistors. The 49-Ω resistor is placed between V_{SS} and the test receiver to provide 50-Ω impedance matching. On the other hand, the 150-Ω probe is inserted between the I/O ports and test receiver as also shown in Fig. 1. The I/O port of the IC could be linked to a long path through the PCB trace, interconnects, cable harness, and the receiver. According to IEC 61000-4-6, these networks show a typical impedance of 150 Ω. Similarly, a matching network as shown in Fig. 2(b) is needed for impedance conversion for the 50-Ω test receiver. The series capacitor blocks dc current and couples the disturbance to the test receiver. A capacitor of 6.8 nF is chosen as the example in the standard, but is not limited to this value. The increased capacitance allows a lower 3-dB bandwidth of transmission.

B. Proposed On-Chip Testing Technique With Bandwidth Extension

Testing of a specific pin is typically performed with the packaged IC on a PCB for the methods currently available for EM emission measurements. The surface mounted device (SMD) is a good choice to realize the PCB level resistive probes with a relatively small size. The SMD resistor can be modeled as shown in Fig. 3 at high frequencies, where the inductance is formed by the finite length of the resistor and

contacting pads, and the capacitance results from the coupling of the pads and substrate. Although the leadless property of SMD reduces the unwanted parasitics compared with the axial leaded devices, the parasitic effects are still a serious issue for high-frequency applications, which makes the PCB level realization of probes difficult to be complied with the IEC specifications even for the IEC standard of only 1 GHz.

Another challenge to be overcome for the EM emission measurements is the undesired effect introduced from the IC package. The RF interference emitted from a packaged IC could be either distributed through the conducted path or radiated from the package itself. The uncertainty of noise origin could mislead the strategies for solving the EMI problem. Although the package could be considered as a part of the IC, various types of packages could exhibit different characteristics regarding noise propagation, which makes the modeling of EM emission of the intrinsic circuit a very difficult task. Also, the impact of parasitic effect introduced by packaging becomes more severe as the operating frequency increases. A better approach is to consider the EM emission behavior separately for the intrinsic IC and package to fully understand the root cause of noise and interference.

In this paper, a solution to the issues of both SMD resistor and IC package for the conducted EM emission measurement is proposed at high-frequency bands. Based on the IPD technology, high precision microfabricated chip probes with 1-/150-Ω network built therein are realized to measure the high-frequency EM emission from the IC by on-chip probing. Fig. 4(a) depicts the proposed solution, where the DUT is flip-chip connected on the carrier IPD substrate with the embedded 1-/150-Ω chip probes. The dc probe (GGB picoprobe) is used for dc power supply. The microwave probe (Cascade ACP-40) collects the emitted EM signal from DUT, and is connected to a spectrum analyzer (Agilent E4440A) as the test receiver via the high-frequency coaxial cable (Astrolab32027) and SMA adaptors, as shown in Fig. 4(b). Fig. 4(c) shows a photograph of the complete measurement setup. The proposed on-chip testing method features high reliability, high stability, and high confidence of the measured results with a significantly improved measurement bandwidth and a very compact size of probe.

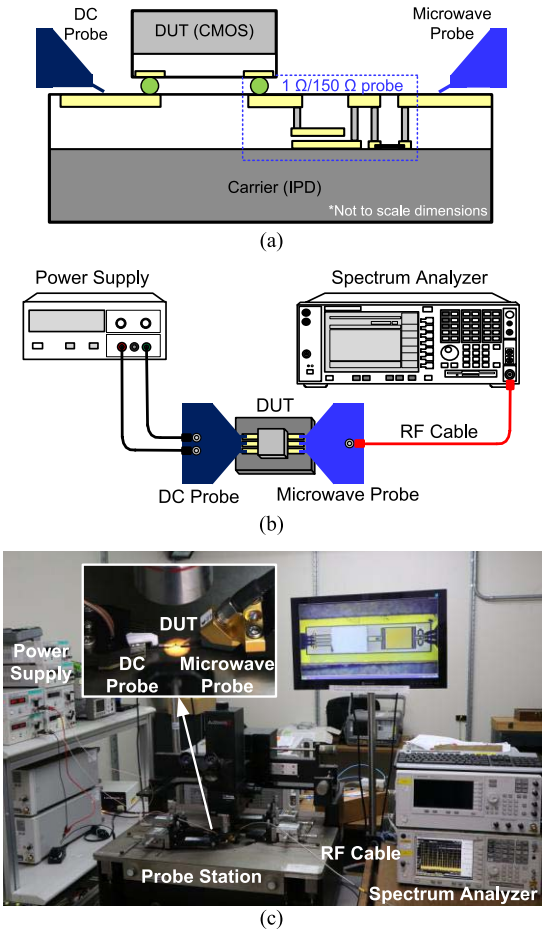


Fig. 4. Proposed wideband on-chip conducted EM emission measurement. (a) IPD chip probes embedded in the substrate with the flipped DUT. (b) Details of measurement setup. (c) Photograph of the complete measurement setup.

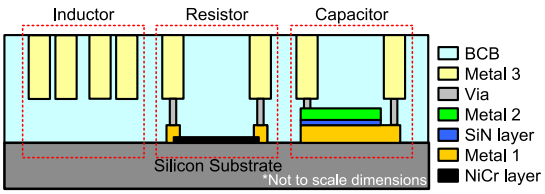


Fig. 5. Cross section of the IPD for RF applications.

III. Realization of Embedded Chip Probes on IPD

The IPD technology is used to realize the EM emission probe, which is a passive device only process developed mainly for RF applications. With the high-resistivity silicon substrate, passive components such as filter [26], [28], coupler [29], [30], phase shifter, and power divider [31]/combiner [32] can be realized using the IPD process for low cost and high volume production. This technology also allows integrating the passive only circuits with active devices/circuits for multichip module applications [33], [34]. The IPD technology adopted here has three metal layers with a low loss tangent dielectric material of benzocyclobutene (BCB), as shown in Fig. 5. The metallic Cu layers from the bottom to the top are denoted by Metal 1, Metal 2, and Metal 3 with the thicknesses of 1, 0.65, and 10 μm, respectively. The top metal layer (M3) is mainly for low-loss interconnects and high-Q inductors. Note that the thickness of the silicon substrate is 650 μm with a resistivity over 3 kΩ cm and that of the BCB layer on top ($\varepsilon_r = 2.65$ and $\tan\delta = 0.0008$–0.002) is 13 μm. A 0.05-μm NiCr layer is deposited for resistors. Also, a thin-film SiN dielectric interlayer ($\varepsilon_r = 6.7$ and $\tan\delta = 0.0002$) with a thickness of 0.2 μm is used to form metal-insulator-metal capacitors.

As the key component of the probe, the resistors used for the design could suffer from process variation, resulting in deviation from the desired value. Several layout techniques were proposed to minimize the process variation in IC design [35], such as size expansion, close placement, interdigitation, common centroid, and dummy devices. Some of the approaches may not be effective for RF design owing to

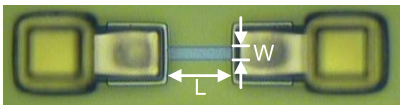


Fig. 6. Chip micrograph showing the layout of a 100-Ω IPD resistor ($W = 5$ μm and $L = 25$ μm).

TABLE I
MEASURED RESISTANCE WITH DIFFERENT EXPANSION RATIOS

Size Expansion	Resistance (Ω) @ 300k Hz		
	120	51	1
1× (W= 5 μm)	149.19	56.44	1.27
2×	127.63	52.91	1.12
4×	122.46	51.23	1.10
6×	120.64	51.05	1.08

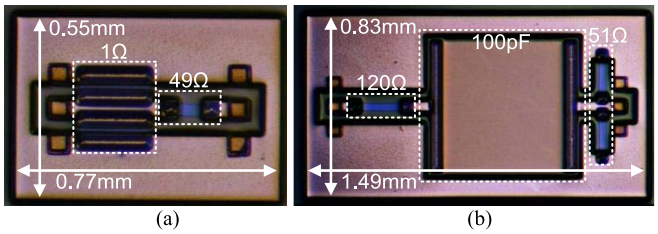


Fig. 7. Micrographs of the chip probes realized in IPD technology. (a) 1-Ω current probe. (b) 150-Ω voltage probe.

TABLE II
IEC SPECIFICATIONS OF THE 1-Ω CURRENT PROBE

Frequency range	DC - 1 GHz
Output impedance (Z_{out})	40 Ω - 60 Ω
Insertion loss in calibration circuit	34 dB ±2 dB
Decoupling	Larger than the limit line as shown in Fig. 11

TABLE III
IEC SPECIFICATIONS OF THE 150-Ω VOLTAGE PROBE

Frequency range	150 k - 1 GHz
Input impedance with 50 Ω termination (Z_{in})	145 Ω ± 20 Ω
Insertion loss within a 50 Ω system	0.2586 (11.75 dB±2 dB)
Voltage ratio (V_{out}/V_{in})	0.1738 (-15.2 dB±2 dB)

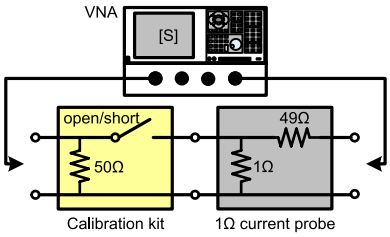


Fig. 8. Measurement configuration for sensitivity and decoupling characteristics by connecting the 1-Ω probe to the calibration kit.

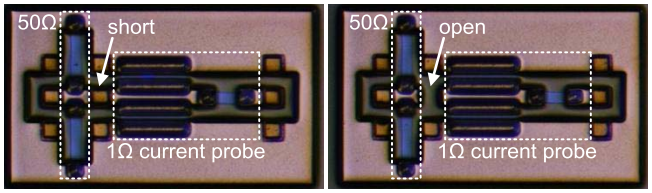
the parasitic effects, and therefore the size expansion technique is adopted in this design for achieving accurate resistance [36]. Fig. 6 shows the chip micrograph of a 100-Ω resistor, where the resistor has a nominal sheet resistance R_{sh} of 20 Ω/square with a minimum layout rule of 5 μm in the IPD process. The fabricated resistance suffers a process variation, which can be mainly attributed to the lift-off process of the deposited NiCr layer. Note that the process induces a width variation ΔW, whereas the length L can be well controlled by the via or interconnect formation. With the increased W (L scales up by the same factor to keep a constant R), the effect of ΔW to the overall width becomes relatively small, and a very precise resistance can be obtained. In this paper, several resistance values in different sizes for the chip probes are examined. Table I lists the measured results of some required resistances. A clear trend shows that the resistance approaches the desired value as the expansion ratio increases. It should be emphasized that although the size is increased for improved accuracy, the parasitic effect of chip resistor is still much smaller compared with that of the SMD resistor. Also, the resistances needed for our application are relatively small, and thus the chip dimension is not a problem.

The coplanar waveguide (CPW) of G-S-G type structure is utilized for the chip probes. The ground planes located at both sides of the signal path make the shunt connection relatively simple. This also shortens the return path compared with the microstrip type design that may contribute additional parasitic inductances from the through substrate via to the ground. Fig. 7(a) shows the chip photo for the current probe illustrated in Fig. 2(a), where the 1-Ω resistor is realized by two 2-Ω resistors connected in parallel to be consistent with the CPW configuration and also for a reduced size, and the 49-Ω resistor is connected in series. For the 150-Ω voltage probe as shown in Fig. 2(b), the 120-Ω resistor is connected in series to the 100-pF capacitor, and the shunt resistor of 51 Ω is realized by two 102-Ω resistors connected in parallel, as shown in Fig. 7(b). With the IPD technology, both microfabricated chip probes have extremely compact sizes of only 0.55 mm × 0.77 mm (1 Ω) and 0.83 mm × 1.49 mm (150 Ω), respectively.

IV. PROBE VERIFICATION AND EXPERIMENTAL RESULTS

A. Probe Verification by IEC Standard

The IEC standard specifies the characteristics of direct coupling method in detail with a measurement bandwidth of 1 GHz, as listed in Tables II and III for the 1- and 150-Ω probes, respectively. The most critical item for achieving reliable measurements using the 1-Ω probe is the insertion loss with the calibration kit connected. The detailed procedure and test setup are depicted as follows. First, the calibration kit, current probe, and test receiver are connected as illustrated in Fig. 8, where the test receiver is a vector network analyzer in our study. With the calibration kit switched to the short or open status, two measurements have to be performed. Note that the calibration kits are realized by two individual chips integrated with the current probe directly to minimize the undesired parasitic effects. The short status is built by



(a) (b)

Fig. 9. Implemented calibration kits with the 1-Ω current probe. (a) Short status. (b) Open status.

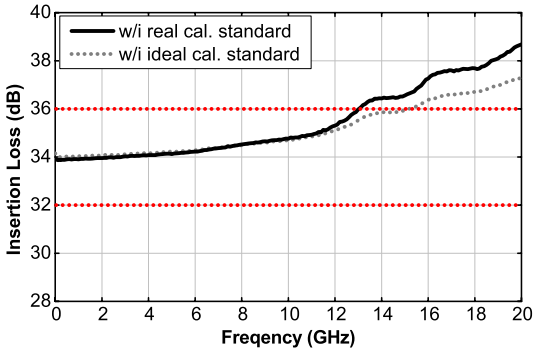


Fig. 10. Sensitivity of the 1-Ω probe with the calibration kit.

connecting the shunt 50-Ω resistor to the current probe directly as shown in Fig. 9(a). On the other hand, a gap between the 50-Ω resistor and the current probe is intentionally left for the open status as shown in Fig. 9(b). The measured insertion loss in the short status is referred to the sensitivity of the probe. A flat frequency response is desired over the test bandwidth, and the IEC specification of insertion loss requires ±2 dB from 34 dB, which is difficult to be obtained using the conventional SMD probe and PCB even with a 1-GHz bandwidth. As shown in Fig. 10, the IPD current probe achieves a significant bandwidth enhancement up to 13 GHz, which is much wider than the specification in the IEC standard. An interesting experiment was conducted to investigate the impact of the calibration kit design on the measurement. We measured the S-parameters of the current probe only first, which were then imported into the simulator. With a virtual calibration kit of an ideal 50 Ω connected, the gray dotted curve in Fig. 10 shows that the applicable bandwidth of sensitivity can be further expanded up to 15 GHz.

Another insertion loss measurement was also performed in the open status. By subtracting these data from the previously measured sensitivity, the difference is referred to as decoupling. The result represents the shielding capability of the probe, as shown in Fig. 11 with a limit curve (dotted line) versus frequency provided in the IEC standard. The last item to be checked is the output impedance of the probe as shown in Fig. 12, which should be near 50 Ω to ensure that the disturbance can be collected with small reflection. The measured result shows that Z_{out} complies well with the specification over the entire measured frequency range.

Table III lists the specification of 150-Ω voltage probe indirect coupling method. The series capacitor dominates the lower 3-dB bandwidth, and different capacitances are allowed in the standard. In this paper, the single maximum capacitor

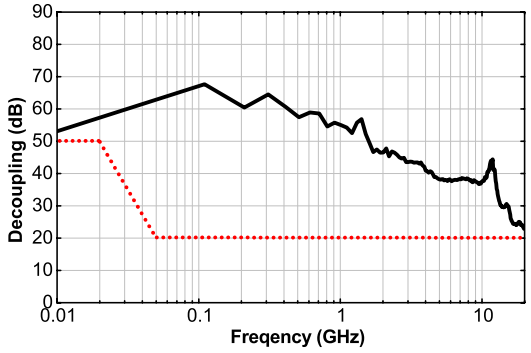


Fig. 11. Decoupling characteristics of the 1-Ω probe.

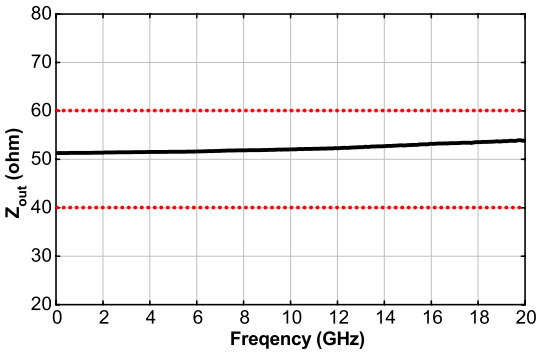


Fig. 12. Measured output impedance of the 1-Ω probe.

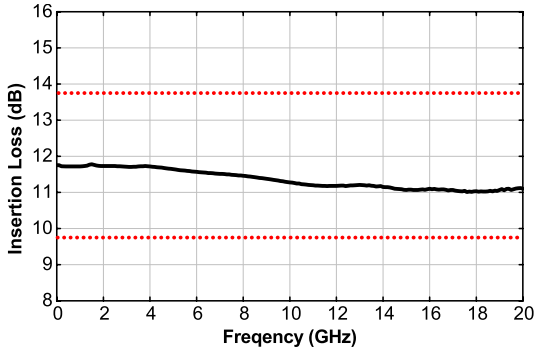


Fig. 13. Measured insertion loss of the 150-Ω probe.

of 100 pF in the IPD design rule is employed. The resulting corner frequency is at around 12 MHz, which is sufficiently low, and therefore will not affect the frequency response at high frequencies. Fig. 13 shows the measured insertion loss of the 150-Ω voltage probe. The result meets the specification of 11.75 ± 2 dB with a good flatness over the measured frequency range. Fig. 14 shows the measured input impedance of the 150-Ω probe that also complies with the specification listed in the standard.

B. Probe Verification by IC

The experimental results verify that both probes can meet the standard of IEC 61967-4 direct coupling method but with a much enhanced bandwidth. To further demonstrate the capability of the proposed probes for the conducted EM emission

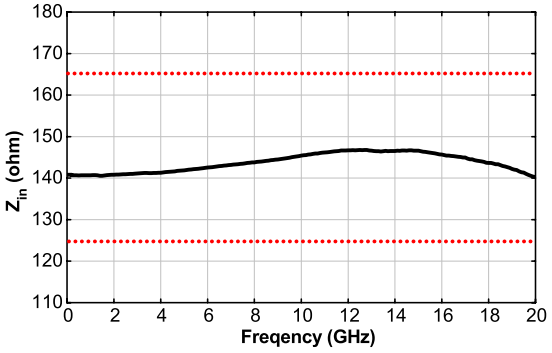
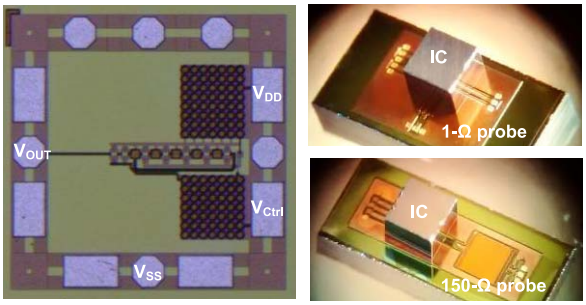


Fig. 14. Measured input impedance of the 150-Ω probe.



(a) (b)

Fig. 15. Micrographs of the implemented test structures. (a) DUT (ring VCO in CMOS) and (b) flipped DUT with the 1- and 150-Ω probes on the IPD substrate.

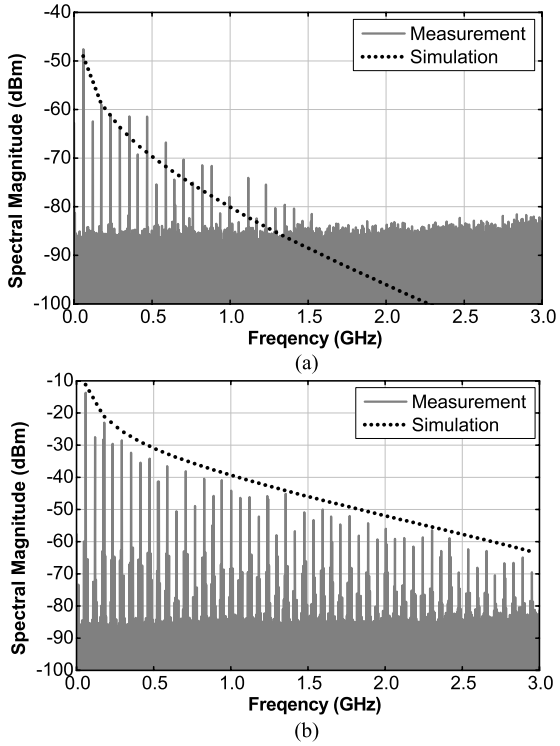


Fig. 16. Measured spectra of (a) V_{SS} pin of VCO using 1-Ω probe and (b) V_{OUT} port of VCO using 150-Ω probe.

for ICs, a ring voltage-controlled oscillator (VCO) implemented in the standard TSMC 1P6M 0.18-μm CMOS process is employed as the DUT, as shown in Fig. 15(a). Note that the unlabeled pads are dummy pads, which are used for additional bonding to support the flipped IC and to ensure the connection between IPD carrier and the IC. The VCO was operated under a supply voltage of 1.8 V with a power dissipation of 4.18 mW, which was then tuned to oscillate at 58 MHz for the following experiments. Note that the oscillator used here can emulate the noise generators in a large-scale IC. With the large ON–OFF swings, the oscillator acts like the latent aggressor that could affect the normal operation of either analog or digital circuits. Also, the reference clock in the range of several tens of megahertz is commonly used for different applications, and the harmonics could spread at the entire spectrum over 1 GHz.

With the test setup shown in Fig. 4, the VCO was flip-chip bonded on the IPD carrier with the 1- and 150-Ω probes embedded in the substrate, respectively, as shown in Fig. 15(b). The 1-Ω probe is connected to the V_{SS} pin of VCO to measure the disturbance of EM emission, and the150-Ω probe is connected to the output port V_{OUT} of the oscillator. The material of the interconnection between the flipped DUT and IPD probes is gold with negligible effect on the probes at the frequencies of interest [37]. As shown in Fig. 16(a) and (b), the measured spectra up to 3 GHz in both cases show good agreements with the simulated results. Compared with Fig. 16(b), the relatively larger discrepancy between the measured and simulated results of Fig. 16(a) can be attributed to the much lower power level of the signal, which definitely introduces more uncertainty to the measurements. An average uncertainty of 3-5 dB is observed during measurements for high-order harmonics with the power level below −60 dBm, and the worst case could be up to 8-dB variation. Also, the inaccuracy of transistor level simulation could come from the uncertainty of transistor compact model, since modeling of device nonlinearity (appears to be the harmonics in the spectrum) is very challenging, especially when the signal level is low. Note that the variation of resistance of the current probe can also affect the measured spectrum, which can be verified by the simulation. However, using the measured S-parameters of the proposed probe for simulation shows an almost identical spectrum compared with that using an ideal 1-Ω probe, which confirms that our probe is sufficiently accurate for wideband EM emission measurements.

It should be emphasized that the proposed method can also work in the practical cases for specific ICs, such as an IC with several V_{DD}-V_{SS} pins or a complex IC made up of building blocks with isolated power domains. With the customized configuration of user-defined test points, the layout can be arranged based on the unit G-S-G probe cell on the IPD substrate to fulfill various testing requirements. Also, the layout of the unit probe cell is kept identical, and thus the measurement bandwidth will not be affected. This is very similar with the cases for the PCB level testing, which also needs to have customized PCB layout for a specific IC pin configuration. Furthermore, with the rearranged pads, the proposed IPD chip probe can be used to test a packaged IC. The IC can be bonded by the solder bump on the chip probe,

and the measurement bandwidth would be much better than the conventional probe built in the PCB level.

V. Conclusion

For achieving wideband measurement of conducted EM emission, we proposed a novel on-chip characterization technique using IPD chip probes up to the gigahertz range for ICs. The size expansion technique was adopted to achieve high precision resistance to meet the required probe specifications. With the microfabrication process, the 1- and 150-Ω probes were demonstrated to occupy only 0.55 mm × 0.77 mm and 0.83 mm × 1.49 mm, respectively. The probes were experimentally verified to comply with the specification of IEC 61967-4 direct coupling method. Compared with the probes realized by the conventional SMD with PCB, the results indicated that the applicable measurement frequency range can be significantly extended up to 15 GHz. Also, a ring VCO realized in 0.18-μm CMOS was used as the DUT for the on-chip test. The results proved that the probes can be used to perform the conducted EM emission measurement at higher frequency bands.

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