CMOS Distributed Amplifiers Using Gate–Drain Transformer Feedback Technique

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***Abstract*—This paper presents CMOS distributed amplifiers (DAs) using the proposed gate–drain transformer feedback technique. The feedback allows reuse of the traveling signal to achieve a high gain-bandwidth product while maintaining low power consumption of DAs. With the folded transmission lines and patterned ground shield, the miniaturized transformer has high quality factors and a well-controlled feedback coupling coefficient. Two DAs are realized using the proposed technique in both 0.18-μm and 90-nm CMOS technologies, respectively. The 0.18-μm CMOS DA achieves a gain of 9.5 dB with a 3-dB bandwidth of 32 GHz, and the noise figure (NF) ranges from 4.1 to 7.6 dB under a power consumption of 71 mW. Under a power consumption of 60 mW, the 90-nm DA demonstrates a gain of 7 dB, a bandwidth of 61.3 GHz, and an NF below 6.2 dB up to 40 GHz. The core areas of the 0.18-μm and 90-nm designs are only 0.58 and 0.41 mm^2, respectively.**

***Index Terms*—CMOS, distributed amplifier (DA), feedback, transformer, wideband.**

I. Introduction

WIDEBAND amplifiers operating in the microwave frequency range are of great interest for various applications. Different approaches have been proposed for wideband amplifier design [1]–[22] such as feedback amplifiers [3], distributed amplifiers (DAs) [4]–[20], [26], [27], and tuned amplifiers [21], [22]. The DA, using the concept of artificial transmission lines, can easily achieve a large bandwidth and reasonable gain. However, compared with other wideband amplifier configurations, the DA topology occupies a large chip area with considerable power dissipation. The low efficiency of the DA topology is mainly due to the gain of the amplifier being added instead of multiplied from each gain stage. The large chip area is because of the area-consuming inductive elements required in each section for the artificial transmission lines.

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Previously reported results of DAs were mostly fabricated in III–V [4], SiGe [5], [6], or silicon-on-insulator (SOI) CMOS [7] technologies to take advantage of the superior transistor characteristics. Lately, CMOS technology has also become an excellent candidate for DA design due to the continuous scaling of device feature sizes with impressive frequency responses under low power consumption. Nevertheless, it is still rather difficult to obtain a high-performance CMOS DA with low power consumption and a small chip area. Different approaches have been proposed to improve the DA characteristics. The cascode gain stage was used with an inductor connected between the two transistors [7]–[9], [15]–[18], [25]. The inductor can resonate with the parasitic capacitances to extend the bandwidth of the DAs. Under a power consumption of 135 mW, a DA with an 8.5-dB gain and a bandwidth of 52 GHz in 0.13-μm CMOS was reported [9]. The cascaded multi-stage DA was proposed to enhance the gain-bandwidth (GBW) product and reduce power consumption [10], [11]. A 70-GHz DA was realized in 90-nm CMOS with a GBW of 157 GHz [10]. A DA using the cascaded topology with a tapered transmission line segment also demonstrated a GBW of 370 GHz [11]. An internal feedback configuration was employed to increase the gain with a minimum reduction in bandwidth [12]. In a three-stage DA, the signal was amplified twice in the core DA (second stage) via the feedback, and a 660 GBW was achieved. A stage-scaling technique was proposed mainly to improve the efficiency of the DA [13], in which the transistor size and transmission line impedance were scaled along the stages. A 110-GHz bandwidth and 13.2% peak power-added efficiency was obtained. A DA with a distributed active input balun was proposed in 65-nm CMOS, which achieved linearity improvement and a GBW of 818 GHz [14]. The coupled gate-line inductors were used to extend the bandwidth without additional power consumption, which also improved the input matching [15]. The DA implemented in 0.18-μm CMOS demonstrated a 10-dB gain with a 16-GHz bandwidth while only consuming 21 mW, but with a relatively large chip area of 1.19 mm^2. The independently coupled gate line and coupled drain line were employed to reduce the chip area [16], and a DA with a gain of 15 dB and a bandwidth of 12 GHz was achieved in 0.13-μm CMOS.

In this paper, we propose a gate–drain transformer feedback technique for DA design to improve the GBW product and reduce the power consumption simultaneously. Differing from the conventional DA configuration and the aforementioned coupled gate/drain line configurations [15], [16], the signals propagating in the gate line and drain line are coupled through a gate–drain transformer in the proposed design technique. With the feedback coupling, the output signal from the drain line of the pre-

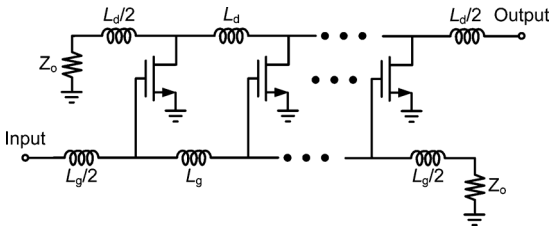

Fig. 1. Conventional MOS DA.

vious stage can be reused as a part of the input gate-line signal and to be amplified again. The feedback transformer is designed in a folded topology by the patterned-ground-shield (PGS) [23] transmission lines with a slow-wave effect to minimize the chip area. We demonstrate DAs in both 0.18-μm and 90-nm CMOS technologies with superior figures-of-merit (FOM). This paper is organized as follows. Section II introduces the fundamentals of DA design. Section III presents the design and analysis of the proposed gate–drain transformer feedback technique. Section IV provides the design and layout considerations of the transformer in the proposed DA. Section V shows the measurement results and comparison with prior works, and Section VI concludes this work.

II. Fundamentals of DA

Fig. 1 shows a conventional DA constructed by MOSFETs and inductors. The basic idea is to use the inductive elements together with the inherent parasitic capacitances in the active devices to create artificial transmission lines for wideband operation. The DA configuration is comprised of two (gate and drain) artificial transmission-line sections with series inductances and shunt capacitances. The inductors absorb the parasitic capacitances introduced from the transistors to achieve a wideband characteristic of the amplifier. As the input signal propagates through the transistors by the gate line, the amplified signal of each stage is accumulated at the output by the drain line. The following equations provide simple guidelines for DA design, including the impedances of the gate and drain lines and also the signal phases in the gate (ϕ_g) and drain (ϕ_d) lines [15]:

$$Z_0 = \sqrt{\frac{L_g}{C_g}} = \sqrt{\frac{L_d}{C_d}} \tag{1}$$

$$\varphi_g = \omega\sqrt{L_g C_g} \tag{2}$$

$$\varphi_d = \omega\sqrt{L_d C_d} \tag{3}$$

$$f_c = \frac{1}{\pi\sqrt{L_g C_g}} = \frac{1}{\pi\sqrt{L_d C_d}} \tag{4}$$

where L_g and L_d are the equivalent inductances of the gate line and drain line, respectively ;C_g and C_d are the equivalent parasitic capacitances of the gate and drain nodes, respectively, and f_c is the cutoff frequency. Z_0 is the system characteristic impedance, which is typically 50 Ω. To ensure the forward signal can be constructively added, the propagation delay of the gate line and drain line should be made equal $(\phi_g = \phi_d)$ so that the signals are in phase.

Design and implementation of a DA in CMOS technology encounters several challenges. One major concern is the lossy Si substrate, which could introduce significant undesired parasitics and degrade the circuit performance. The DA structure often occupies a large chip area, making the parasitic effect more pronounced and more unpredictable in practical design. The spiral inductors are also commonly used in CMOS DAs [2], [8], [15], [16]. The low-Q inductors introduce losses and reduce the gain of the amplifier. The relatively low gain of CMOS at high frequencies also makes it difficult to achieve high-gain DAs. One possible solution is to use more gain stages, but with increased power consumption and chip area. A stage number ranging from 3 to 6 is typically used for CMOS DA design [8], [15]–[17], [19].

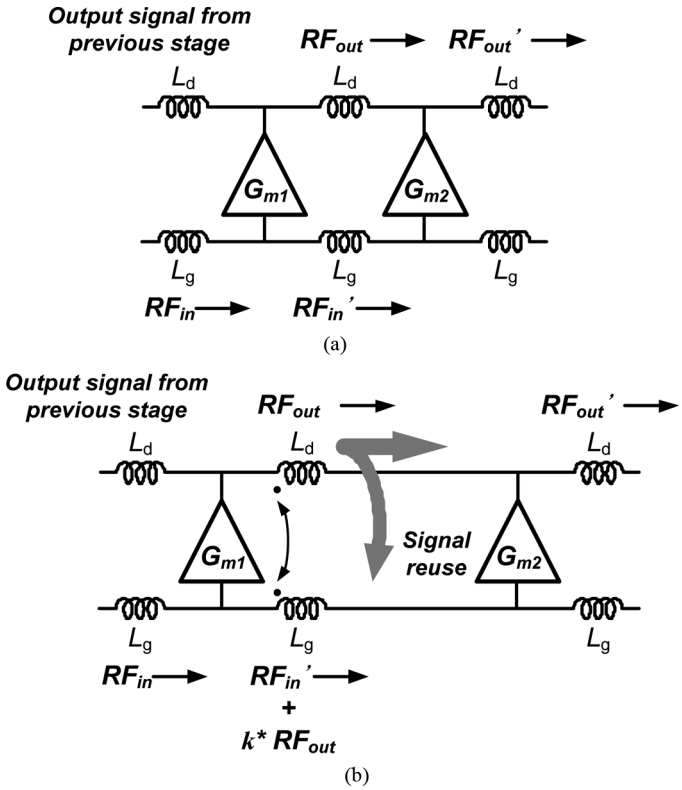

Fig. 2. Conceptual plot to illustrate the proposed gate–drain coupling feedback DA design. (a) Conventional DA. (b) Gate–drain coupling DA with a coupling factor k.

III. Gate–Drain Transformer Feedback DA

Fig. 2 illustrates the concept of the proposed gate–drain transformer feedback by comparing it to the conventional DA. Fig. 2(a) shows the signal propagation and amplification in a conventional DA topology. The input signal coming from the previous stage $(\mathrm{RF_{in}})$ through the gate line is amplified and then appears at the drain node. This signal combining with the output signal from the previous stage becomes the total output signal $(\mathrm{RF_{out}})$ of this section. Meanwhile, part of the input signal $(\mathrm{RF'_{in}})$ continuously travels in the gate line, and is amplified by the following gain stage. With a proper design of delays in both the gate line and drain line, the signal through each stage can be added in the drain line, and the output is the sum of all the gain stages $(\mathrm{RF'_{out}})$. Note that the gate line and drain line are connected to the input and output of each stage independently in the

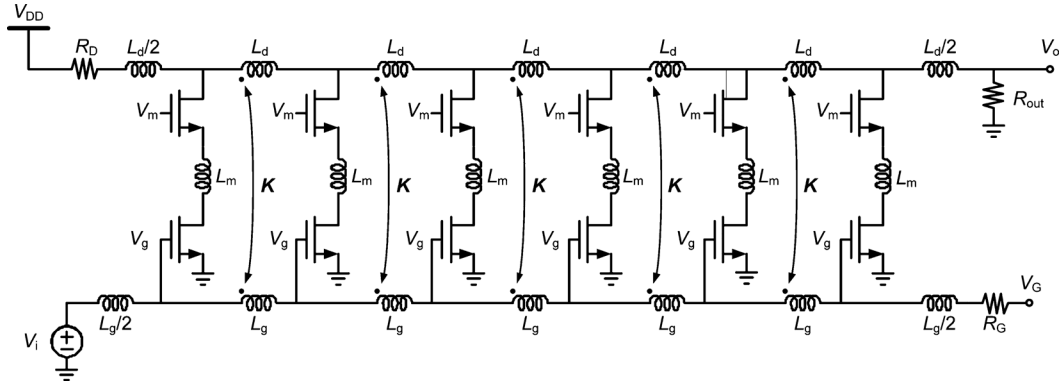

Fig. 3. Circuit topology of the proposed six-stage gate–drain transformer coupling DA.

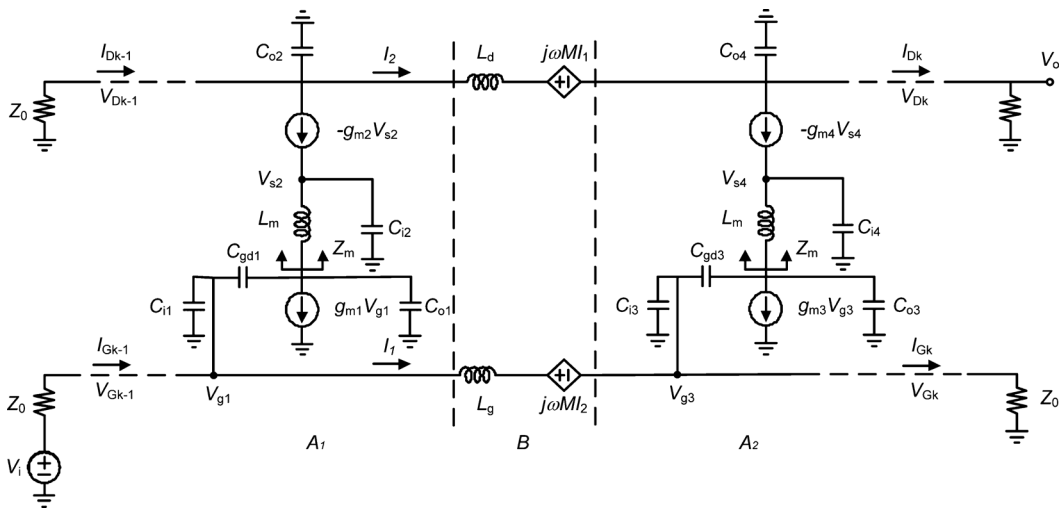

Fig. 4. Small-signal equivalent-circuit model of a simplified two-stage gate–drain coupling DA using the current-controlled voltage sources to model the transformer.

conventional DA configuration. As a result, the gate signal and drain signal also travel individually. Fig. 2(b) illustrates the concept of signal propagation in the proposed transformer feedback DA. With proper design of the gate–drain feedback, the output signal from the drain line of the previous stage $(\mathrm{RF_{out}})$ is coupled back to the gate line with a coupling coefficient k and can be reused as the input signal for the next stage. Consequently, the signal is amplified again to achieve a high GBW product under small power consumption.

It should be emphasized that the coupled transformers are bidirectional devices, and the energy transfer percentage for both feedback and feedforward is identical. However, the signal level in the drain line is much higher than that in the gate line after amplification. As a result, the energy coupling from the drain line to the gate line (feedback) dominants, whereas that from the gate line to drain line (feedforward) is relatively small and can be neglected. This is also evident from simulation, in which an obvious increase of the gate-line signal level can be observed with feedback coupling. In addition, simulation was performed to check the impact of feedback on the phase of the gate-line signal. With a proper design of the transformer coupling factor, the phase change is not obvious, which implies a good phase match between the fed back signal and the original signal on the gate line. The increased gate-line signal with the gate–drain coupling also suggests a good phase match between the two signals.

Fig. 3 shows the detailed circuit configuration of the proposed gate–drain transformer feedback DA. The cascode design with reduced Miller effect and improved gain is used for the gain cell in each stage. To further enhance the GBW product, a peaking inductor L_m is connected between the drain of the common-source stage and the source of the common-gate stage to resonate with the parasitic capacitances introduced by the transistors and also the substrate. In this design, the output signal is effectively reused through the transformer feedback with a well-controlled coupling factor k, as will be explained in Section IV in detail. The 50-Ω resistors R_G and R_D function as terminations for the drain and gate lines, respectively, to prevent power reflection. A six-stage design is employed to achieve a high GBW product. Note the last stage of the DA is not coupled back to the gate line of the first input stage. With a total of six gain stages, only five of them employ the gate–drain feedback configuration. The following derives the analytical equations of the proposed gate–drain feedback DA topology.

Fig. 4 shows the simplified small-signal model of the DA for circuit analysis, which includes two identical unit gain stages (A_1 and A_2) and one gate–drain coupling transformer (B), where $C_{\mathrm{i}1}$ and $C_{\mathrm{i}2}$ represent the input capacitances of M_1

(gate) and M_2 (source), respectively; C_{gd1} is the gate–drain capacitance of M_1; C_{o1} and C_{o2} are the equivalent output capacitances at the drain node of M_1 and M_2, respectively. Also, g_{m1} and g_{m2} are the transconductances of M_1 and M_2, respectively, and Z_m is the impedance looking from the drain of M_1 into L_m. Similar parameter definitions can be applied to the second gain stage. In a transformer, the input current in the primary coil induces an alternating magnetic flux. By coupling through the air and silicon substrate, the flux linked to the secondary coil also changes, and consequently an electromotive force (EMF) is induced in the secondary coil. Therefore, the coupling effect of the transformer can be described by two current-controlled voltage sources, $j\omega MI_1$ and $j\omega MI_2$, as shown in Fig. 4, where M is the mutual inductance between the primary and secondary coils.

The transmission ($ABCD$) matrix is used for analytical equation derivation owing to the cascade of the DA. The 4×4 matrix describing the overall input–output relation can be defined as follows [24]:

$$\begin{bmatrix} V_{DK-1} \\ I_{DK-1} \\ V_{GK}-1 \\ I_{GK}-1 \end{bmatrix} = \begin{bmatrix} D_{11} & D_{12} & D_{13} & D_{14} \\ D_{21} & D_{22} & D_{23} & D_{24} \\ D_{31} & D_{32} & D_{33} & D_{34} \\ D_{41} & D_{42} & D_{43} & D_{44} \end{bmatrix} \begin{bmatrix} V_{DK} \\ I_{DK} \\ V_{GK} \\ I_{GK} \end{bmatrix} \quad (5)$$

where the voltages and currents are denoted in Fig. 4, and the voltage gain can be obtained by V_{DK}/V_{GK-1}. The transmission matrix of each gain stage with the peaking inductor L_m can be expressed as

$$[A_1] = [A_2] = [A] = \begin{bmatrix} 1 & 0 & 0 & 0 \\ Y_{22} & 1 & Y_{21} & 0 \\ 0 & 0 & 1 & 0 \\ Y_{12} & 0 & Y_{11} & 1 \end{bmatrix} \quad (6)$$

where Y_{11}, Y_{12}, Y_{21}, and Y_{22} represent the two-port Y-parameters of the unit gain stage, and can be obtained by the small-signal model. The $ABCD$ matrix for the gate–drain coupling transformer can be derived as

$$B = \begin{bmatrix} 1 & j\omega L_d & 0 & j\omega M \\ 0 & 1 & 0 & 0 \\ 0 & j\omega L_g & 1 & j\omega M \\ 0 & 0 & 0 & 1 \end{bmatrix}. \quad (7)$$

The matrix $[C]$ can be simply obtained by $[A_1] \times [B] \times [A_2]$, as shown in (8) at the bottom of this page. With the input/output ports, and the gate/drain lines terminated by Z_0, the gain of the amplifier can be calculated based on (9), shown at the bottom of this page. Note that (9) is a modified $ABCD$ matrix in which the gate and drain line terminations are considered by replacing I_{DK-1} and I_{GK} as $-V_{DK-1}/Z_0$ and V_{GK}/Z_0, respectively, and the effect of source and load impedances are also taken into account in the matrix parameters directly. Finally, (9) could be rewritten as (10), shown at the bottom of the following page, to obtain the amplifier gain by using the reverse matrix $[D']$. The equivalent transconductance G_m of the unit gain stage can be used to simplify the calculation, which can be expressed as [15]

$$G_m = -g_{m1} \frac{1}{1+sZ_m c_{01}} \frac{1}{1+s\frac{C_{i2}}{g_{m2}}}. \quad (11)$$

It can also be proven that $I_{GK-1} = V_{GK-1}/Z_{11}$, where Z_{11} is the Z matrix parameter of $[A]$. The voltage gain V_{DK}/V_{GK-1} could then be calculated as

$$\frac{V_{DK}}{V_{GK-1}} = (D'_{11}G_m Z_0 + D'_{12}G_m + D'_{13} + D'_{14}/Z_{11}). \quad (12)$$

Fig. 5 compares the calculated gain (0.18-μm CMOS DA) based on (12), the simulated gain by the small-signal model, as shown in Fig. 4, and also the result obtained from the simplified two-stage DA using large-signal model (with the exact same design of the final DA). Note the small-signal parameters are

$$[C] = \begin{bmatrix} 1+j\omega(L_dY_{22}+MY_{12}) & j\omega L_d \\ 2Y_{22}+j\omega Y_{21}(L_gY_{22}+MY_{12})+j\omega Y_{22}(L_dY_{22}+MY_{12}) & j\omega(L_gY_{21}+L_dY_{22})+1 \\ j\omega(L_gY_{22}+MY_{12}) & j\omega L_g \\ 2Y_{12}+j\omega Y_{11}(L_gY_{22}+MY_{12})+j\omega Y_{12}(L_dY_{22}+MY_{12}) & J\omega(L_dY_{12}+L_gY_{11}) \\ j\omega(L_dY_{21}+MY_{11}) & j\omega M \\ 2Y_{21}+j\omega Y_{21}(L_gY_{21}+MY_{11})+j\omega Y_{22}(L_dY_{21}+MY_{11}) & j\omega M(Y_{21}+Y_{22}) \\ 1+j\omega(L_gY_{21}+MY_{11}) & j\omega M \\ 2Y_{11}+j\omega Y_{11}(L_gY_{21}+MY_{11})+j\omega Y_{12}(L_dY_{21}+MY_{11}) & j\omega M(Y_{11}+Y_{12})+1 \end{bmatrix} \quad (8)$$

$$\begin{bmatrix} V_{DK-1} \\ -V_{DK-1}/Z_0 \\ V_{GK-1} \\ I_{GK-1} \end{bmatrix} = \begin{bmatrix} C_{11}+C_{12}/Z_0 & C_{12} & C_{13} & C_{14} \\ C_{21}+C_{22}/Z_0 & C_{22} & C_{23} & C_{24} \\ C_{31}+Z_0C_{41}+(C_{32}+Z_0C_{42})/Z_0 & C_{32}+Z_0C_{42} & C_{33}+Z_0C_{43} & C_{34}+Z_0C_{44} \\ C_{41}+C_{42}/Z_0 & C_{42} & C_{43} & C_{44} \end{bmatrix} \begin{bmatrix} V_{DK} \\ I_{DK} \\ V_{GK} \\ V_{GK}/Z_0 \end{bmatrix} \quad (9)$$

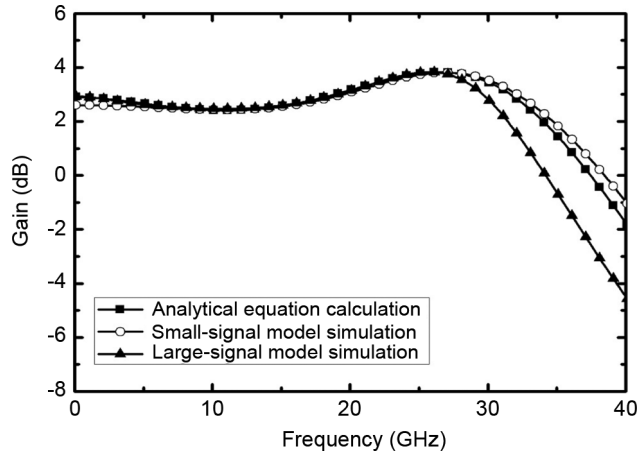

Fig. 5. Gain of the simplified two-stage gate–drain coupling DA obtained by three different approaches.

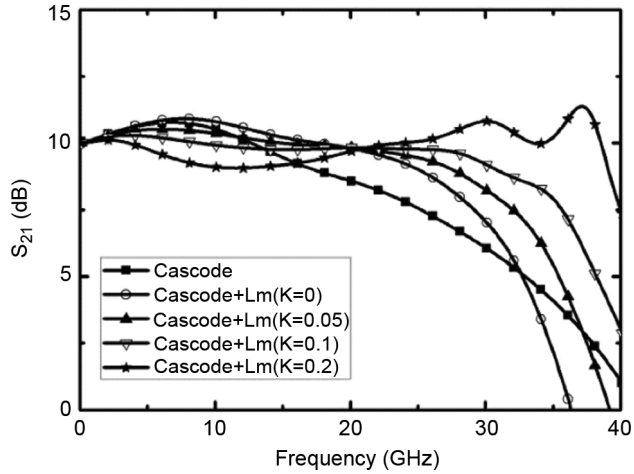

Fig. 6. Simulated results of a six-stage DA in 0.18-μm CMOS with different L_m and k factors.

extracted from the foundry provided transistor model. An excellent agreement is obtained among the calculated/simulated results with three different approaches.

The larger bandwidth in the analytical equation and small-signal model simulation could be attributed to the simplified small-signal model with less parasitic effects, and the slight difference at high frequencies between the small-signal model simulation and analytical equation is due to the neglected higher order terms in the matrix calculation. It should be emphasized that the gain peaking effect and bandwidth improvement can be observed in all the three cases. As will be shown in Section IV, the coupling factor in the proposed DAs is designed on purpose to increase with frequency for compensating the gain reduction and signal loss at high frequencies. This is also a key design feature to achieve excellent GBW product of DAs under low power consumption in this study.

Fig. 6 compares the simulated transfer characteristic S_{21} under different conditions to investigate the effect of L_m peaking and gate–drain coupling on circuit performance. Using 0.18-μm CMOS with six gain stages and ideal transformers, the 3-dB bandwidth of the DA with a simple cascode unit gain cell is $\sim$ 20 GHz. By adding L_m peaking, the bandwidth is improved up to $\sim$ 25 GHz. For the configuration proposed in this design with a proper gate–drain coupling, the bandwidth can be enhanced even up to $\sim$ 38 GHz ($k = 0.2$), which is about 1.9$\times$ compared with the conventional cascode gain stage design. As can be seen, the bandwidth enhancement is relatively sensitive to the coupling factor k, as can be observed in Fig. 6. If the amount of coupling is too large, the circuit could be unstable. In general, the bandwidth enhancement is ultimately limited by the circuit stability due to the positive feedback employed between the gate line and drain line. In the proposed DA design, the peaking effect of the transformer and feedback coefficient are designed at around the 3-dB bandwidth for a single stage, as the gain stage increases, the gain enhances with a similar bandwidth. A well-controlled k factor, especially on the lossy Si substrate, is critical in practical design, and the details will be discussed in the following section.

It should be mentioned that the concept of the proposed gate–drain feedback is quite different from the commonly used termination impedance optimization DA and/or the DA with m-derived matching network [6], [9], [11], [12]. The above two approaches focus on improving the matching for better DA bandwidth. In contrast, the proposed DA with improved bandwidth and efficiency is due to the positive feedback and reused drain signal by the gate–drain feedback transformer. This can be clearly seen from the simulated results in Fig. 6 in which the DA characteristics are very sensitive to the coupling coefficient.

$$\begin{bmatrix} V_{DK} \\ I_{DK} \\ V_{DK} \\ V_{GK}/Z_0 \end{bmatrix} = \begin{bmatrix} D'_{11} & D'_{12} & D'_{13} & D'_{14} \\ D'_{21} & D'_{22} & D'_{23} & D'_{24} \\ D'_{31} & D'_{32} & D'_{33} & D'_{34} \\ D'_{41} & D'_{42} & D'_{43} & D'_{44} \end{bmatrix} \begin{bmatrix} V_{DK-1} \\ -V_{DK-1}/Z_0 \\ V_{GK-1} \\ I_{GK-1} \end{bmatrix}$$

where

$$\begin{bmatrix} D'_{11} & D'_{12} & D'_{13} & D'_{14} \\ D'_{21} & D'_{22} & D'_{23} & D'_{24} \\ D'_{31} & D'_{32} & D'_{33} & D'_{34} \\ D'_{41} & D'_{42} & D'_{43} & D'_{44} \end{bmatrix} = \begin{bmatrix} C_{11} + C_{12}/Z_0 & C_{12} & C_{13} & C_{14} \\ C_{21} + C_{22}/Z_0 & C_{22} & C_{23} & C_{24} \\ C_{31} + Z_0 C_{41} + (C_{32} + Z_0 C_{42})/Z_0 & C_{32} + Z_0 C_{42} & C_{33} + Z_0 C_{43} & C_{34} + Z_0 C_{44} \\ C_{41} + C_{42}/Z_0 & C_{42} & C_{43} & C_{44} \end{bmatrix}^{-1} \quad (10)$$

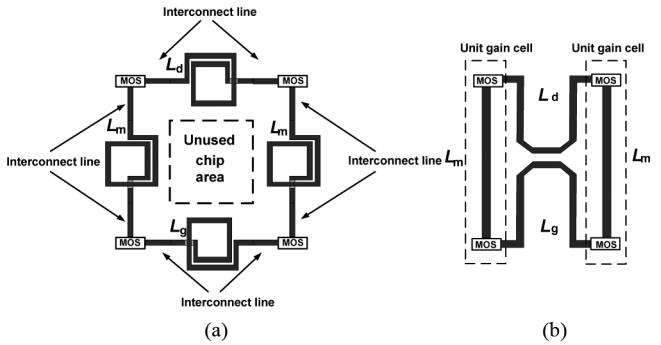

Fig. 7. Layout arrangement of DA. (a) Design using spiral inductors for gate/drain lines and peaking inductors. (b) Proposed layout design using transmission lines for gate–drain coupling transformer and peaking inductor.

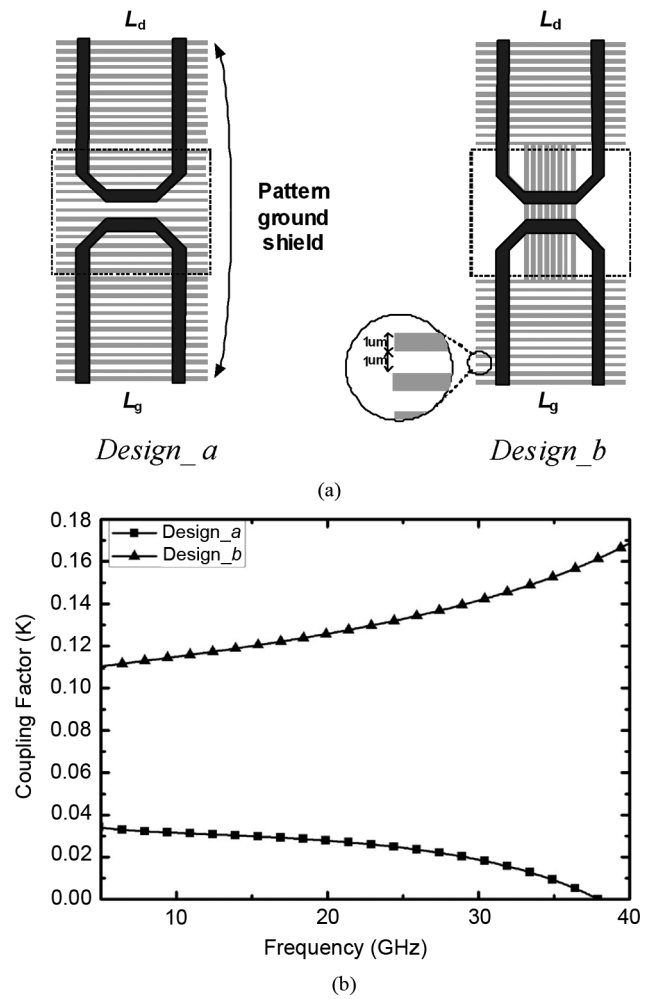

Fig. 8. Transformer design with folded transmission lines. (a) Different PGS designs. (b) Corresponding coupling factors.

IV. Design of Feedback Transformer

As mentioned earlier, one main issue for DA design is the relatively large chip area. With the gate/drain lines and peaking inductors designed by spiral inductors, the layout arrangement could be difficult and may leave a large unused chip area, as illustrated in Fig. 7(a). If using spiral inductors in the proposed design, the circuit implementation would also become more difficult. As the geometry changes, the mutual inductance and self-inductance of a spiral inductor will change simultaneously. This makes the design of the proposed DA complicated. The lengths of interconnects are also not easily estimated before the layout is completed.

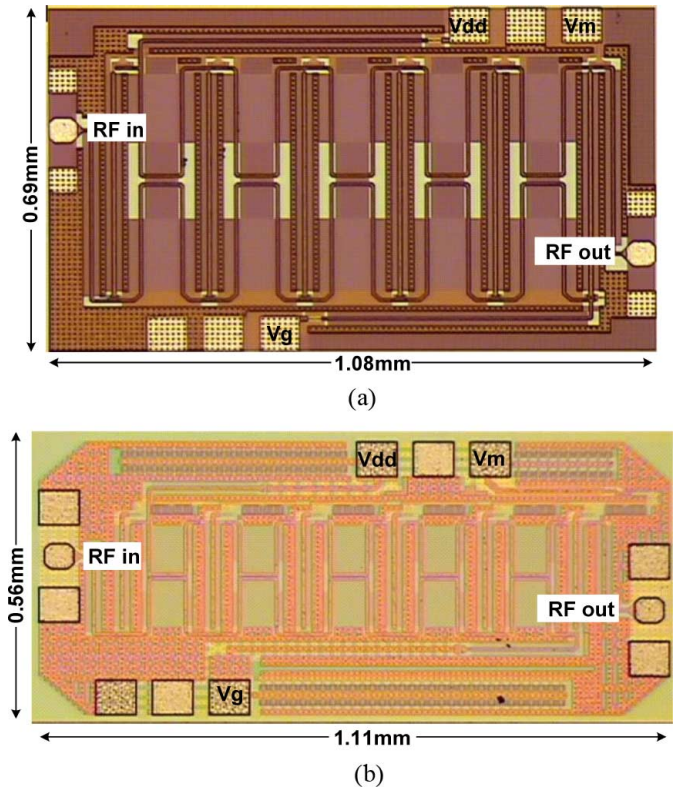

Fig. 9. Chip micrographs of the proposed gate–drain transformer feedback DAs. (a) 0.18-μm CMOS DA. (b) 90-nm CMOS DA.

Two typical design approaches for the transformer are often used in the standard CMOS process, one is the stacked structure, and the other is the coplanar topology. Previous analysis (see Fig. 6) suggests that a relatively small k factor is sufficient for the gate–drain coupling, and thus the coplanar-type design is more suitable in this design. A transformer using folded transmission lines is proposed. Fig. 7(b) illustrates the layout of two cascaded unit gain stages using the transmission lines for the peaking inductor L_m and the gate–drain feedback transformer. Compared with the transformer using spiral inductors, the coplanar transmission-line design has much fewer bends and without the need of vias. Consequently, the loss is reduced and higher quality factors can be obtained. During the design procedure, the width of the transmission lines was fixed first for Z_0 of 50 Ω, and the total length of each line is also kept as constant. The coupling factor can then be easily designed by adjusting the spacing between the two transmission lines and the length of the coupled region.

To further improve the quality factor and also have a well-controlled coupling factor, the pattern-ground-shield (PGS) technique is adopted [23]. Fig. 8(a) compares two different PGS designs (*Design_a* and *Design_b*) of the coupling transformer using folded transmission lines, and Fig. 8(b) shows the corresponding coupling factor as a function of frequency for the 0.18-μm CMOS design, simulated by the EM

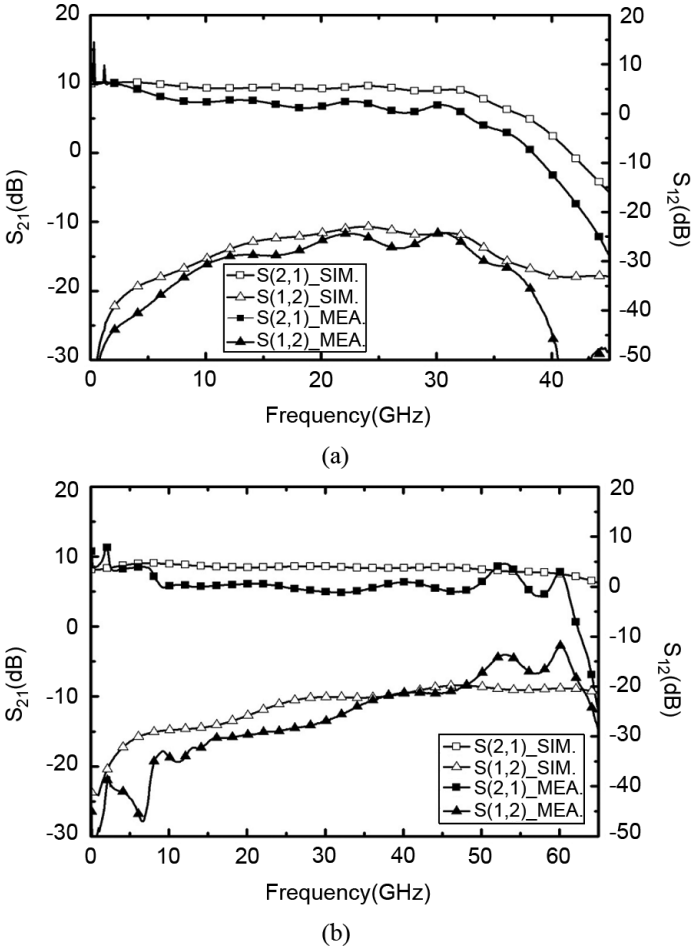

Fig. 10. Measured and simulated S_{21} and S_{12} of the proposed gate–drain transformer feedback DAs. (a) 0.18-μm CMOS DA. (b) 90-nm CMOS DA.

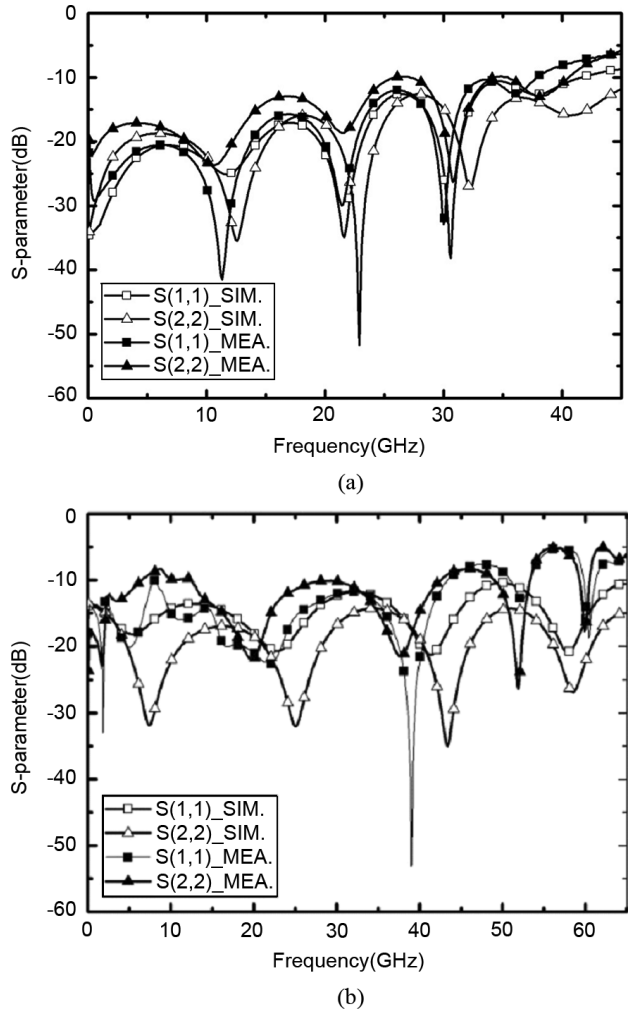

Fig. 11. Measured and simulated S_{11} and S_{22} of the proposed gate–drain transformer feedback DAs. (a) 0.18-μm CMOS DA. (b) 90-nm CMOS DA.

tool. In *Design_a*, the metal stripes are in parallel with L_g and L_d in the strong coupling region, which increases the loss and decreases the coupling coefficient, especially at high frequencies. On the other hand, *Design_b* shows the PGS layout in our final design, in which the strips of the PGS are arranged to be vertical with the gate line and drain line in the strong coupling region. The PGS can cut off the induced loop current in the substrate, resulting in equivalently increased mutual inductance between L_g and L_d with frequency and the coupling factor k. The enhanced k factor can compensate the inherently decreased gain at high frequencies for the transistor, which is beneficial to maintaining a constant gain over a wide frequency range of the amplifier. By electromagnetic (EM) simulation, it can be observed that the quality factor increases as the width and spacing of the PGS stripes reduce. In our design, the width and the interval of the ground shield metal lines are both 1 μm. The Q factor increases by about 10%–25% in general in the frequency range of interest.

V. Measured Results and Discussion

The proposed DAs with gate–drain transformer feedback coupling were implemented in both 0.18-μm and 90-nm CMOS technologies and the chip micrographs are shown in Fig. 9(a) and (b), respectively. The core area of the 0.18-μm design is only 0.58 (0.98×0.59) mm^2, and that for the 90-nm design is only 0.41 (0.97×0.42) mm^2. The S-parameters were measured by the Agilent E4440A network analyzer, as shown in Figs. 10 and 11, together with the simulated results for the transmission (S_{21} and S_{12}) and reflection characteristics (S_{11} and S_{22}), respectively. The 0.18-μm design is biased at $V_d = 3$ V, $V_m = 1.7$ V, and $V_g = 0.75$ V with a total power consumption of 71 mW, and those for the 90-nm design are 2.2 V, 1.5 V, 0.66 V, and 60 mW, respectively. As shown in Fig. 10, the 0.18-μm CMOS DA achieves a power gain of 9.5 dB and a 3-dB bandwidth of 32 GHz. The 90-nm design also shows a power gain of 7 dB and a 3-dB bandwidth up to 61.3 GHz. The input and output reflection coefficients of the 0.18-μm DA remains under -9.8 dB within the bandwidth, and those are also all below -8.8 dB up to 50 GHz (< -5.7 dB up to 61.3 GHz) for the 90-nm design. Fig. 12 compares the simulated and measured noise characteristics of both designs. The measured noise figure (NF), as shown in Fig. 12(a), ranges from 4.1 to 7.6 dB within the 3-dB bandwidth of the 0.18-μm DA, and the NF is below 6.2 dB up to the measurement limitation of 40 GHz for the 90-nm design, as shown in Fig. 12(b). The measured and simulated group-delay variations are shown in

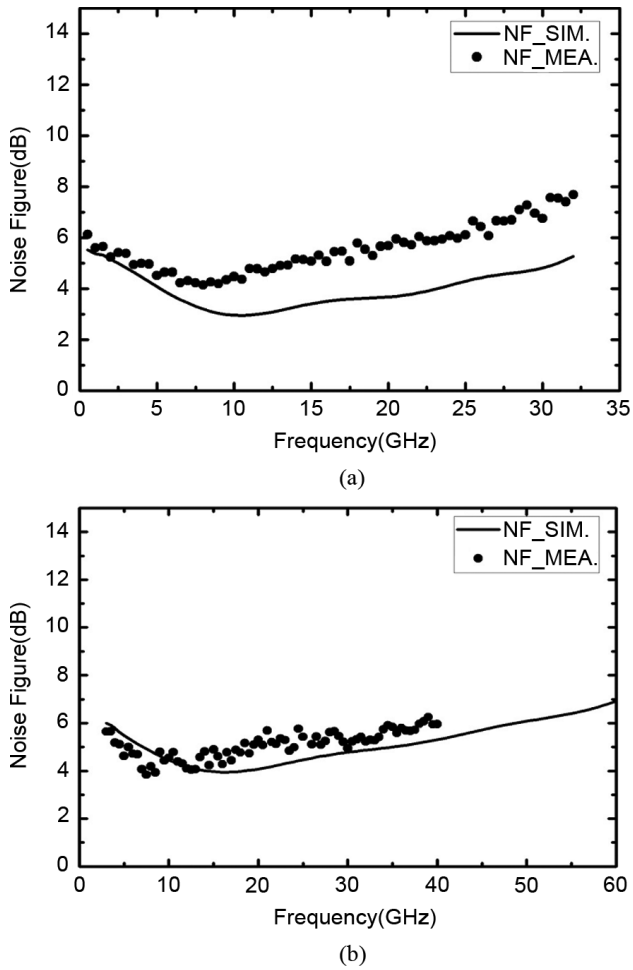

Fig. 12. Measured and simulated NFs of the proposed gate–drain transformer feedback DAs. (a) 0.18-μm CMOS DA. (b) 90-nm CMOS DA.

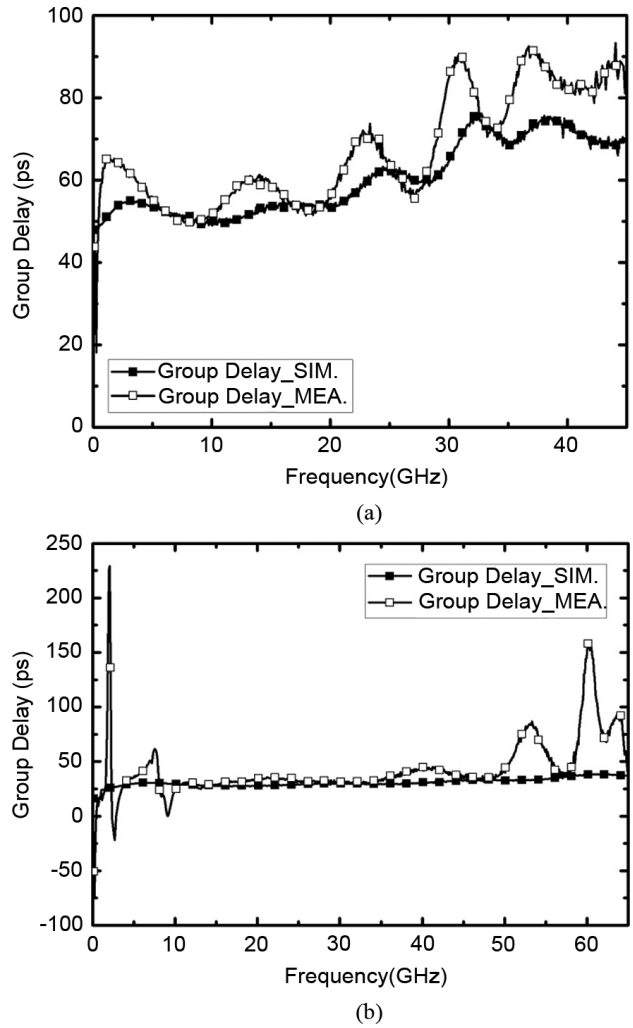

Fig. 13. Measured and simulated group delay of the proposed gate–drain transformer feedback DAs. (a) 0.18-μm CMOS DA. (b) 90-nm CMOS DA.

Fig. 13(a) and (b), which are 55 ± 35 ps for the 0.18-μm design and 75 ± 75 ps for the 90-nm design (without considering the low-frequency peak), respectively. Based on two-tone measurements ($\Delta f = 1$ MHz), the extrapolated third-order intermodulation intercept point (IIP3) at 20 GHz is 2.5 dBm for the 0.18-μm design and that at 40 GHz is 3.9 dBm for the 90-nm DA.

Fig. 14 presents the stability factors of both the 0.18-μm and 90-nm CMOS DAs. The 0.18-μm design achieves unconditional stability with $K > 1$ in the measured frequency range (from 10 MHz to 45 GHz). The 90-nm DA also shows $K > 1$ at most frequencies, but becomes slightly smaller than one at around the 3-dB frequency (minimum value $\sim$ 0.99). The reason for the K very close to one at high frequencies in 90-nm CMOS can be attributed to the insufficient dc bypass using the metal–insulator–metal (MIM) capacitances. By a modified design using MOS bypass capacitances with increased capacitance density, the K factor is well above one in the 0.18-μm CMOS DA.

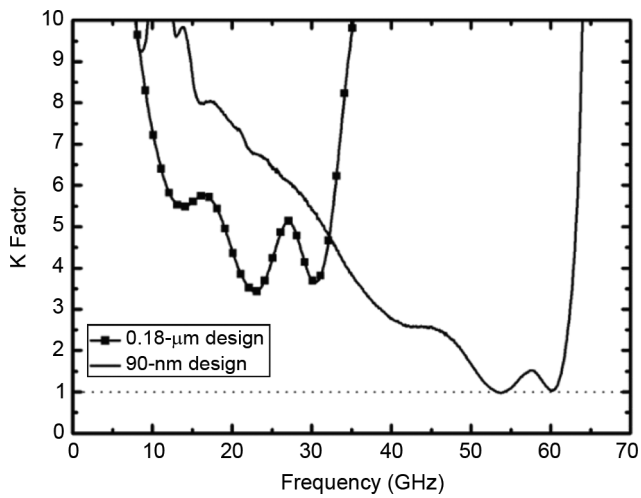

Fig. 14. Stability factors of both the 0.18-μm and 90-nm CMOS DAs.

Table I summaries the circuit performance and also the comparison with prior works. As can be seen, the DAs using the proposed transformer feedback design consume much smaller power while with a compact chip area. The achieved FOMs are among the best compared with previously published works. Note f_T of 60, 90, and 120 GHz are used for the 0.18-μm, 0.13-μm, and 90-nm MOS transistors, respectively.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

	This work Design_I	This work Design_II	[2]	[8]		[9]	[10]	[11]	[12]	[17]	[19]
Technology	0.18μm CMOS	90nm CMOS	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS	0.13μm CMOS	90nm CMOS	90nm CMOS	90nm CMOS	0.18μm CMOS	90nm CMOS
S_{21} (dB)	9.5	7	10	16.2	20	8.5	7	14	19	9.5	7.4
BW (GHz)	32	61.3	44	33.4	39.4	52	70	73.5	74*	32	80
GBW (GHz)	95.5	137	139	216	394	138	157	370	660	95.5	190
P_{DC} (mW)	71	60	103	260	250	142	122	84	84	97	120
Core area (mm^2)	0.58	0.41	0.98	1.81	1.76	1.76	0.72	1.72	1.19	0.49	0.37
FOM[1]	38.7	46.5	15.3	7.6	14.9	6.2	14.9	21.3	N/A	33.5	35.7
FOM[2] ($1/(W\cdot mm^2)$)	10.1	10.2	--	--	--	--	21.2	--	N/A	--	--

$FOM^1 = 1000 \cdot \frac{GBW}{P_{DC} \cdot f_T \cdot Area}$ $FOM^2 = 1000 \cdot \frac{GBW}{P_{DC} \cdot f_T \cdot Area} \cdot \frac{P1_{dB}}{NF}$

*Not 3-dB bandwidth.

VI. CONCLUSION

This paper has presented the design of DAs using the proposed gate–drain transformer feedback technique. By the gate–drain transformer coupling, the signal was reused to reduce the power consumption significantly, while maintaining a large GBW product. The gate/drain lines were arranged in a folded manner with the pattern ground shield to minimize the chip size and obtain a well-controlled coupling coefficient. With 0.18-μm and 90-nm CMOS, respectively, the 3-dB bandwidths of 32 and 61.3 GHz were demonstrated under power consumptions of 71 and 60 mW, and the core areas were only 0.58 and 0.41 mm^2. The achieved FOMs are among the best compared with previously published results.

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