An Inductorless 20-Gbaud Overshoot Suppression Modulator Driver Using Interleave Frequency Variant Feedback in 90-nm CMOS

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***Abstract*— An inductorless modulator driver with effective overshoot suppression and a large swing for high-speed optical communications is presented. A novel interleave frequency variant feedback (IFVF) technique is proposed, which employs active feedback loops with the *RC* degeneration. The *RC* degeneration allows place the pole in the overall transfer function to shape the waveform for overshoot and ringing suppression. Using a 90-nm complementary metal oxide semiconductor (CMOS) technology, the driver achieves a maximum 3.4 V_{pp} differential output voltage swing. Clear eye diagrams for non-return to zero (NRZ) and pulse amplitude modulation 4-level (PAM4) signal formats can be obtained up to 32 Gb/s and 20 Gbaud, respectively. The circuit consumes a total power of 560 mW and occupies a core area of only 0.092 mm^2.**

***Index Terms*— CMOS, high speed, inductorless, interleave feedback, linearity, modulator driver, nonreturn to zero (NRZ), pulse amplitude modulation 4-level (PAM4), silicon photonics.**

I. Introduction

In RECENT years, the strong demand for high data rates has driven the innovation of high-speed communication networks. The optical interconnects play an important role in this scenario. Compared with conventional electrical interconnects, optical interconnects using fibers or optical waveguides have the advantages of low loss and wide bandwidth (BW). Silicon photonics has attracted much attention recently owing to the potential of achieving a high integration level of the optical components and ICs for high-speed data transmission [1], [2], [3]. One very challenging topic of the ICs in silicon photonics applications is the modulator driver, which requires a relatively high output swing (typical > 3 V_{pp}) to obtain a sufficient extinction ratio [4], [5], [6].

With the requirements of large output swing and high-speed operation, the GaAs, InP, and SiGe technologies are often employed to realize the modulator drivers, taking advantage of the intrinsic material properties and high-performance transistors [7], [8], [9], [10]. The complementary metal oxide semiconductor (CMOS) technology is, however, a preferred solution for silicon photonics applications, considering the issues of cost and integration level. Previous studies have reported very good results of high-speed CMOS modulator drivers [11], [12], [13]. Solutions are proposed to solve the issues of low breakdown voltage and operating bandwidth, limited by the transistor characteristics. Many reported results are with the relatively simple nonreturn to zero (NRZ) modulation format, and the inductive components are often extensively employed to enhance the circuit performance [11], [14], [15]. The multilevel pulse amplitude modulation (PAM) signal format is an effective way to enhance the data rate, which allows doubling the data rate compared to NRZ [16], [17]; however, this also poses a significant challenge in the driver design, in which the transition among different data levels and intersymbol interference (ISI) become serious issues for high-speed operation. Fig. 1 illustrates the concepts of NRZ and PAM 4-level (PAM4) signal formats. The PAM4 signal divides the signal with four different levels to double the data throughput in an ideal case. In practice, the signal overshoot could be a critical issue, especially for PAM4. As shown in Fig. 1(a), the NRZ format is relatively insensitive to overshoot. In contrast, as the nonideal effects occur in the multilevel signaling, the intermediate voltage levels, such as 01 and 10, could be misjudged due to the reduced minimum eye-opening, leading to a signal integrity problem.

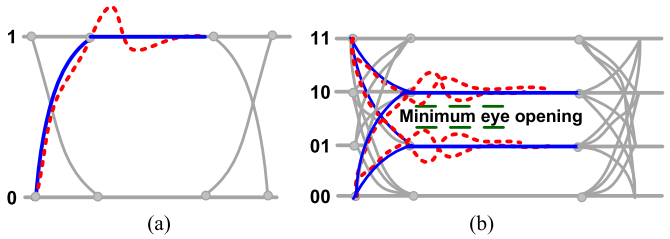

Fig. 1. Conceptual plot of the impact of signal overshoot on (a) NRZ and (b) PAM4 eye diagrams.

In this article, an inductorless 20-Gbaud 3-V_{pp} PAM4 modulator driver fabricated in 90-nm CMOS is demonstrated. The interleave frequency variant feedback (IFVF) technique is proposed to achieve a high data rate and large swing with effective overshoot suppression with high linearity. Two interleave active feedback loops with *RC* degeneration are employed in the cascaded amplifying stages, demonstrating a clear PAM4 eye diagram with equally spaced signal levels. This article is organized as follows. Section II describes the

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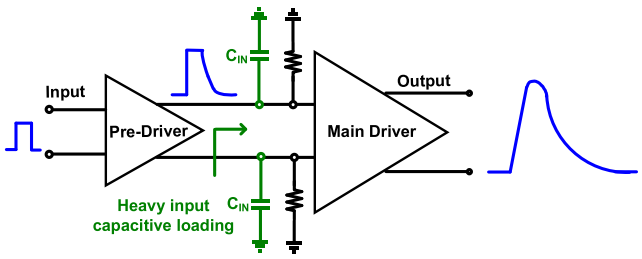

Fig. 2. Illustration of the ISI issue due to a long tail in a conventional modulator driver due to heavy capacitive loading in the main driver.

design considerations of the ISI issue for a high-speed modulator driver. Section III presents the topology and detailed analysis of the proposed circuit. Both analytical equations and simulated results are provided to explain the principle of the proposed design. The measured results and discussions are shown in Section IV. Finally, Section V concludes this work.

II. Design Considerations of Modulator Driver

A. ISI Issue in Conventional Modulator Drivers

Fig. 2 shows the conceptual plot of a typical cascade modulator driver, which includes a predriver and main driver [14]. The main driver often employs relatively large transistors to provide a sufficient driving capability for the modulator. As illustrated in Fig. 2, considerable parasitic capacitances of the transistors cannot be avoided in the main driver. The associated dominant pole will limit the bandwidth of the overall driver circuit. Given the time domain characteristics, the output waveform is distorted, showing a long tail owing to the heavy capacitive loading, the overall circuit response can be simplified as an RC lowpass behavior [18], and the duration of the tail can be estimated by

$$V_{\text{out}} = V_o\left(1 - e^{-T_{\text{bit}}/RC}\right)e^{-NT_{\text{bit}}/RC} \tag{1}$$

where V_0 and T_{bit} are the amplitude of the input pulse and the symbol time, respectively, and N is an integer to sample the signal level at different times. The voltage decay is inversely proportional to the RC time constant. If the operating data rate is high, the output voltage cannot decline to the desired threshold level within the desired time period. The long tail could increase the ISI, resulting in the bit error issue, which degrades signal integrity and limits the data rate.

B. Modulator Driver Design for ISI Improvement

To achieve the requirement of large output swing and broadband simultaneously, the topologies of the distributed amplifier (DA) and cascade inductive peaking amplifier are widely used in the prior arts for modulator driver design [15], [19], [20], [21]. The DA utilizes artificial transmission lines to absorb the parasitic capacitances of the transistors, which can effectively extend the bandwidth with a relatively flat gain response; however, it also brings out several issues. The DAs are often comprised of many stages to achieve a sufficient gain due to the additive mechanism of each gain cell. The long inductive gate and drain lines with the multiple gain stages could lead to significant chip area consumption. The large stage number and the loss introduced by the transmission lines also increase power consumption. In contrast, the cascade topology has the advantage of multiplying the gain of each stage and can obtain a high gain with a lesser stage number. The cascaded stages, however, usually lead to significant bandwidth reduction, and increasing power consumption and/or using inductive elements is essential to achieve a large bandwidth.

As illustrated in Fig. 2, a typical cascade topology needs the main driver for high output voltage swing, and heavy capacitive loading comes with the main driver resulting in limited bandwidth and a long tail issue of the output waveform. The inductor peaking techniques are commonly used for the broadband amplifier design to solve these problems, which can create zeros and/or complex conjugate poles in the transfer function for bandwidth extension [22]. One major issue of using inductive peaking is the relatively large chip area, especially for the advanced technology nodes with a high cost. Another problem is the deteriorated gain flatness in the cascade topology with inductive peaking for wideband applications. Compared to the DA with a relatively flat gain, the gain variation introduced by inductive peaking can cause serious signal ringing and overshoot, as illustrated in Fig. 1. For modulator driver applications, this could introduce a significant ISI issue, especially in the PAM4 signal format.

Compared with the works using the peaking inductors, the main advantage of the proposed inductorless modulator driver is the chip area. Note that the power consumption could be relatively higher due to the active feedback loop to enhance the bandwidth. It should be mentioned that using inductor peaking is more straightforward, where L and R in each stage can be adjusted to optimize the circuit performance. On the other hand, active feedback is more sensitive in terms of design parameters. One issue often encountered using inductor peaking or active feedback in practical design is overpeaking, which could cause a circuit stability problem. The proposed IFVF has the advantage of reducing ringing and improving circuit stability by adding RC degeneration to optimize the injected feedback signal.

In this article, we propose an inductorless modulator driver based on the cascade amplifier topology. The interleave frequency variant feedback technique is proposed to solve the above-mentioned issues. Without using any inductive components and external bias-Tee at the output, a very compact design can be achieved.

III. Circuit Design and Analysis

A. Circuit Topology

Fig. 3(a) shows the block diagram of the proposed IFVF modulator driver, which includes four transconductance stages, G_{m1}–G_{m4}, and one transimpedance gain stage Z_{t5}. Also, two interleave frequency variant active feedback loops, FV-G_{m1} and FV-G_{m2}, are employed, as indicated in Fig. 3(a), connecting from the output nodes of G_{m3} and G_{m4} back to the input nodes of G_{m2} and G_{m3}, respectively. The last stage of the transimpedance amplifier (TIA) converts the current signal to a large output voltage swing for driving the 50-Ω modulator.

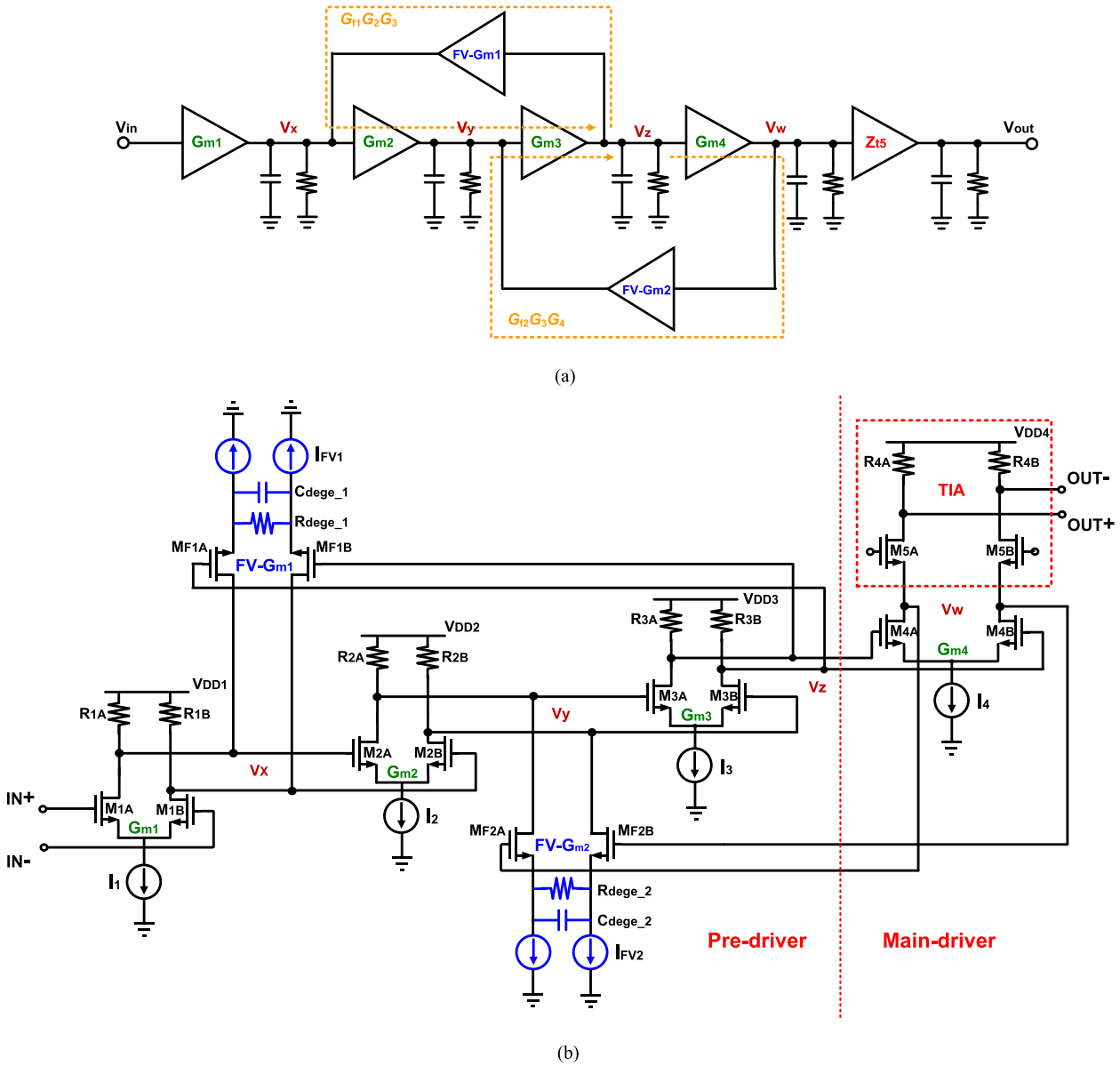

Fig. 3. (a) Block diagram of the proposed modulator driver. (b) Transistor level circuit schematic of the proposed modulator driver.

Fig. 3(b) presents the corresponding circuit topology at a transistor level. The gain cells G_{m1} to G_{m3} are realized by the common-source (CS) differential pairs with resistive loads. The cascode stage functions as the main driver, which includes two gain stages, G_{m4} and Z_{t5}. The CS stage G_{m4} of cascode converts the input voltage signal to current, while the common-gate (CG) stage functions as a TIA for the voltage output. The two frequency-variant gain stages in the feedback loops with RC degeneration are controlled by the bias current I_{FV1} and I_{FV2}.

In order to achieve a better tradeoff between power efficiency and bandwidth, the stage number of the predriver should be minimized. The proposed circuit topology includes a three-stage predriver together with a single-stage main driver for the output stage, as shown in Fig. 3(b). Owing to the desired large output swing, large transistors are needed for the main driver. The corresponding parasitic capacitances become significant, thereby limiting the bandwidth. With the nested configuration, two layers of active feedback in the three-stage pre-driver with a relatively high loop gain are an efficient design to obtain a wide bandwidth while maintaining low power consumption. In addition, a medium gain is sufficient for a typical modulator driver (an overall ~20 dB gain in this design), and a three-stage stage predriver is suitable to meet the required gain specification. It should be emphasized that the proposed nested feedback configuration allows combining the predriver and the main driver to increase the loop gain by connecting the second active feedback loop to the node between the CS and CG stages in the main driver.

An intuitive way to explain the function of the active feedback loops is that the feedback stage acts as the transconductance converter to the sample and then injects an opposite, delayed, and scaled version of the current to the specific node [23] for adjusting the signal. As a result, the time domain

TABLE I
DESIGN PARAMETERS AND BIAS OF THE MODULATOR DRIVER

M_{1A}/M_{1B}	30μm	R_{1A}/R_{1B}	90Ω
M_{2A}/M_{2B}	50μm	R_{2A}/R_{2B}	70Ω
M_{3A}/M_{3B}	120μm	R_{3A}/R_{3B}	65Ω
M_{4A}/M_{4B}	360μm	R_{4A}/R_{4B}	50Ω
M_{5A}/M_{5B}	200μm	R_{dege_1}/R_{dege_2}	75Ω/75Ω
M_{F1A}/M_{F1B}	25μm	C_{dege_1}/C_{dege_2}	220fF/220fF
M_{F2A}/M_{F2B}	30μm	I_1/I_2	8.5mA/16.5mA
I_3/I_4	25mA/83mA	I_{eq1}/I_{eq2}	4mA/12mA
V_{DD1}/V_{DD2}	2.2V/2.2V	V_{DD3}/V_{DD4}	2.2V/5V

response can be optimized with a proper feedback network design. Note that G_{m1}, G_{m2}, and G_{m3} are designed to obtain a current ratio of ∼1:2:3 to provide a sufficient driving capability for the predriver. The main driver has a bias current level of ∼80 mA with an effective load of 25 Ω to achieve a maximum 4 V_{ppd} differential output. The design of the loop gain and *RC* degeneration in the two feedback loops are determined based on an analytical analysis together with the simulated transient response. The detailed design parameters and bias conditions are listed in Table I.

It should be emphasized that active feedback is an effective technique that can be used for bandwidth extension in broadband amplifier design. The conventional second-order active feedback is widely adopted for the receiver in optical communications [24]. The gain-bandwidth product (GBP) can be increased significantly, even exceeding the f_T of the transistor. The third-order active feedback was also used for bandwidth enhancement [25]. One major issue for the higher-order feedback is the severe gain peaking compared with the second-order design. The interleave active feedback topology was proposed to alleviate the over-peaking problem while achieving bandwidth extension simultaneously, which can be decomposed into two third-order feedback loops with different loop gains [26]. The overall frequency response is a multiplication of the two different gain profiles, and a relatively flat gain over a wide frequency range can be achieved. A high-performance 10 Gb/s limiting amplifier (LA) has been reported based on this technique with detailed analysis [26]. The nested active feedback is a modified version of the third-order feedback topology, which introduces an additional feedback cell inside the third-order feedback loop that can also alleviate the over-peaking issue and improve stability [27]. Note that identical stages are employed to build the amplifier with a relatively small output signal swing in most of the previous studies. Based on the concept of interleaving active feedback, we propose the IFVF topology for high swing and broadband modulator driver design. Different from previously reported topologies, the nonidentical gain and feedback cells are used to overcome the heavy capacitive loading issue to obtain a large output swing. Also, a novel idea using the active frequency variant feedback with the *RC* degeneration is proposed, which can create additional poles for overshoot suppression and stability enhancement while maintaining a wide bandwidth and achieving high linearity. To the best of the authors' knowledge, using the interleave active feedback topology with different cell sizes and *RC* degeneration for broadband large-signal modulator driver design has never been reported before.

B. Transfer Function

According to Fig. 3(a), the transfer function of the proposed modulator driver can be derived as

$$H_1(s) = \frac{v_x}{v_{\text{in}}} = \frac{G_1(s)}{1 - \frac{G_{f1}(s)G_2(s)G_3(s)}{1-G_{f2}(s)G_3(s)G_4(s)}} \tag{2}$$

$$H_2(s) = \frac{v_y}{v_x} = \frac{G_2(s)}{1 - G_{f2}(s)G_3(s)G_4(s)} \tag{3}$$

$$H_3(s) = \frac{v_z}{v_y} = G_3(s) \tag{4}$$

$$H_4(s) = \frac{v_w}{v_z} = G_4(s) \tag{5}$$

$$H_5(s) = \frac{v_{\text{out}}}{v_w} = G_5(s) \tag{6}$$

$$H_{\text{total}}(s) = \frac{v_{\text{out}}}{v_{\text{in}}} = \prod_{i=1}^{5} H_i(s) = \frac{G_1(s)G_2(s)G_3(s)G_4(s)G_5(s)}{1 - G_{f1}(s)G_2(s)G_3(s) - G_{f2}(s)G_3(s)G_4(s)} \tag{7}$$

where $G_1(s)$ to $G_4(s)$ present the voltage gain of the gain cells 1–4, respectively, $G_5(s)$ is the voltage gain of the TIA, and $G_{f1}(s)$ and $G_{f2}(s)$ are the voltage gains of the two active feedback cells, respectively. Note that the voltage gain is used for the TIA to simplify the expression. With the concept of superposition, the overall loop gain becomes $G_{f1}(s)G_2(s)G_3(s) + G_{f2}(s)G_3(s)G_4(s)$ contributed from both active feedback loops for bandwidth extension.

The transfer function is derived by dividing the circuit into several blocks along the signal path. $H_1(s)$ takes the loading of the two active feedback loops into account, as can be seen from G_{f1}(s) and $G_{f2}(s)$ in the denominator of the transfer function, while $H_2(s)$ includes the second loop via $G_{f2}(s)$. $H_3(s)$ and $H_4(s)$ are relatively simple since the feedback paths of V_z and V_w are connected to the transistor gate directly with a negligible loading effect. It can be observed from the derived transfer functions that the first and second stages are the de-emphasis stages, while the following stages are for amplification. As shown in $H_1(s)$ and $H_2(s)$, the denominator terms are always larger than one due to the inverted gain stages and negative feedback. In practical design, the low-frequency gain is reduced by the first two stages and the active feedback, as indicated in (2) and (3). The rest of the gain stages are then designed to boost the gain to achieve a flat frequency response. Based on the actual final design, as shown in Fig. 3(b), Fig. 4 plots the simulated transfer function at different stages to demonstrate the points described above. As shown in Fig. 4, the gain is suppressed significantly at low frequencies with over peaking at high frequencies if considering v_y/v_{in} with the first two stages and active feedback. With the following

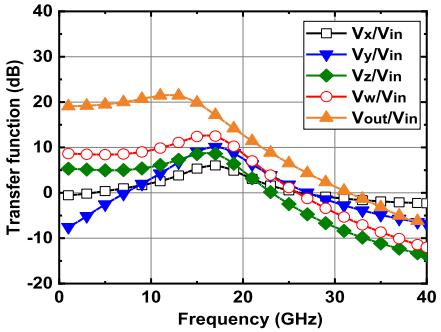

Fig. 4. Transfer functions at different nodes in the proposed modulator driver.

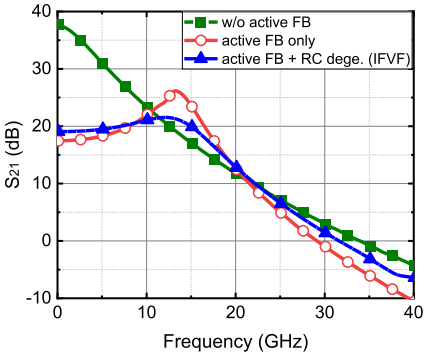

Fig. 5. Comparison of the simulated frequency responses of the modulator driver in different design cases.

stages, the low-frequency gain increases gradually, and finally, the desired transfer function with a relatively flat gain response can be achieved.

Fig. 5 compares the simulated frequency response of the modulator driver based on the actual circuits. The cascaded design without the active feedback shows a relatively small bandwidth. With the active feedback added, an obvious bandwidth extension and also overpeaking characteristic can be observed. With a fundamental second-order active feedback, it can be proved that the bandwidth can be increased by 1.55× if the damping factor of the transfer function is designed as 0.707 [18]. In the proposed nested third-order design, a higher loop gain (∼20 dB) can be achieved, resulting in a significant bandwidth extension. One issue of using the active feedback design is the overpeaking, especially with higher-order active feedback loops. By adding *RC* degeneration to the feedback loop (IFVF), the overpeaking issue can be alleviated effectively, as can be seen in Fig. 5. More details of the corresponding time-domain response will be discussed in Section III-E.

C. Pole-Zero Analysis in Active Feedback With RC Degeneration

As mentioned previously, active feedback can cause issues of overpeaking and instability. As a result, overshoot and ringing become serious in the waveform. Based on the interleave active feedback topology, the proposed IFVF technique introduces the concept of using *RC* degeneration in the active feedback cell to solve the problems. Creating an additional zero by *RC* in the feedback stage can result in a very different characteristic for the overall circuit. From an alternative point of view, the transfer function is constructed based on a general pole-zero analysis with a simplified assumption that the core amplifier has three major individual poles of $p_3 > p_2 > p_1$. In practical design, p_1 is corresponding to the input of the main driver (v_z), p_2 can be referred to as the node between the CG and CS stages of the main driver (v_w), and p_3 results from the input of the third stage (v_y). The closed-loop form of the simplified transfer function can be expressed as

$$A_f = \frac{\frac{A_o}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)}}{1+\frac{A_o\beta\left(1+\frac{s}{z_1}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)}} \tag{8}$$

where A_0 is the low-frequency gain of the intrinsic amplifier, and β is the feedback coefficient. As can be seen, an additional zero is included owing to the *RC* degeneration in the active feedback. Note that the effect of two feedback loops is simplified to only one β-related term since one of the active feedback loops dominates in practical design. Equation (8) can be rearranged to be (9), as shown below

$$A_f = \frac{A_o}{\left(1+\frac{s}{z_1}\right)\left[\frac{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)}{\left(1+\frac{s}{z_1}\right)}+A_o\beta\right]}. \tag{9}$$

Assuming z_1 is chosen to be close to p_3 and can compensate with each other, (9) can be further simplified as

$$A_f \approx \frac{A_o}{\left(1+\frac{s}{z_1}\right)\left[\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)+A_o\beta\right]}. \tag{10}$$

With a properly arranged z_1, the zero introduced by the *RC* degeneration can act as a real pole in the overall frequency response, which can effectively reduce the overshoot and enhance stability. The denominator also includes a second-order polynomial term with a pair of complex conjugate poles, which can be expressed as

$$s^2+\left(\frac{\omega_o}{Q}\right)s+(\omega_o)^2 \tag{11}$$

where

$$\omega_o^2 = p_1p_2(1+A_0\beta) \tag{12}$$

$$Q = \frac{\sqrt{p_1p_2(1+A_0\beta)}}{p_1+p_2}. \tag{13}$$

If the polynomial term dominates, the time-domain characteristics, such as overshoot and ringing, will be mainly determined by the Q value here. The nonideal effect becomes more serious if Q is too large. In the actual design, the time-domain characteristics are affected by both types of poles simultaneously. Based on (8) and with MATLAB, the Bode plot can be used to further investigate the design principle and the impact of z_1 on circuit characteristics. Note that the low-frequency loop gain $A_0\beta$ used in the simulation is 20 dB, where $A_0 = 40$ dB, $\beta = -20$ dB. Also, the poles in the transfer functions are estimated based on the actual final design by fitting the frequency response. Fig. 6(a) and (b) shows the

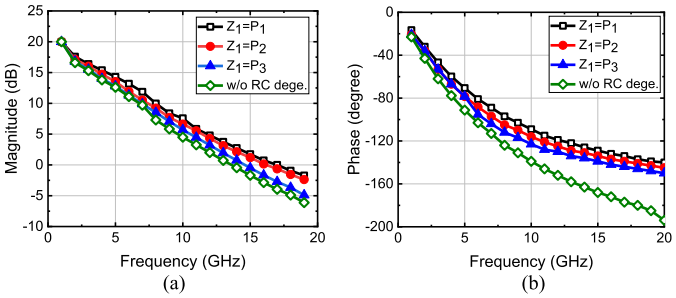

Fig. 6. Calculated Bode plots of the loop gain based on the simplified transfer function. (a) Magnitude. (b) Phase.

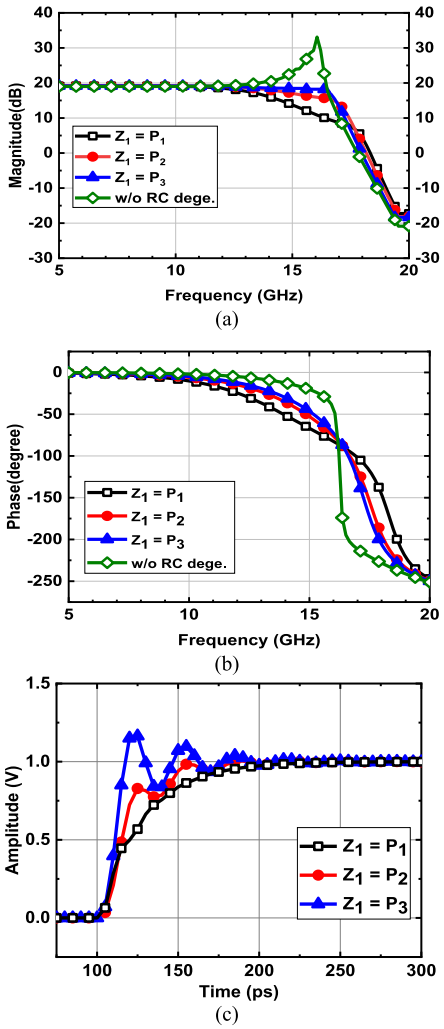

Fig. 7. Calculated Bode plots of the modulator drivers based on the simplified transfer function. (a) Magnitude. (b) Phase. (c) Time domain step response with different locations of z_1.

simulated loop gain for the magnitude and phase, respectively, in the cases with (z_1 placed at p_1, p_2, p_3, respectively) and without *RC* degeneration. An obvious phase reduction can be observed with the *RC* degeneration added to the active feedback loop, which effectively enhances the circuit stability.

Fig. 7(a) and (b) presents the corresponding close-looped frequency response of the modulator driver, and the desired frequency response can be obtained as z_1 is placed at p_3.

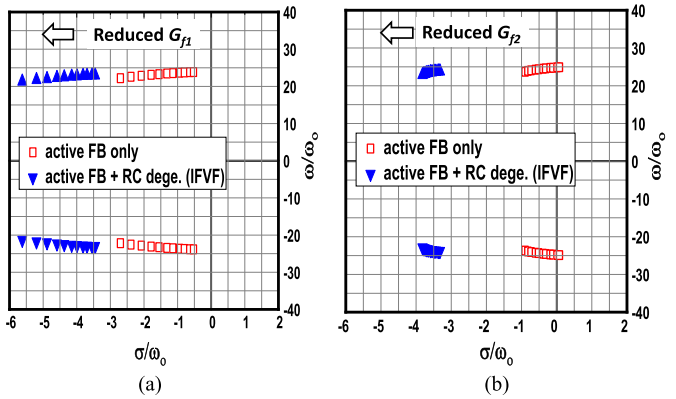

Fig. 8. Comparison of simulated pole-zero plots of the modulator driver w/i and w/o IFVF by sweeping the voltage gain of the two active feedback cells. (a) G_{f1} and (b) G_{f2}, respectively.

It should be emphasized that overpeaking could occur without adding the *RC* degeneration in the active feedback network, as illustrated in Fig. 7(a), which is consistent with the results of the simulated loop gain, as shown in Fig. 6. In addition, the phase change becomes less abrupt with z_1 created by the *RC* degeneration, which is consistent with the relatively flat gain observed in the magnitude plot. Fig. 7(c) plots the corresponding time-domain response with a step input also based on (8) as the output voltage normalized to 1 V. The curves show that the improved rise time with a reasonable ringing can be obtained as z_1 is placed at p_3, which also agrees well with the Bode plots. Although the ringing seems to be relatively high among the three cases, it is still much improved compared to that without using the IFVF technique (see Fig. 10). Also note that the case without *RC* degeneration cannot converge in the step response and is not included in Fig. 7(c). In practical design, the simulation tool was employed rigorously to investigate the optimal values of *RC* degeneration in the feedback loop, mainly based on the overall time-domain characteristics of the modulator driver.

D. Loop Gain and Linearity

The active feedback IFVF topology has two critical design parameters, namely, the *RC* degeneration and the gain of the feedback loop. Based on the actual circuit, Fig. 8(a) and (b) shows the simulated pole-zero plots by sweeping the voltage gain of the two active feedback cells G_{f1} and G_{f2}, respectively, to evaluate the stability as a function of loop gain. Note that the loop gain is changed by adjusting the current sources I_{FV1} and I_{FV2} of FV-G_m. Also, only a pair of dominant complex conjugate poles are shown in Fig. 8(a) and (b) of each case to simplify the analysis.

First, as shown in Fig. 8(a), the complex conjugate poles move towards the more negative end along the x-axis with a reduced loop gain G_{f1} (*RC* is fixed), which indicates improved stability. More importantly, the locations of the complex conjugate poles move substantially towards the left-hand side with the *RC* degeneration in the active feedback. The results indicate that the modulator driver becomes more stable and could alleviate the overshoot and ringing effect in the

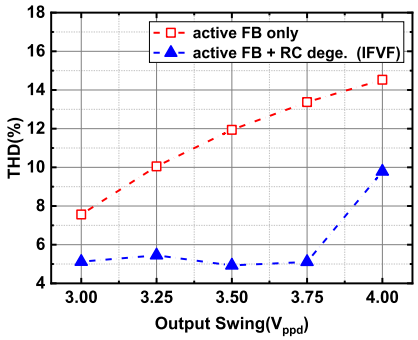

Fig. 9. Simulated THD with a 1-GHz 500 mV_{ppd} sinusoidal input signal as a function of the output swing. The increased output level is achieved by reducing the feedback factor of the active feedback loop using the current sources.

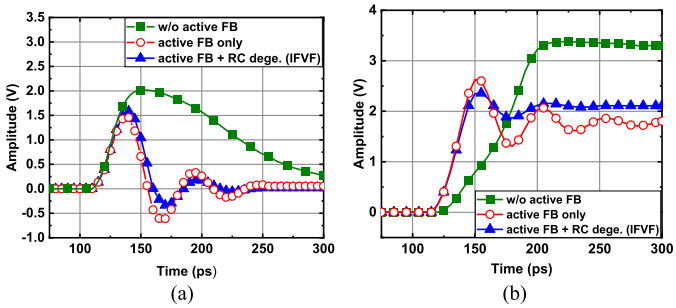

Fig. 10. Simulated results of different input waveforms. (a) Pulse (500 mV_{ppd} and 25 ps) and (b) step response.

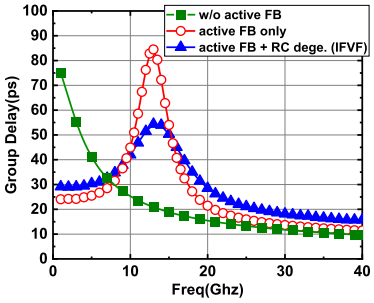

Fig. 11. Comparison of the simulated group delay of the proposed modulator driver.

waveform, which is consistent with our previous analysis. Fig. 8(b) shows a similar plot for G_{f2}, where the locations of poles are relatively insensitive to the change of loop gain. Note that although the voltage level at v_w is relatively high, the CS stage in the cascode topology is with a low voltage gain, and G_4 becomes much lower than G_2. As a result, the first loop gain $G_{f1}G_2G_3$ is much higher than the second loop gain $G_{f2}G_3G_4$ ($G_{f1} \approx G_{f2}$); therefore, the circuit is less sensitive to G_{f2}. The difference is, however, still significant if the IFVF technique is applied. In the actual design, the circuit characteristics are mainly optimized by the first active feedback loop due to the sensitivity to the loop gain, which is also consistent with our assumption in deriving the pole-zero transfer function of (8). Note that the complex conjugate poles in the final design are close to $\sigma/\omega_0 = -4.5$ and $\omega/\omega_0 = \pm 22.5$ where $\omega_0 = 1$ GHz, as included in Fig. 8.

The linearity of the modulator driver is also a critical issue, especially for the PAM4 signaling. Based on the actual design, Fig. 9 compares the simulated total harmonic distortion (THD) without and with the proposed IFVF as a function of the output swing. To evaluate the impact of IFVF on circuit linearity, the increased output level is achieved by reducing the feedback factor with the current sources of the active feedback loops while the input signal level is kept at 500 mV_{PPd} at 1 GHz. As shown in Fig. 9, the THD can be suppressed effectively at a high output swing using the proposed IFVF with the *RC* degeneration applied in the active feedback loop. The improved THD is beneficial to maintain equal spacing among different signal levels in the PAM4 signal format.

E. Pulse/Step Response and Eye-Diagram

An ideal pulse with 500 mV_{ppd} and 25 ps (40 Gb/s) pulsewidth is applied at the input of the actual modulator driver to evaluate the bandwidth limitation and residual signal tail, as shown in Fig. 10(a), which is consistent with the frequency response shown in Fig. 5. By removing the active feedback loop, we can obtain the curve "w/o active FB." With the active feedback loop but simply removing the *RC* degeneration elements, we can obtain the curve "active FB loop only." For the optimal result, "active FB loop + *RC* degeneration (IFVF)," the zero is placed between p_2 and p_3 by optimizing the step response in the actual design. Note that the zero introduced by the *RC* degeneration is not exactly placed at p_3 as we analyzed by MATLAB, which is a conceptual explanation.

First, a very long tail can be observed if the active feedback loops are removed in the driver, which is similar to the waveform illustrated in Fig. 2. By using the interleave active feedback, the signal tail can be reduced significantly; however, the signal tail issue can be further improved by the proposed IFVF to reach a better damping characteristic. As can be seen, the post cursor is reduced, which will lead to an increased minimum vertical eye-opening [28]. Fig. 10(b) compares the simulated step response of the modulator driver, which can emulate the transition among different voltage levels in the PAM4 signal format. Here, we use the transition from 00 to 10 as an example ($V_{in} = 333$ mV_{ppd}). A very slow response can be observed without using the active feedback loops in the driver. In contrast, the rise time (10%–90%) can be improved significantly if the active feedback loops are employed. The rise times are 37, 15, and 20.6 ps for without any feedback, and without and with IFVF, respectively. Although the proposed design technique increases the rise time slightly, the issues of overshoot and settling time are alleviated significantly, resulting in much improved PAM4 signal integrity. Fig. 11 compares the group delay. The results indicate the effectiveness of using the *RC* degeneration in the active feedback loop to reduce the group delay variation.

The simulated NRZ and PAM4 eye diagrams are shown in Figs. 12 and 13, respectively. As can be seen, serious data-dependent jitter is induced in the case without using the proposed IFVF technique, which is consistent with that

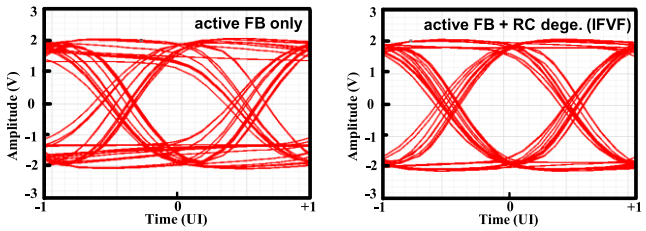

Fig. 12. Simulated 40 Gb/s NRZ eye diagrams. (a) Active feedback only and (b) active feedback w/i *RC* degeneration in the active feedback loops.

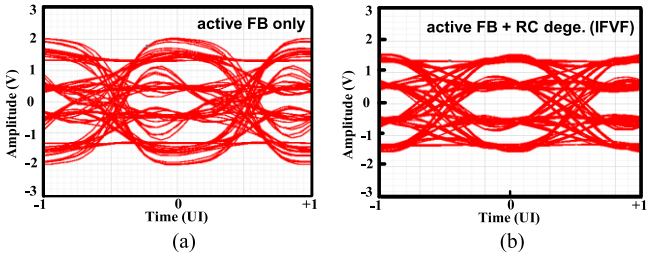

Fig. 13. Simulated result of 20 Gbauds PAM-4 signals. (a) Active feedback only and (b) active feedback w/i *RC* degeneration in the active feedback loops.

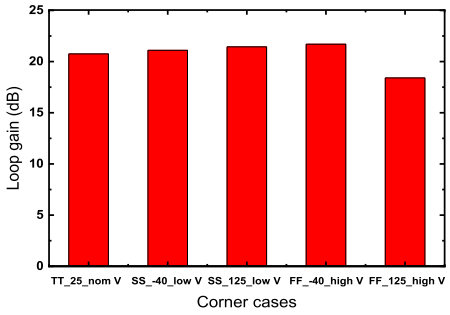

Fig. 14. Simulated loop gain of the proposed IFVF modulator driver in different corner cases.

observed obtained in Fig. 10(a). In addition, as multilevel signaling is applied, such as PAM4 with a reduced SNR [29], the overshoot becomes a much more serious issue. For example, the overshoot could exceed half of the eye interval, as shown in Fig. 13(a). In contrast, the overshoot issue can be alleviated significantly with the proposed IFVF technique, resulting in a clear eye diagram and improved signal integrity, as shown in Fig. 13(b). Note that this agrees well with the simulated step response in Fig. 10(b).

One issue with the active feedback is that the circuit could be more sensitive to the process, voltage, temperature (PVT) variation, which is dominated by the loop gain. Fig. 14 shows the simulated loop gain $G_{f1}(s)G_2(s)G_3(s) + G_{f2}(s)G_3(s)G_4(s)$ including some worst cases based on the actual circuit. As can be seen, the typical case (TT, 25 °C, nominal V) shows a gain of 20.7 dB, and the gain changes within a relatively small range between 21.1 and 21.7 dB for the other three corner cases (SS, −40 °C, low V; SS, 125 °C, low V; FF, −40 °C, high V). On the other hand, a more obvious change to 18.4 dB can be observed for the last corner case

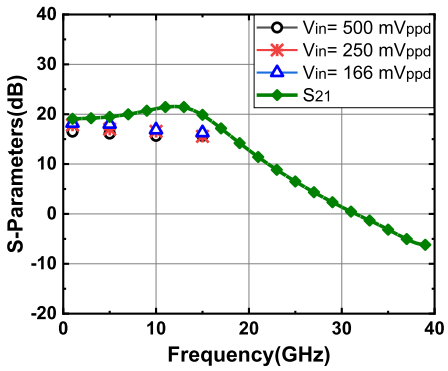

Fig. 15. Comparison of the simulated frequency response of the IFVF modulator driver under different input swing levels with S_{21}.

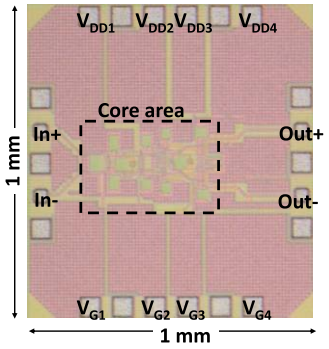

Fig. 16. Micrograph of the proposed IFVF modulator driver in 90-nm CMOS.

(FF, 125 °C, high V). In practical design, this can be fixed by adjusting the bias current in the active feedback loop.

Also, one important consideration for the previous small-signal pole-zero analysis is if this is suitable for the large-signal modulator driver. Fig. 15 shows the simulated large-signal transient gain to verify this point using a single-tone sinewave at several frequencies. With three different voltage levels (corresponding to 1/3, 1/2, and the full swing of the output signal), the result indicates that the gain is very consistent in a wide input signal range, and agrees very well with the S-parameters at low frequencies. Note that the gain also becomes relatively flat at high frequencies compared with that obtained in the S-parameters. With the consistency between the small-signal and large-signal characteristics, the pole-zero analysis should be able to reasonably predict the circuit stability under the large-signal operating condition.

IV. Measured Results and Discussion

The proposed inductorless IFVF modulator driver has been implemented in a 90-nm CMOS technology, which occupies a core area of only 0.092 mm^2 (227 × 405 μm), as shown in Fig. 16. The differential S-parameters were measured on-wafer with the RF probes by a four-port network analyzer (Keysight N5247A) under a total power consumption of 560 mW from 0.1 to 40 GHz. Fig. 17 compares the simulated and measured S-parameters, which show an excellent agreement over a wide frequency range. The modulator achieves a high gain of ∼18 dB and a 3-dB bandwidth close to 16 GHz with

TABLE II
PERFORMANCE SUMMARY OF MODULATOR DRIVER AND COMPARISON WITH PRIOR WORKS

Spec.	[7] JSSC 2020	[12] JSSC 2019	[32] TVLSI 2014	[33] TMTT 2017	[34] RFIC 2019	[35] TCAS-II 2016	This Work
Tech.	130 nm BiCMOS	45 nm RFSOI	130 nm	130 nm BiCMOS	40 nm	65 nm	90 nm
f_T (GHz)	250	290	90	300	270	160	120
Signal format	NRZ/PAM4/PAM8	PAM4/NRZ	NRZ	NRZ/PAM4	NRZ	NRZ	NRZ/PAM4
Inductor	YES	YES	YES	YES	YES	NO	NO
Output Bias-Tee	NO	NO	YES	NO	NO	YES	NO
Linear	YES	YES	NO	YES	NO	NO	YES
Max. Data Rate (Gb/s)	138	112	20	90	28	20	40
Max. Swing (V_{ppd})	6	5.2	7	4	4	5	3.4
P_{DC} (mW)	1000	890	900	550	585	534	560
Core area (mm^2)	0.33+	0.31	0.72	0.476+	0.25	0.068	0.092
Norm. area (mm^2)	0.16	1.24	0.345	0.228	1.265	0.13	0.092
Power eff. (mW/Gbps)	7.24	7.95	45	6.11	20.9	26.7	14
FOM[1]	0.55	0.43	0.25	0.55	0.18	0.23	0.6
FOM[2]	3.43	0.35	0.72	2.4	0.14	1.8	6.5
FOM[3]	20.58	1.75	5.01	9.64	0.56	9	22.1

+Estimated by chip photo; FoM[1] = 1000· max. data rate/(P_{DC}·f_T); FoM[2] = 1000· max. data rate/(P_{DC}·f_T· norm. area);
FoM[3] = 1000· max. data rate · max. swing/(P_{DC}·f_T· norm. area); normalized area = Core area · (90 nm / Tech.)^2

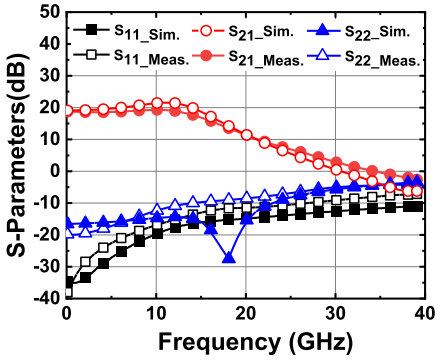

Fig. 17. Simulated and measured results of differential S-parameters of the proposed inductorless modulator driver.

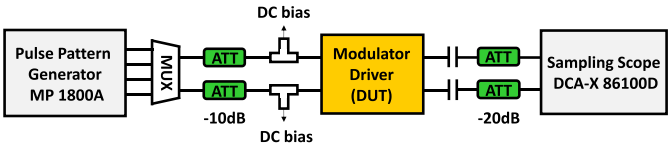

Fig. 18. PAM4 measurement setup for the modulator driver.

a flat S_{21} response. The measured reflection coefficients S_{11} and S_{22} are both below −10 dB within the 3-dB frequency. The transient response was measured using a pattern generator Anritsu MP1800A and a sampling scope Keysight 86100D. Fig. 18 shows the block diagram for the PAM4 measurement setup. After the MUX and 10-dB attenuators, a maximum input differential swing of 500 mV_{ppd} can be obtained at the input of the modulator driver. The bias-Tee is only used to provide the gate bias of the input stage M_{1A}/M_{1B} due to the on-chip dc bias pad limitation, and no bias-Tee is used at the output. The dc blocks at the output and the 20-dB attenuators are connected to protect the sampling scope. Note that the pattern generator has a maximum data rate of 32 Gb/s.

Fig. 19(a)–(d) shows the measured NRZ electrical eye diagram of the modulator driver with a differential output at 10, 20, 25, and 32 Gb/s, respectively. Fig. 20(a)–(d) shows the measured PAM4 signal eye diagrams with the data rates of 5, 10, 15, and 20 Gbaud, respectively. As can be seen, clear eye diagrams are obtained with equally distributed levels. The measured PAM4 signal demonstrates excellent linearity with an R_{LM} ratio over 92%, where the ratio level mismatch (RLM) is defined as [30], [31]

$$\mathrm{RLM} = 3 \cdot \frac{V_{\min}}{V_{\mathrm{pk-pk}}}. \tag{14}$$

Table II shows a comparison with the prior works of the modulator drivers in different technologies. Without using any inductive components, the proposed modulator driver using the IFVF technique demonstrates high-speed operation with a large output swing and only consumes a very small chip

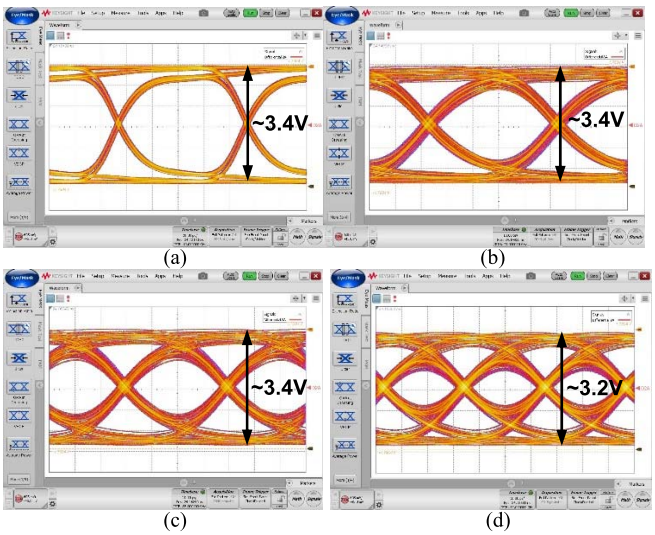

Fig. 19. Measured results of NRZ eye diagram. (a) 10, (b) 20, (c) 25, and (d) 32 Gb/s.

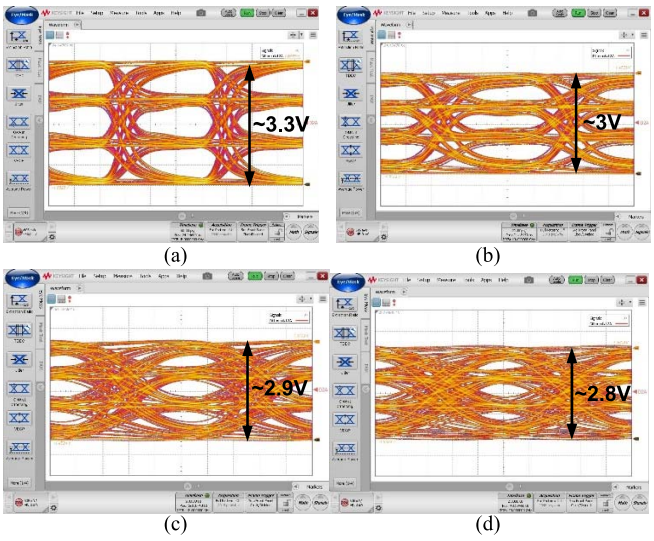

Fig. 20. Measured result of PAM4 eye diagram. (a) 5, (b) 10, (c) 15, and (d) 20 Gbaud.

area. The obtained figure-of-merits (FoMs) are among the best compared with prior published results. Note that FoM^1 is based on [36] for DAs, but here the GBP is replaced by the data rate to evaluate the modulator driver. On the other hand, FoM^2 also includes the normalized chip area to the different technology nodes, which is based on [35] to emphasize the area efficiency. Based on FoM^2, FoM^3 also considers the maximum output swing, which is an important index for the modulator driver.

V. Conclusion

A high-speed inductorless modulator driver in 90-nm CMOS has been demonstrated. Using the proposed IFVF technique, the two active feedback loops with the *RC* degeneration can add desired poles in the transfer function and effectively suppress overshoot and ringing in the waveform. The experiential results showed clear eye diagrams for NRZ and PAM4 signal formats obtained up to 32 Gb/s and 20 Gbaud, respectively. Without using any inductive components, a very compact design can be achieved with a core area of only 0.092 mm^2.

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