

# Square-Gate AlGaN/GaN HEMTs With Improved Trap-Related Characteristics

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**Abstract**—In this brief, the trap-related characteristics of high-breakdown AlGaN/GaN high-electron-mobility transistors (HEMTs) were investigated. Compared with a conventional multifinger layout, the square-gate design presented reduced the current collapse from 19% to 6% and almost eliminated the gate lag. The flicker noise density and the gate leakage decreased from  $1.16 \times 10^{-10}$  to  $1.17 \times 10^{-11}$  1/Hz ( $f = 100$  Hz) and from  $7.36 \times 10^{-5}$  to  $1.80 \times 10^{-6}$  A/mm ( $V_{GS} = -4$  V and  $V_{DS} = 100$  V), respectively. The breakdown voltage was also improved from 350 to 650 V. With the channel area away from the defects generated by the mesa etching process, the square-gate AlGaN/GaN HEMTs demonstrated excellent performance with much less trapping effects.

**Index Terms**—High-electron-mobility transistor (HEMT), layout, power semiconductor devices.

## I. INTRODUCTION

HIGH-PERFORMANCE AlGaN/GaN high-electron-mobility transistors (HEMTs) have been successfully demonstrated for high-power applications owing to the excellent material properties of GaN [1], [2]. However, the degradation and reliability problems of GaN HEMTs, caused by the trap-related effects, have been a critical issue that is widely discussed in recent years [3]–[6]. These defects may result from surface states, dislocations in the buffer layer, and plasma etch damage [7]–[11], which act as trapping–detraping centers to affect device characteristics. The well-known phenomena are the current collapse [3], [4], [6], and gate-lag effects [3], [5], [6], which degrade the device transconductance and current density. The traps existing in the transistor were also reported to be closely related to the flicker noise characteristics [12], [13]. In addition, the defect charges around the gate finger not only cause barrier narrowing in the AlGaN cap layer, leading to increased gate leakage current [14], but also bring out a higher electric field density at the gate

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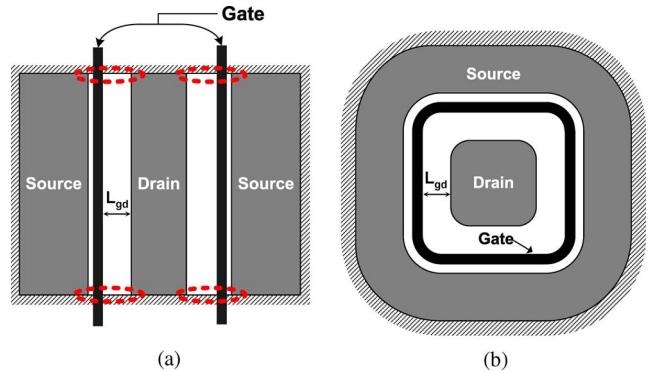


Fig. 1. AlGaN/GaN HEMTs: (a) Two-finger and (b) square-gate layouts.

electrode edge, resulting in enhanced impact ionization and reduced breakdown voltage.

Many previous studies of GaN HEMTs focused on the origins of the surface states and technologies, such as various passivation methods and surface treatments, for trapping effect reduction [5], [15]–[22]. Excellent results for the transistors with small current collapse have been reported [14]–[19], [21], [22]. However, these works only investigated typical multifinger configurations with a small gate-to-drain distance  $L_{gd}$  (typically, 1–3  $\mu\text{m}$ ), which were not suitable for applications up to several hundred volts. In this study, we found that the trapping effect is severe for conventional multifinger transistors with a large  $L_{gd}$  (12  $\mu\text{m}$  in this case), even with careful passivation, because of the traps located around the RIE-etched mesa edge. Compared with GaAs, GaN has a higher bonding energy and is more chemically inert [7]. Therefore, the RIE process for GaN etching is more difficult and requires higher ion energy and plasma flux, which often generate ion-induced damages and unsmoothed sidewalls [7]. Previous studies reported that the etching process for mesa isolation in GaN-based devices produced deep level traps, causing increased leakage current [7]–[11]. In this brief, the square-gate layout approach is proposed to reduce the effects of traps at the mesa edge on the transistor characteristics. The trap-related characteristics such as current collapse, gate lag, flicker noise, gate leakage, and breakdown voltage are investigated to verify this viewpoint. The square-gate GaN HEMTs were reported, and an excellent breakdown voltage up to 8300 V was achieved [2]. However, the advantage of improved trap-related characteristics of using the square-gate design has not been discussed, which is the main scope of this study.

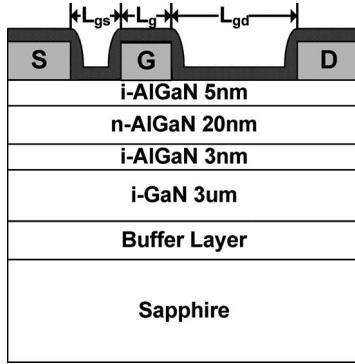


Fig. 2. Layer structure of the AlGaN/GaN HEMTs.

## II. DEVICE DESIGN AND FABRICATION

Fig. 1 shows the layouts of both the two-finger device and the square-gate topology. The mesa edges are highlighted by diagonal strips in both layouts. For the two-finger design in Fig. 1(a), the gate fingers are extended beyond the mesa edge to ensure that the channel is fully depleted under the OFF state, and the boundary of the channel is defined by the mesa. Note that the mesa process is essential for electrical isolation of individual transistors. With the identical layer structure and process steps, the reduced trapping effects, as will be carried out later, can mainly be ascribed to the square-gate design with eliminated mesa edge effect. As indicated in Fig. 1(b), the critical channel area (between the source and the drain) is fully surrounded by the source region rather than that exposed to the mesa edge [encircled by the dotted line, see Fig. 1(a)] in the conventional two-finger layout.

The cross section of the modulation-doped AlGaN/GaN heterostructure is shown in Fig. 2. The device structure was grown on a c-plane sapphire substrate by metal-organic chemical vapor deposition. The epitaxial structure consisted of a GaN buffer layer, a 3- $\mu$ m undoped GaN layer, a 3-nm undoped AlGaN layer, a 20-nm n-doped AlGaN barrier layer, and, finally, a 5-nm undoped AlGaN cap layer. The Al mole fraction in the AlGaN layer was 0.25. Device isolation was achieved by dry etching using a Cl<sub>2</sub>/Ar gas mixture, and a silicon nitride layer, 1.2  $\mu$ m thick, was deposited for surface passivation. It is worth mentioning that the etching process and surface passivation were carefully optimized for the current collapse effect. Using a similar process, the maximum drain current reduction was recovered from 37.5% to only 6.9% for the Cl<sub>2</sub>/Ar-recessed GaN HEMTs ( $L_{gd} = 2 \mu\text{m}$ ) [22].

In this study, the gate length  $L_g$  and the gate-to-source spacing  $L_{gs}$  are both 2  $\mu\text{m}$  for the two designs, while a large gate-to-drain spacing  $L_{gd}$  of 12  $\mu\text{m}$  is used as the drift extension region. The overall channel widths of both devices are 400  $\mu\text{m}$ . Fig. 3 compares the typical  $I_D$ - $V_{DS}$  characteristics of the two designs. As can be seen, the curves are almost identical, and well-defined pinchoff characteristics can be observed. The typical threshold voltage  $V_{th}$  is  $\sim -4 \text{ V}$ . The maximum current density and transconductance are  $\sim 250 \text{ mA/mm}$  ( $V_{GS} = 1 \text{ V}$ ,  $V_{DS} = 10 \text{ V}$ ) and  $\sim 75 \text{ mS/mm}$  ( $V_{GS} = -1 \text{ V}$ ,  $V_{DS} = 10 \text{ V}$ ), respectively. It should be mentioned that the gate electrode in the square-gate design can be connected in a repeatable manner by

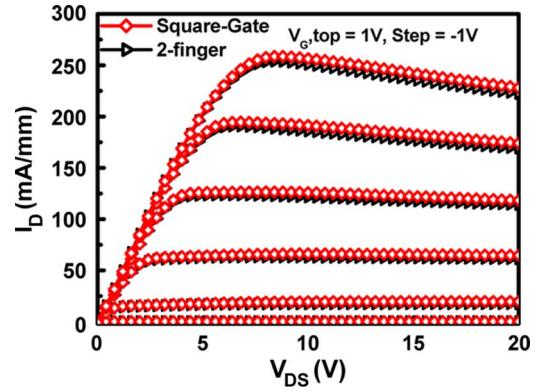


Fig. 3. Measured  $I_D$ - $V_{DS}$  characteristics for both two-finger and square-gate devices.

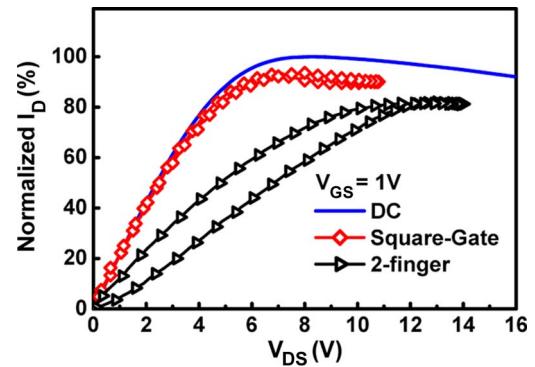


Fig. 4. Current collapse characteristics for both two-finger and square-gate devices.

a Ti/Au top metal layer above the SiN passivation layer through a via hole. In this way, a multifinger transistor can be realized for high-power applications.

## III. RESULTS AND DISCUSSION

The current collapse measurement of the device was performed under the sweep of a 60-Hz rectified sine wave using a Tektronix 370 curve tracer. Note that the drain voltage is supplied as a rectified sine wave of 60 Hz, while a pulse signal is applied to the gate with a duration of 250  $\mu\text{s}$ , which is suitable for observing the collapse effect [22], [23]. The current collapse effect in GaN-based devices has been investigated, which can be explained by the electron injection into the surface states [24]–[26]. With the surface states existing between the gate and drain area, the captured electrons in the slow traps cannot respond fast enough to the applied pulse signal. The trapped electrons induce a negative voltage to deplete the channel, causing a reduced drain current. Therefore, the current collapse effect closely depends on the trap density and can be used to test the traps in a transistor.

The impact of the trapping effects can be observed by comparing the dc  $I$ - $V$  characteristics (measured by an Agilent semiconductor analyzer) with the swept signal as shown in Fig. 4 ( $V_{GS} = 1 \text{ V}$ ). As can be seen, the traditional two-finger device shows a clear degradation when compared with the dc results, whereas the square-gate design has a much less current collapse effect. The hysteresis characteristic observed in the

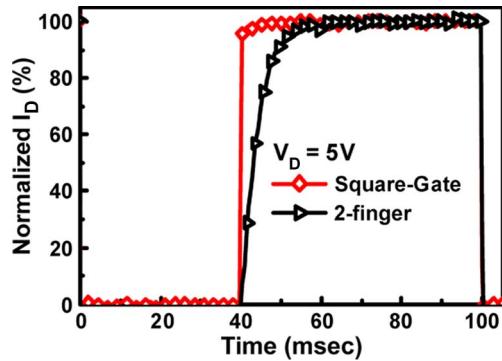


Fig. 5. Measured gate-lag characteristics for both two-finger and square-gate devices.

two-finger device also indicates that the trapped carriers have very large time constants. The current collapse factor  $\Delta I_{\max}$ , defined as  $(I_{\text{dc\_peak}} - I_{\text{ac\_peak}})/I_{\text{dc\_peak}}$  at  $V_{\text{GS}} = 1$  V, was reduced from  $\sim 19\%$  to only  $\sim 6\%$  for the square-gate design, where  $I_{\text{dc\_peak}}$  is the maximum dc drain current within the applied drain voltage range and  $I_{\text{ac\_peak}}$  has a similar definition but with the swept ac signal. The results suggest that a severely damaged mesa edge may not be fully recovered even when carefully passivated by SiN. For the two-finger design, the remaining traps along the mesa edge are in the vicinity of the active area, which can still affect the channel carriers. This may not be obvious for devices with a small  $L_{\text{gd}}$  (typically, 1–3  $\mu\text{m}$ ), but it becomes a dominant factor in power devices with a relatively large  $L_{\text{gd}}$ . In this case, the overall length along the sensitive channel area exposed to the mesa edge is around 48  $\mu\text{m}$  [ $4 \times 12 \mu\text{m}$  as indicated in Fig. 1(a)]. In contrast, even with large  $L_{\text{gd}}$  in the square-gate devices, the critical channel area is surrounded by the source and is far away from the mesa edge. As a result, the square-gate design presents a significantly reduced current collapse effect.

The gate-lag measurements use a pulse voltage biased from  $-5$  to  $0$  V at the gate terminal by the Agilent 8114 pulse generator [22]. The period and the duty cycle of the gate pulse voltage used were  $0.1$  s and  $60\%$ , respectively. Fig. 5 shows the results with the drain bias fixed at  $5$  V. For the two-finger device, an obvious drain current lag can be observed, where the lag is longer than  $10$  ms. On the other hand, the gate-lag effect is almost eliminated in the square-gate device. Similar to the current collapse effect, the lag of the drain current is also due to the fact that the captured electrons in the traps cannot respond fast enough to the gate pulse signal. As can be seen, the observation in the gate-lag measurements presents a consistent trend with the current collapse results. Note that the trapping effect can mainly be observed under the applied ac pulse signal, and, thus, similar dc  $I$ – $V$  characteristics and threshold voltages are obtained in both designs as shown in Fig. 3.

Fig. 6 shows the normalized flicker noise current spectral densities  $S_{\text{id}}/I^2$  of both designs ( $V_{\text{GS}} = 0$  V and  $V_{\text{DS}} = 1$  V). Compared with the traditional two-finger device, the noise level of the square-gate transistor improves about one order of magnitude from  $1.16 \times 10^{-10}$  to  $1.17 \times 10^{-11}$  1/Hz (at  $100$  Hz). The result shown in Fig. 7 is the measured OFF-state gate leakage current. The square-gate device presents a significantly

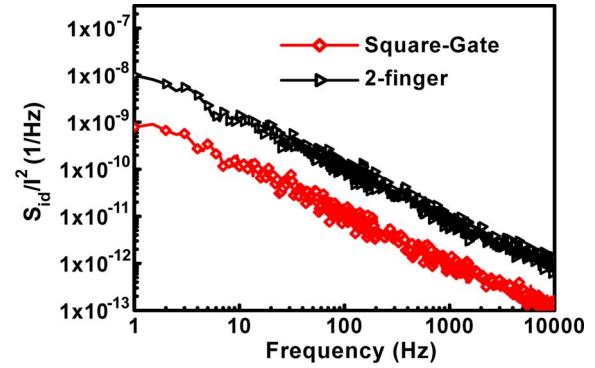


Fig. 6. Measured flicker noise characteristics for both two-finger and square-gate devices.

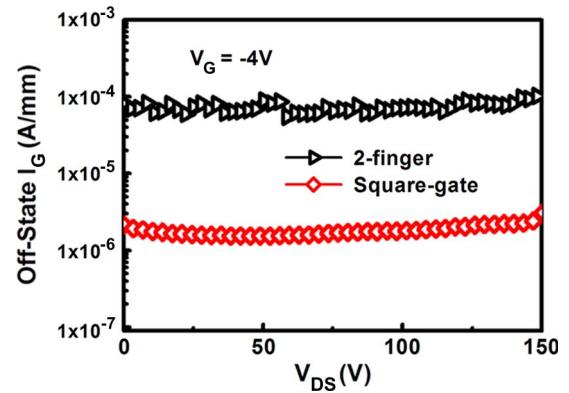


Fig. 7. Gate leakage characteristics for both two-finger and square-gate devices.

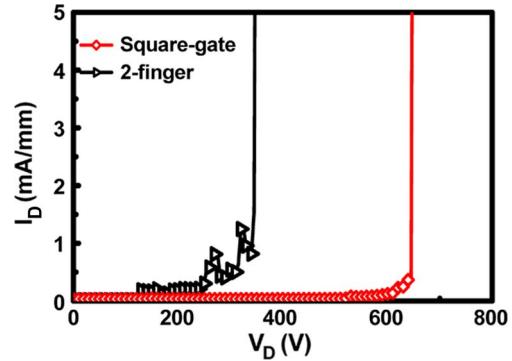


Fig. 8. Measured breakdown voltages for both two-finger and square-gate devices.

lowered leakage current by almost two orders of magnitude in the range of  $\sim 10^{-6}$  A/mm. As mentioned earlier, the flicker noise characteristic and gate leakage current level are both closely related to the defects in the transistor. The square-gate design eliminates the mesa edge trapping effect, leading to reduced flicker noise and gate leakage current.

Finally, the improved OFF-state blocking capability was also confirmed. The breakdown voltage  $V_{\text{BK}}$  of the device with the square-gate layout shown in Fig. 8 can reach  $650$  V, whereas the two-finger device can reach only about  $350$  V. The contribution of the square-gate design for the significantly enhanced breakdown characteristic could be twofold. First, the rounded

corners can reduce the high electric field at the gate finger tips in the two-finger design. In addition, the trap charges underlying the gate finger, which can lower  $V_{BK}$ , are avoided in the square-gate design. Compared with the state of the art [2], the square-gate GaN HEMTs using a field-plate (FP) structure show a  $V_{BK}$  of  $\sim 500$  V ( $L_{gd} = 10 \mu\text{m}$ ) and a  $V_{BK}$  of  $\sim 1000$  V ( $L_{gd} = 20 \mu\text{m}$ ). Our device, without the additional FP structure, has a  $V_{BK}$  of up to 650 V ( $L_{gd} = 12 \mu\text{m}$ ), which demonstrates excellent quality of the transistors studied here regarding both technology and design. All the measurement results show that the square-gate design is effective in eliminating the effects of traps associated with the mesa edge.

#### IV. CONCLUSION

In this brief, the square-gate design has been proposed to alleviate the trap-related effects associated with plasma etch damage along the mesa edge in AlGaN/GaN HEMTs. Compared with the conventional multifinger layout, the square-gate device presented a significantly improved current collapse and gate-lag effect. The flicker noise level and the OFF-state gate leakage current were both reduced by more than one order of magnitude. A much higher breakdown voltage up to 650 V was also obtained. The results suggest that the defects around the mesa edge generated by the RIE process are critical, particularly for the high-power devices with a large gate-to-drain extension distance.

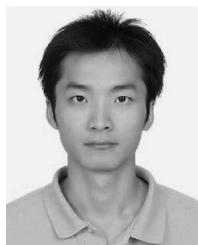
#### REFERENCES

- W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, and H. Ohashi, "High breakdown voltage AlGaN–GaN power-HEMT design and high current density switching behavior," *IEEE Trans. Electron Devices*, vol. 50, no. 12, pp. 2528–2531, Dec. 2003.
- Y. Uemoto, D. Shibata, M. Yanagihara, H. Ishida, H. Matsuo, S. Nagai, N. Batta, M. Li, T. Ueda, T. Tanaka, and D. Ueda, "8300 V blocking voltage AlGaN/GaN power HFET with thick poly-AlN passivation," in *IEDM Tech. Dig.*, Dec. 2007, pp. 861–864.
- R. Vetary, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, Mar. 2001.
- T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto, and K. Maezawa, "A study on current collapse in AlGaN/GaN HEMTs induced by bias stress," *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 37–38, Oct. 2003.
- G. Koley, V. Tilak, L. F. Eastman, M. Bianchi, and M. G. Spencer, "Slow transients observed in AlGaN/GaN HFETs: Effects of  $\text{SiN}_x$  passivation and UV illumination," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 886–893, Apr. 2003.
- G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U. K. Mishra, C. Canali, and E. Zanoni, "Surface-related drain current dispersion effects in AlGaN–GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1554–1561, Oct. 2004.
- S. J. Pearson, R. J. Shul, and F. Ren, "A review of dry etching of GaN and related materials," *MRS Internet J. Nitride Semicond. Res.*, vol. 5, no. 11, pp. 1–38, Nov. 2000.
- X. A. Cao, S. J. Pearson, G. T. Dang, A. P. Zhang, F. Ren, and J. M. Van Hove, "GaN n- and p-type Schottky diodes: Effect of dry etch damage," *IEEE Trans. Electron Devices*, vol. 47, no. 7, pp. 1320–1324, Jul. 2000.
- A. A. Syed, X. A. Cao, A. A. Woodworth, and C. D. Stinespring, "Electrical characteristics of Pt/Au Schottky contacts to plasma-etched AlGaN," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 26, no. 4, pp. 1420–1424, Jul./Aug. 2008.
- R. J. Shul, L. Zhang, A. G. Baca, C. G. Willison, J. Han, S. J. Pearson, K. P. Lee, and F. Ren, "Inductively coupled high-density plasma-induced etch damage of MESFETs," *Solid State Electron.*, vol. 45, no. 1, pp. 13–17, Jan. 2001.
- Z.-Q. Fang, D. C. Look, X.-L. Wang, J. Han, F. A. Khan, and I. Adesida, "Plasma-etching-enhanced deep centers in n-GaN grown by metalorganic chemical-vapor deposition," *Appl. Phys. Lett.*, vol. 82, no. 10, pp. 1562–1564, Mar. 2003.
- A. V. Vertiatchikh and L. F. Eastman, "Effect of the surface and barrier defects on the AlGaN/GaN HEMT low-frequency noise performance," *IEEE Electron Device Lett.*, vol. 24, no. 9, pp. 535–537, Sep. 2003.
- O. Katz, G. Bahir, and J. Salzman, "Low-frequency 1/f noise and persistent transients in AlGaN–GaN HFETs," *IEEE Electron Device Lett.*, vol. 26, no. 6, pp. 345–347, Jun. 2005.
- W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, "Influence of surface defect charge at AlGaN–GaN–HEMT upon Schottky gate leakage current and breakdown voltage," *IEEE Trans. Electron Devices*, vol. 52, no. 2, pp. 159–164, Feb. 2005.
- B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 21, no. 6, pp. 268–270, Jun. 2000.
- K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "Effects of SiN passivation and high-electric field on AlGaN–GaN HFET degradation," *IEEE Electron Device Lett.*, vol. 24, no. 7, pp. 421–423, Jul. 2003.
- A. P. Edwards, J. A. Mittereder, S. C. Binari, D. S. Katzer, D. F. Storm, and J. A. Roussos, "Improved reliability of AlGaN–GaN HEMTs using an  $\text{NH}_3$  plasma treatment prior to SiN passivation," *IEEE Electron Device Lett.*, vol. 26, no. 4, pp. 225–227, Apr. 2005.
- M. D. Hampson, S. C. Shen, R. S. Schwindt, R. K. Price, U. Chowdhury, M. M. Wong, T. G. Zhu, D. Yoo, R. D. Dupuis, and M. Feng, "Polyimide passivated AlGaN–GaN HFETs with 7.65 W/mm at 18 GHz," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 238–240, May 2004.
- W. K. Wang, C. H. Lin, P. C. Lin, C. K. Lin, F. H. Huang, Y. J. Chen, G. T. Chen, and J. I. Chyi, "Low-k BCB passivation on AlGaN–GaN HEMT fabrication," *IEEE Electron Device Lett.*, vol. 25, no. 12, pp. 763–765, Dec. 2004.
- R. Chu, L. Shen, N. Fichtenbaum, D. Brown, S. Keller, and U. K. Mishra, "Plasma treatment for leakage reduction in AlGaN/GaN and GaN Schottky contacts," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 300–302, Apr. 2008.
- T. Kikkawa, M. Nagahara, N. Okamoto, Y. Tateno, Y. Yamaguchi, N. Hara, K. Joshi, and P. M. Asbeck, "Surface-charge controlled AlGaN/GaN-power HFET without current collapse and  $G_m$  dispersion," in *IEDM Tech. Dig.*, Dec. 2001, pp. 585–588.
- C. Chan, T. Lee, S. Hsu, L. Chen, and Y. Lin, "Impacts of gate recess and passivation on AlGaN/GaN HEMTs," *Jpn. J. Appl. Phys.*, vol. 46, no. 2, pp. 478–484, Feb. 2007.
- S. Arulkumaran, T. Egawa, H. Ishikawa, and T. Jimbo, "Comparative study of drain current collapse in AlGaN/GaN high-electron-mobility transistors on sapphire and semi-insulating SiC," *Appl. Phys. Lett.*, vol. 81, no. 16, pp. 3073–3075, Oct. 2002.
- H. Hasegawa, T. Inagaki, S. Ootomo, and T. Hashizume, "Mechanisms of current collapse and gate leakage currents in AlGaN/GaN heterostructure field effect transistors," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 21, no. 4, pp. 1844–1855, Jul. 2003.
- T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto, and K. Maezawa, "A study on current collapse in AlGaN/GaN HEMTs induced by bias stress," *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2015–2020, Oct. 2003.
- G. Meneghesso, F. Rampazzo, P. Kordos, G. Verzellesi, and E. Zanoni, "Current collapse and high-electric-field reliability of unpassivated GaN/AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2932–2941, Dec. 2006.



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