

Square-Gate AlGaIn/GaN HEMTs With Improved Trap-Related Characteristics

Yu-Syuan Lin, Jia-Yi Wu, Chih-Yuan Chan, Shawn S. H. Hsu, *Member, IEEE*,
Chih-Fang Huang, *Member, IEEE*, and Ting-Chi Lee

Abstract—In this brief, the trap-related characteristics of high-breakdown AlGaIn/GaN high-electron-mobility transistors (HEMTs) were investigated. Compared with a conventional multifinger layout, the square-gate design presented reduced the current collapse from 19% to 6% and almost eliminated the gate lag. The flicker noise density and the gate leakage decreased from 1.16×10^{-10} to 1.17×10^{-11} 1/Hz ($f = 100$ Hz) and from 7.36×10^{-5} to 1.80×10^{-6} A/mm ($V_{GS} = -4$ V and $V_{DS} = 100$ V), respectively. The breakdown voltage was also improved from 350 to 650 V. With the channel area away from the defects generated by the mesa etching process, the square-gate AlGaIn/GaN HEMTs demonstrated excellent performance with much less trapping effects.

Index Terms—High-electron-mobility transistor (HEMT), layout, power semiconductor devices.

I. INTRODUCTION

HIGH-PERFORMANCE AlGaIn/GaN high-electron-mobility transistors (HEMTs) have been successfully demonstrated for high-power applications owing to the excellent material properties of GaN [1], [2]. However, the degradation and reliability problems of GaN HEMTs, caused by the trap-related effects, have been a critical issue that is widely discussed in recent years [3]–[6]. These defects may result from surface states, dislocations in the buffer layer, and plasma etch damage [7]–[11], which act as trapping–detrapping centers to affect device characteristics. The well-known phenomena are the current collapse [3], [4], [6], and gate-lag effects [3], [5], [6], which degrade the device transconductance and current density. The traps existing in the transistor were also reported to be closely related to the flicker noise characteristics [12], [13]. In addition, the defect charges around the gate finger not only cause barrier narrowing in the AlGaIn cap layer, leading to increased gate leakage current [14], but also bring out a higher electric field density at the gate

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Y.-S. Lin, S. S. H. Hsu, and C.-F. Huang are with the Department of Electrical Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan (e-mail: shhsu@ee.nthu.edu.tw).

J.-Y. Wu and C.-Y. Chan were with the Department of Electrical Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan. They are currently with Taiwan Semiconductor Manufacturing Company, Hsinchu 30075, Taiwan.

T.-C. Lee is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan.

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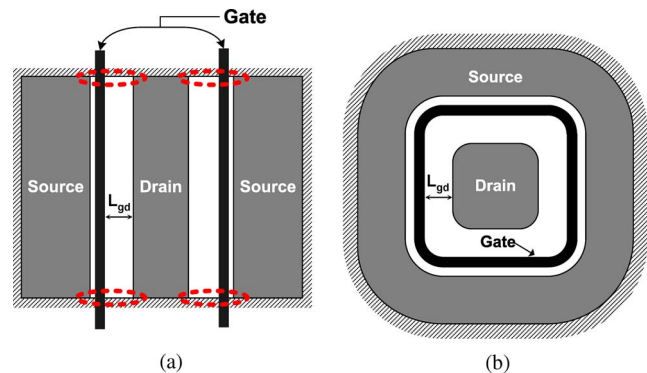


Fig. 1. AlGaIn/GaN HEMTs: (a) Two-finger and (b) square-gate layouts.

electrode edge, resulting in enhanced impact ionization and reduced breakdown voltage.

Many previous studies of GaN HEMTs focused on the origins of the surface states and technologies, such as various passivation methods and surface treatments, for trapping effect reduction [5], [15]–[22]. Excellent results for the transistors with small current collapse have been reported [14]–[19], [21], [22]. However, these works only investigated typical multifinger configurations with a small gate-to-drain distance L_{gd} (typically, 1–3 μm), which were not suitable for applications up to several hundred volts. In this study, we found that the trapping effect is severe for conventional multifinger transistors with a large L_{gd} (12 μm in this case), even with careful passivation, because of the traps located around the RIE-etched mesa edge. Compared with GaAs, GaN has a higher bonding energy and is more chemically inert [7]. Therefore, the RIE process for GaN etching is more difficult and requires higher ion energy and plasma flux, which often generate ion-induced damages and unsmoothed sidewalls [7]. Previous studies reported that the etching process for mesa isolation in GaN-based devices produced deep level traps, causing increased leakage current [7]–[11]. In this brief, the square-gate layout approach is proposed to reduce the effects of traps at the mesa edge on the transistor characteristics. The trap-related characteristics such as current collapse, gate lag, flicker noise, gate leakage, and breakdown voltage are investigated to verify this viewpoint. The square-gate GaN HEMTs were reported, and an excellent breakdown voltage up to 8300 V was achieved [2]. However, the advantage of improved trap-related characteristics of using the square-gate design has not been discussed, which is the main scope of this study.

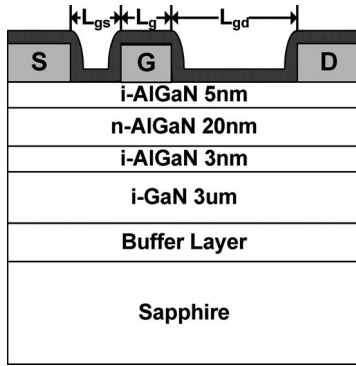


Fig. 2. Layer structure of the AlGaIn/GaN HEMTs.

II. DEVICE DESIGN AND FABRICATION

Fig. 1 shows the layouts of both the two-finger device and the square-gate topology. The mesa edges are highlighted by diagonal strips in both layouts. For the two-finger design in Fig. 1(a), the gate fingers are extended beyond the mesa edge to ensure that the channel is fully depleted under the OFF state, and the boundary of the channel is defined by the mesa. Note that the mesa process is essential for electrical isolation of individual transistors. With the identical layer structure and process steps, the reduced trapping effects, as will be carried out later, can mainly be ascribed to the square-gate design with eliminated mesa edge effect. As indicated in Fig. 1(b), the critical channel area (between the source and the drain) is fully surrounded by the source region rather than that exposed to the mesa edge [encircled by the dotted line, see Fig. 1(a)] in the conventional two-finger layout.

The cross section of the modulation-doped AlGaIn/GaN heterostructure is shown in Fig. 2. The device structure was grown on a c-plane sapphire substrate by metal-organic chemical vapor deposition. The epitaxial structure consisted of a GaN buffer layer, a 3- μm undoped GaN layer, a 3-nm undoped AlGaIn layer, a 20-nm n-doped AlGaIn barrier layer, and, finally, a 5-nm undoped AlGaIn cap layer. The Al mole fraction in the AlGaIn layer was 0.25. Device isolation was achieved by dry etching using a Cl_2/Ar gas mixture, and a silicon nitride layer, 1.2 μm thick, was deposited for surface passivation. It is worth mentioning that the etching process and surface passivation were carefully optimized for the current collapse effect. Using a similar process, the maximum drain current reduction was recovered from 37.5% to only 6.9% for the Cl_2/Ar -recessed GaN HEMTs ($L_{\text{gd}} = 2 \mu\text{m}$) [22].

In this study, the gate length L_g and the gate-to-source spacing L_{gs} are both 2 μm for the two designs, while a large gate-to-drain spacing L_{gd} of 12 μm is used as the drift extension region. The overall channel widths of both devices are 400 μm . Fig. 3 compares the typical I_D - V_{DS} characteristics of the two designs. As can be seen, the curves are almost identical, and well-defined pinchoff characteristics can be observed. The typical threshold voltage V_{th} is ~ -4 V. The maximum current density and transconductance are ~ 250 mA/mm ($V_{\text{GS}} = 1$ V, $V_{\text{DS}} = 10$ V) and ~ 75 mS/mm ($V_{\text{GS}} = -1$ V, $V_{\text{DS}} = 10$ V), respectively. It should be mentioned that the gate electrode in the square-gate design can be connected in a repeatable manner by

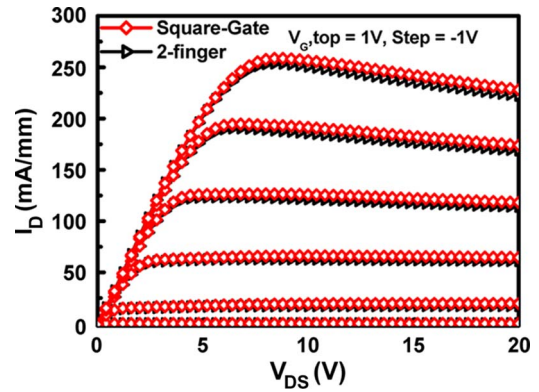


Fig. 3. Measured I_D - V_{DS} characteristics for both two-finger and square-gate devices.

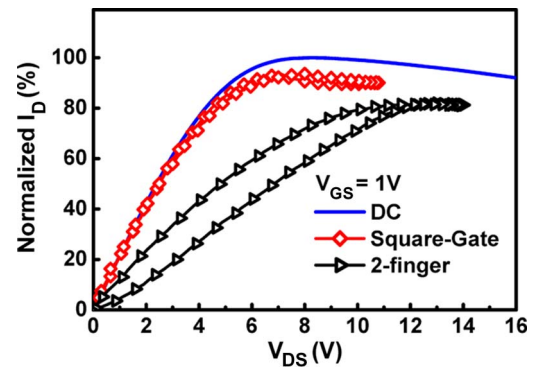


Fig. 4. Current collapse characteristics for both two-finger and square-gate devices.

a Ti/Au top metal layer above the SiN passivation layer through a via hole. In this way, a multifinger transistor can be realized for high-power applications.

III. RESULTS AND DISCUSSION

The current collapse measurement of the device was performed under the sweep of a 60-Hz rectified sine wave using a Tektronix 370 curve tracer. Note that the drain voltage is supplied as a rectified sine wave of 60 Hz, while a pulse signal is applied to the gate with a duration of 250 μs , which is suitable for observing the collapse effect [22], [23]. The current collapse effect in GaN-based devices has been investigated, which can be explained by the electron injection into the surface states [24]–[26]. With the surface states existing between the gate and drain area, the captured electrons in the slow traps cannot respond fast enough to the applied pulse signal. The trapped electrons induce a negative voltage to deplete the channel, causing a reduced drain current. Therefore, the current collapse effect closely depends on the trap density and can be used to test the traps in a transistor.

The impact of the trapping effects can be observed by comparing the dc I - V characteristics (measured by an Agilent semiconductor analyzer) with the swept signal as shown in Fig. 4 ($V_{\text{GS}} = 1$ V). As can be seen, the traditional two-finger device shows a clear degradation when compared with the dc results, whereas the square-gate design has a much less current collapse effect. The hysteresis characteristic observed in the

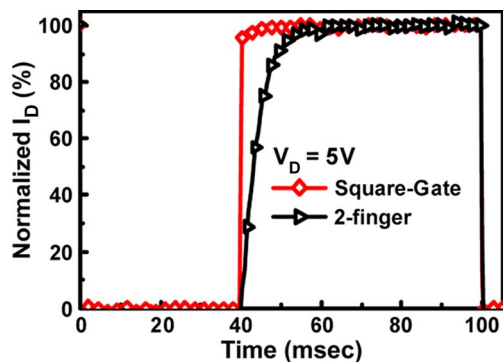


Fig. 5. Measured gate-lag characteristics for both two-finger and square-gate devices.

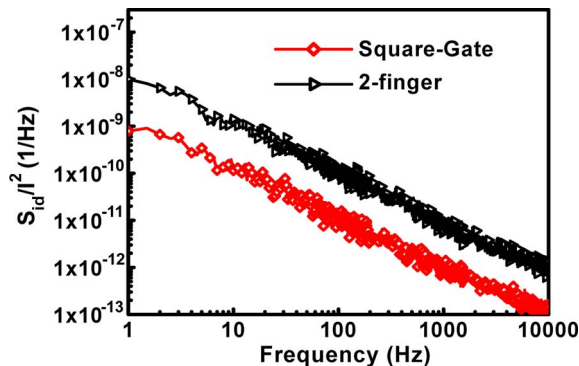


Fig. 6. Measured flicker noise characteristics for both two-finger and square-gate devices.

two-finger device also indicates that the trapped carriers have very large time constants. The current collapse factor ΔI_{\max} , defined as $(I_{dc_peak} - I_{ac_peak})/I_{dc_peak}$ at $V_{GS} = 1$ V, was reduced from $\sim 19\%$ to only $\sim 6\%$ for the square-gate design, where I_{dc_peak} is the maximum dc drain current within the applied drain voltage range and I_{ac_peak} has a similar definition but with the swept ac signal. The results suggest that a severely damaged mesa edge may not be fully recovered even when carefully passivated by SiN. For the two-finger design, the remaining traps along the mesa edge are in the vicinity of the active area, which can still affect the channel carriers. This may not be obvious for devices with a small L_{gd} (typically, 1–3 μm), but it becomes a dominant factor in power devices with a relatively large L_{gd} . In this case, the overall length along the sensitive channel area exposed to the mesa edge is around 48 μm [$4 \times 12 \mu\text{m}$ as indicated in Fig. 1(a)]. In contrast, even with large L_{gd} in the square-gate devices, the critical channel area is surrounded by the source and is far away from the mesa edge. As a result, the square-gate design presents a significantly reduced current collapse effect.

The gate-lag measurements use a pulse voltage biased from -5 to 0 V at the gate terminal by the Agilent 8114 pulse generator [22]. The period and the duty cycle of the gate pulse voltage used were 0.1 s and 60%, respectively. Fig. 5 shows the results with the drain bias fixed at 5 V. For the two-finger device, an obvious drain current lag can be observed, where the lag is longer than 10 ms. On the other hand, the gate-lag effect is almost eliminated in the square-gate device. Similar to the current collapse effect, the lag of the drain current is also due to the fact that the captured electrons in the traps cannot respond fast enough to the gate pulse signal. As can be seen, the observation in the gate-lag measurements presents a consistent trend with the current collapse results. Note that the trapping effect can mainly be observed under the applied ac pulse signal, and, thus, similar dc I - V characteristics and threshold voltages are obtained in both designs as shown in Fig. 3.

Fig. 6 shows the normalized flicker noise current spectral densities S_{id}/I^2 of both designs ($V_{GS} = 0$ V and $V_{DS} = 1$ V). Compared with the traditional two-finger device, the noise level of the square-gate transistor improves about one order of magnitude from 1.16×10^{-10} to 1.17×10^{-11} 1/Hz (at 100 Hz). The result shown in Fig. 7 is the measured OFF-state gate leakage current. The square-gate device presents a significantly

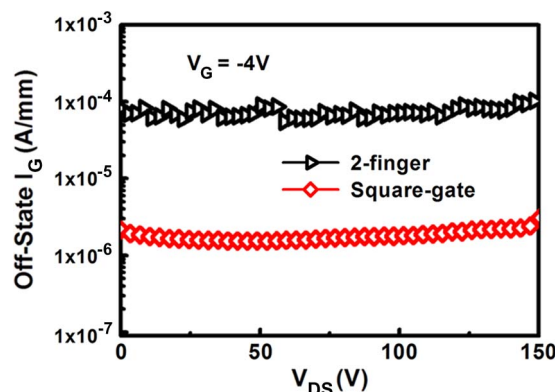


Fig. 7. Gate leakage characteristics for both two-finger and square-gate devices.

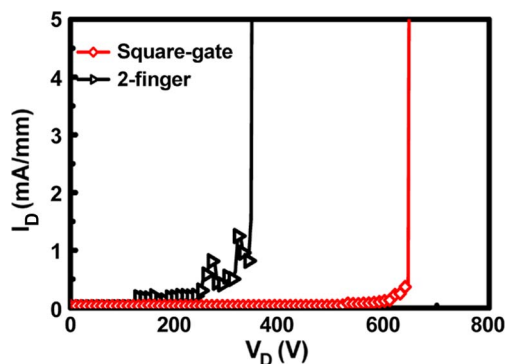


Fig. 8. Measured breakdown voltages for both two-finger and square-gate devices.

lowered leakage current by almost two orders of magnitude in the range of $\sim 10^{-6}$ A/mm. As mentioned earlier, the flicker noise characteristic and gate leakage current level are both closely related to the defects in the transistor. The square-gate design eliminates the mesa edge trapping effect, leading to reduced flicker noise and gate leakage current.

Finally, the improved OFF-state blocking capability was also confirmed. The breakdown voltage V_{BK} of the device with the square-gate layout shown in Fig. 8 can reach 650 V, whereas the two-finger device can reach only about 350 V. The contribution of the square-gate design for the significantly enhanced breakdown characteristic could be twofold. First, the rounded

corners can reduce the high electric field at the gate finger tips in the two-finger design. In addition, the trap charges underlying the gate finger, which can lower V_{BK} , are avoided in the square-gate design. Compared with the state of the art [2], the square-gate GaN HEMTs using a field-plate (FP) structure show a V_{BK} of ~ 500 V ($L_{gd} = 10$ μm) and a V_{BK} of ~ 1000 V ($L_{gd} = 20$ μm). Our device, without the additional FP structure, has a V_{BK} of up to 650 V ($L_{gd} = 12$ μm), which demonstrates excellent quality of the transistors studied here regarding both technology and design. All the measurement results show that the square-gate design is effective in eliminating the effects of traps associated with the mesa edge.

IV. CONCLUSION

In this brief, the square-gate design has been proposed to alleviate the trap-related effects associated with plasma etch damage along the mesa edge in AlGaIn/GaN HEMTs. Compared with the conventional multifinger layout, the square-gate device presented a significantly improved current collapse and gate-lag effect. The flicker noise level and the OFF-state gate leakage current were both reduced by more than one order of magnitude. A much higher breakdown voltage up to 650 V was also obtained. The results suggest that the defects around the mesa edge generated by the RIE process are critical, particularly for the high-power devices with a large gate-to-drain extension distance.

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Yu-Syuan Lin was born in Changhua, Taiwan, in 1981. He received the B.S. degree from the Department of Electrical Engineering, National Tsing Hua University, Hsinchu, Taiwan, in 2003, where he is currently working toward the Ph.D. degree in the Institute of Electronics Engineering.

His current research interests include the design and fabrication of GaN high-voltage and RF devices and modeling of GaN and silicon-based RF devices.



Jia-Yi Wu was born in Nantou, Taiwan, in 1983. He received the M.S. degree from the Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan, in 2008.

He is currently a Process Engineer with Taiwan Semiconductor Manufacturing Company, Hsinchu. His research interests include the design, fabrication, and characterization of GaN high-voltage and RF devices.



Chih-Yuan Chan was born in Kaohsiung, Taiwan, in 1979. He received the M.S. and Ph.D. degrees from the Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan, in 2003 and 2008, respectively.

He is currently an RF Device Modeling/Characterization Engineer with Taiwan Semiconductor Manufacturing Company, Hsinchu. His research interests include Si-based microwave CMOS devices, layout optimization for high-frequency devices, noise characterization and modeling, and

RF measurement technology.



Shawn S. H. Hsu (M'04) was born in Tainan, Taiwan. He received the B.S. degree from National Tsing Hua University, Hsinchu, Taiwan, in 1992, the M.S. and Ph.D. degrees from the Electrical Engineering and Computer Science Department, University of Michigan, Ann Arbor, MI, in 1997, and 2003, respectively.

He is currently an Associate Professor with the Institute of Electronics Engineering, National Tsing Hua University. His research interests include the high-frequency transistor/interconnect modeling and the design of MMICs and RFICs using Si/III-V-based devices for low-noise, high-linearity, and high-efficiency system-on-chip applications.

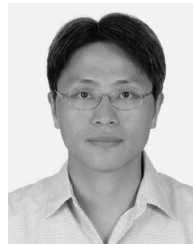
Prof. Hsu was the recipient of the Junior Faculty Research Award of National Tsing Hua University in 2007.



Chih-Fang Huang (M'04) received the M.S.E. and Ph.D. degrees from the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, in 2000 and 2003, respectively. His doctoral work focused on the design, fabrication, and characterization of 4H-SiC BJTs for high-power high-temperature applications.

In 2004, he joined Advanced Power Technology CO (now Microsemi), Boulder, CO, where he engaged in the development of SiC BJTs for RF power amplification and SBDs for power electronics appli-

cations. He is currently an Assistant Professor with the Department of Electrical Engineering, National Tsing Hua University, Hsinchu, Taiwan.



Ting-Chi Lee was born in Taoyuan, Taiwan, in 1971. He received the Ph.D. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2004. His main work during the Ph.D. study included the device structure design, device fabrication, and characterization of GaN heterostructure field-effect transistors (HFETs).

After graduation, he worked with the Department of Electronics Engineering, National Chiao Tung University, as a Postdoctoral Researcher, where he studied the effects of surface treatment on GaN

HFETs, including gate recess and passivation. In 2006, he joined the Electronics and Optoelectronics Research Laboratory, Industrial Technology Research Institute, Hsinchu, as an Engineer. In 2009, he returned to the Department of Electronics Engineering, National Chiao Tung University, as a Postdoctoral Researcher, where he is studying Sb-based high-speed HFETs.