# AlGaN/GaN HEMTs on Silicon With Hybrid Schottky–Ohmic Drain for RF Applications

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***Abstract*— In this paper, the AlGaN/GaN high electron mobility transistors on a low resistivity Si substrate with the hybrid drain structure for RF applications are analyzed in detail, based on measurements, TCAD simulation, model extraction, and delay time calculation of the transistors. Owing to the *E*-field redistribution of the Schottky extension, both the leakage current and the breakdown voltage can be improved. Also, the enhanced RF performance can be attributed to the reduced transit time and increased transconductance, resulting from the increased electron velocity and reduced drain depletion width. With a 3-$\mu$m extension length and a 0.2-$\mu$m gate length, $f_T$ and $f_{MAX}$ of transistors can be improved from 32.7 to 49.9 GHz (52.6%) and from 35.8 to 49.2 GHz (37.4%), respectively, with ON–OFF ratio enhancement by four orders of magnitude. The breakdown voltage was improved from 21 to 38 V (80.9%).**

***Index Terms*— GaN, high electron mobility transistors (HEMTs), hybrid drain, RF, Schottky, silicon substrate, transit time.**

## I. Introduction

THE properties of high electron saturation velocity and large breakdown voltage in GaN-based materials pave the way for high power and high frequency applications. Recently, GaN-based transistors grown on a silicon substrate have demonstrated outstanding characteristics, which makes it realistic to obtain low cost and high-performance components and systems [1]–[4]. One important issue to enhance the high frequency characteristics is the scaling of devices, which were reported from different researchers for the GaN-based transistors [5]–[8]. Scaling of the gate length is the most commonly used approach. Another critical geometrical parameter not often emphasized is the source–drain distance ($L_{SD}$). With a scaled $L_{SD}$, the intrinsic path of carrier propagation is shortened, leading to improved high frequency performance.

Conventionally, the source–drain distance of ohmic electrodes (typical $L_{SD} \sim$ 1-2 $\mu$m) is limited by the metal morphology due to the high temperature alloying process. With an aggressively scaled $L_{SD}$, the alignment of gate electrode becomes difficult and the distance from the gate to both source and drain could vary [9], [10]. An $n^+$-GaN regrowth approach with nonalloyed ohmic was demonstrated in AlGaN/GaN high electron mobility transistors (HEMTs) on SiC substrate, which achieved excellent $f_T/f_{MAX}$ of 260/394 GHz for $L_{SD}$ of only 170 nm with a gate length of 40 nm [6]. As can be seen, the nonalloy process with a rather complicated regrown structure was used to reduce the source–drain distance for high frequency applications. As the gate–drain distance reduces, the impact of drain voltage on the potential barrier of buffer layer also becomes significant, resulting in an increased subthreshold drain leakage [11]. Therefore, reducing the source–drain distance of devices for improved frequency response while maintaining simple process steps and high reverse blocking capability remains challenging.

In our previous work, the hybrid Schottky–ohmic drain structure employed in GaN-based devices for power electronics applications was reported to simultaneously improve the breakdown voltage and leakage current [12]. In this paper, we demonstrate the AlGaN/GaN HEMTs using a relatively simple line gate combined with the proposed Schottky extension $L_{ext}$ for improved high frequency characteristics, which has not been discussed in the previous published studies. With a properly designed $L_{ext}$, the altered *E*-field in the buffer and channel can prevent degradation of the leakage current and breakdown voltage from the effectively reduced $L_{SD}$. More importantly, the hybrid drain structure enhances the electron velocity and reduces drain depletion width, leading to improved transit delay and high frequency performance of transistors even on a low resistivity (LR) Si substrate. The detailed analysis of TCAD simulation, equivalent circuit model, and delay time is conducted to further investigate the impact of Schottky extension on device RF characteristics.

This paper is organized as follows. Section II presents the device structure and fabrication of the proposed devices with the hybrid drain design. Section III shows the measured dc characteristics for the devices with different lengths of Schottky extension. Section IV compares the RF characteristics for the devices with/without Schottky drain extension. The observed trends for both dc and RF characteristics are explained by the TCAD simulation. The modified equivalent circuit model including the hybrid drain and substrate effect is established. Also, the analysis of delay time is conducted in detail. Section V concludes this paper.

## II. Device Structure and Fabrication

The layer structure of the AlGaN/GaN HEMTs grown by metalorganic chemical vapor deposition on an LR silicon substrate is shown in Fig. 1. The structure from the bottom to top is a 2-$\mu$m buffer layer, a 2-$\mu$m GaN channel,

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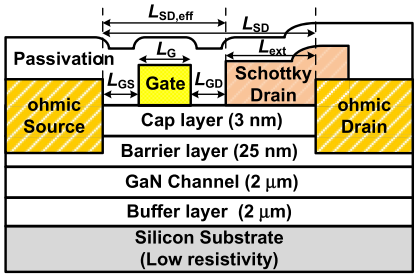



Fig. 1. Cross section of the AlGaN/GaN HEMT on silicon substrate.

a 25-nm $Al_{0.25}Ga_{0.75}N$ barrier layer, and a 3-nm UID GaN cap layer. The fabricated GaN-on-Si HEMTs have a width of $2 \times 50$ $\mu$m, a gate length of 0.2 $\mu$m, and a gate–source spacing ($L_{GS}$) of 0.4 $\mu$m. The length of Schottky drain extension ($L_{ext}$) was designed as 1, 2, 3, and 4 $\mu$m with the fixed gate–drain spacing ($L_{GD}$) of 0.4 $\mu$m and the effective source–drain distance $L_{SD,eff}$ of 1 $\mu$m by taking the Schottky drain into consideration. Note that the source–drain distance (ohmic electrodes) for the reference devices without Schottky extension ($L_{ext} = 0$ $\mu$m) was designed as $L_{SD} = 2$ $\mu$m. The main consideration is the yield of fabrication for the reference devices if $L_{SD}$ of 1 $\mu$m is used. As mentioned in Section I, the source–drain distance of ohmic electrodes is limited by the metal morphology due to the high temperature alloying process. The proposed hybrid drain design offers the solution for reduced $L_{SD}$ with a good yield. We also compared the transistor characteristics both with $L_{SD}$ of 1 $\mu$m for the reference devices and the hybrid–drain devices by TCAD simulation to observe the RF characteristics. The device with Schottky extension shows clear improvement on the frequency response.

The ohmic contact was first fabricated with recess to reduce the contact resistance, and followed by the metal deposition of Ti/Al/Ni/Au using e-gun evaporation, and then with the rapid thermal annealing at 800 °C for 30 s in $N_2$ ambient. The mesa isolation was done by using dry etching with $Cl_2/BCl_3$ mixture gas for an etching depth of 350 nm. After mesa isolation, a 0.2-$\mu$m line gate was developed with e-beam lithography to demonstrate the high-performance RF devices. The Schottky metal stack of Ni/Au was then deposited using e-gun evaporation and followed by the liftoff process. After Schottky gate formation, the Schottky extension with a metal stack of Ti/Au was formed. Note that this differs from our previous process using the same metal layers for both Schottky gate and hybrid drain [12]. The separated process steps allow a lower work function metal for the Schottky drain, resulting in a reduced turn-ON voltage. Finally, a multilayer passivation structure of $SiN_x/SiO_x/SiN_x$ was deposited by PECVD at 300 °C. The contact resistance ($R_c$) of 0.4 $\Omega \cdot$ mm and the sheet resistance ($R_{sh}$) of 486 $\Omega/\square$ were obtained, respectively, by the transmission line method (TLM) after passivation.

## III. DC Characteristics of Devices

Fig. 2(a) and (b) shows the dc $I$–$V$ characteristics for the devices with $L_{ext} = 0$ (reference device) and 3 $\mu$m, respectively. The $R_{ON}$ of ~3.7 and ~3.4 $\Omega \cdot$ mm can be

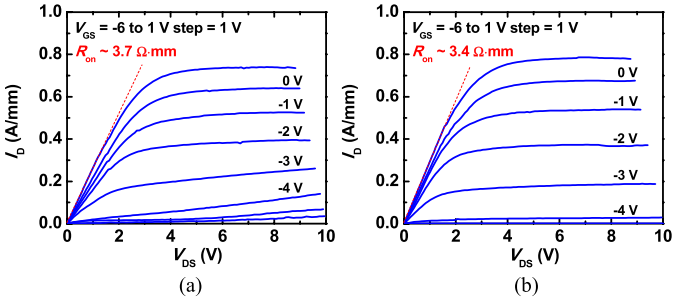



Fig. 2. $I_D$–$V_{DS}$ characteristics of the GaN-on-Si HEMTs ($W_G = 2 \times 50$ $\mu$m) for (a) $L_{ext} = 0$ $\mu$m and (b) $L_{ext} = 3$ $\mu$m.

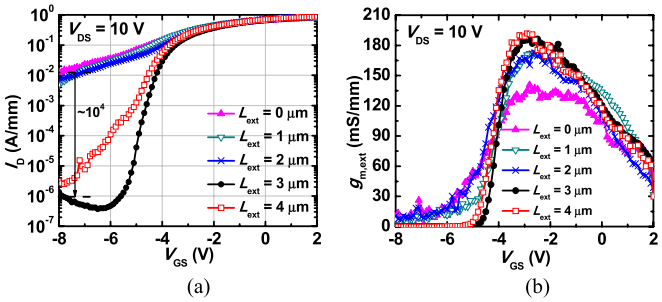
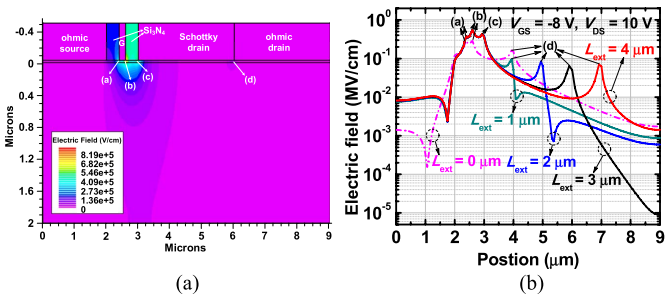



Fig. 3. Measured dc characteristics for (a) $I_D$–$V_{GS}$ and (b) $g_{m,ext}$-$V_{GS}$ at $V_{DS} = 10$ V.

extracted for the devices without and with Schottky extension, respectively. Compared with the estimated results by TLM (1.8 and 1.3 $\Omega \cdot$ mm, respectively), the extracted resistances are slightly higher. It should be pointed out that the TLM pattern and the actual HEMT structure are somehow different, which may be the origin of the discrepancy between the estimated and extracted results. A similar trend was also reported from other references [13], [14]. Fig. 3 shows the measured transfer characteristics of the devices with different values of $L_{ext}$. As shown in Fig. 3(a), a relatively high drain leakage current is observed for $L_{ext} \leq 2$ $\mu$m, whereas that is reduced obviously as $L_{ext}$ further increases. With a small $L_{ext}$, the redistribution of $E$-field by the Schottky extension is not very effective, and a high $E$-field still exists in the GaN channel/buffer layer near the edge of ohmic drain. The electrons inject into the GaN channel/buffer layer due to the $E$-field can cause a rapid increase of the subthreshold drain leakage current, which can be identified by the relatively small ON–OFF ratio. In contrast, the leakage current of the device with $L_{ext}$ of 3 $\mu$m is suppressed significantly by about four orders of magnitude compared with the reference devices, which can be attributed to the effectively reduced $E$-field peak intensity of ohmic drain and the alleviated leakage current [12], [15], [16]. The result suggests that the design parameter $L_{ext}$ of ~3 $\mu$m is an optimized extension length for low leakage. Fig. 3(b) shows the dc $g_{m,ext}$ (extrinsic transconductance) characteristics for the devices with different $L_{ext}$. The peak $g_{m,ext}$ at $V_{GS} = -3$ V is 141 and 187 mS/mm for the devices with $L_{ext}$ of 0 and 3 $\mu$m, respectively. As can be observed, the devices with Schottky extension exhibit an improved $g_{m,ext}$, which will be explained in Section IV together with the small-signal model and delay time analysis.

The $E$-field distribution of TCAD simulation was performed to support our explanations for the observed trends in Fig. 3(a).

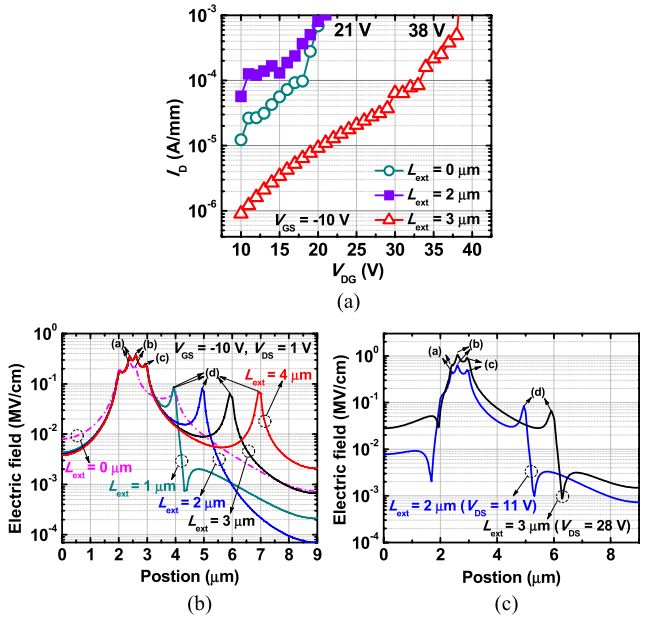



(a) (b)

Fig. 4. TCAD simulation of the hybrid drain devices. (a) Device structure for $L_{\text{ext}} = 3\ \mu$m. (b) $E$-field distribution for $V_{\text{GS}} = -8$ V and $V_{\text{DS}} = 10$ V.

Note that the positions of (a), (b), (c), and (d) shown in Fig. 4(a) are the locations of gate edge at source side, gate edge at drain side, edge of Schottky drain, and edge of ohmic drain, respectively. As shown in Fig. 4(b), the peak at the ohmic drain edge clearly reduces for the hybrid drain devices compared with the reference device (see position at 4 $\mu$m). In addition, compared with the devices for $L_{\text{ext}} = 1$ and 2 $\mu$m, the device with $L_{\text{ext}} = 3\ \mu$m shows the further reduced electric field at the ohmic drain edge, leading to a relatively large suppression of leakage current. As $L_{\text{ext}}$ further increases to 4 $\mu$m, the electric field of ohmic drain increases again, which could be the origin of the slightly increased drain leakage current. The observed trend in simulation agrees with the measured leakage current. It should be emphasized that the simulated results shown here do not include the metal spikes underneath the ohmic contacts. It has been reported from different researchers that the spikes underneath ohmic contact from the alloying process could produce local $E$-field peaks, resulting in an increased buffer leakage current in GaN HEMTs [16]–[18]. The spikes are difficult to be included in practical TCAD simulation, but could also be an important factor to affect the distribution of the $E$-field and leakage current. Although the difference in the simulated $E$-field peak intensity between $L_{\text{ext}} = 2$ and 3 $\mu$m is not very large, considering the spikes together with the $E$-field redistribution around the ohmic drain, the combined effect could lead to a significantly suppressed leakage current as observed in the experiments, which may not be fully explained by the simulated results.

It is also of interest to compare the proposed GaN devices on the LR substrate with other substrates such as sapphire and SiC. A test pattern was fabricated to investigate the buffer leakage with the removed 2DEG channel between two mesa-isolated ohmic contacts [17]. The measured leakage current across the contacts (separated by 5 $\mu$m) is in a range from $3.5 \times 10^{-11}$ to $7.7 \times 10^{-8}$ A/mm for the bias voltage from 0 to 100 V. Note that the corresponding buffer resistivity of $\sim 1.3 \times 10^{8}\ \Omega\cdot$cm is close to that of the GaN layer on sapphire with carbon doping [19]. The leakage current in the case of GaN grown on SiC substrate with C-doped buffer layer was also reported to exhibit a very low leakage current (<1 nA at 100 V) due to small lattice mismatch [20]. The low leakage current obtained in this paper suggests that the GaN on LR silicon substrate should be sufficiently good for the RF devices if with a high-resistivity buffer layer.




(a) (b) (c)

Fig. 5. (a) Measured three-terminal OFF-state breakdown characteristics. (b) Simulated $E$-field distribution for $V_{\text{GS}} = -10$ V and $V_{\text{DS}} = 1$ V with different values of $L_{\text{ext}}$. (c) Simulated $E$-field distribution of the devices for $L_{\text{ext}} = 2$ and 3 $\mu$m with the bias conditions corresponding to Fig. 5(a) when breakdown occurs.

Fig. 5 shows the dependence of measured breakdown voltage $V_{\text{BK}}$ (at $V_{\text{GS}} = -10$ V) on $L_{\text{ext}}$, including the reference device. The breakdown voltage was improved from 21 to 38 V for $L_{\text{ext}}$ increasing from 2 to 3 $\mu$m. With a properly extended Schottky drain, the alleviated $E$-field peak in the drain side around the ohmic spikes can help to suppress the leakage current, and therefore, the devices show an improved breakdown voltage. The leakage current observed in Fig. 3(a) with a significant improvement for the devices with $L_{\text{ext}} = 3\ \mu$m is consistent with $V_{\text{BK}}$ observed in Fig. 5(a). The simulated $E$-field distribution for $V_{\text{GS}} = -10$ V and$V_{\text{DS}} = 1$ V shown in Fig. 5(b) indicates that the $E$-field at the ohmic drain edge for $L_{\text{ext}} = 2\ \mu$m is similar with that for the reference device, which could be the reason that the weak dependence of $I_D$ on a relatively low $V_{\text{DS}}$ was found for $L_{\text{ext}} = 0$ and 2 $\mu$m in Fig. 5(a). It can be observed that the $E$-field peak of the edge of ohmic drain is reduced for $L_{\text{ext}} = 3\ \mu$m, which could explain the suppressed leakage current. Fig. 5(c) shows the simulated $E$-field distribution for the devices with $L_{\text{ext}} = 2$ and 3 $\mu$m at $V_{\text{DS}}$ of 21 and 38 V when breakdown occurs, respectively, corresponding to Fig. 5(a). A slightly smaller $E$-field peak of ohmic drain for the case of $L_{\text{ext}} = 3\ \mu$m can be observed even with a large difference in the applied drain bias. The result agrees that the Schottky drain is effective to reduce $E$-field around the ohmic drain for $L_{\text{ext}} = 3\ \mu$m to achieve a higher $V_{\text{BK}}$.

## IV. RF Characteristics of Devices

### A. Analysis of Small-Signal Equivalent Circuit Model

The modified small-signal equivalent circuit model for the GaN-on-Si HEMTs including the hybrid drain and substrate effect is shown in Fig. 6, where most of the definitions of general model parameters can be found in [21]. Based on the

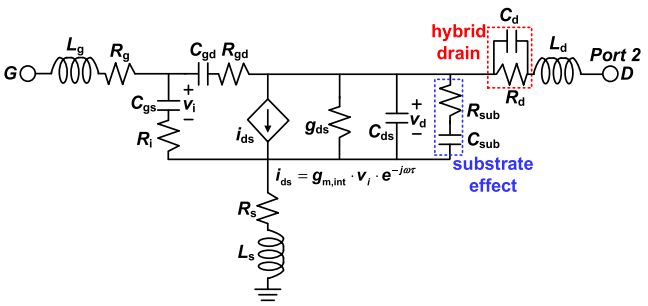



Fig. 6. Modified small-signal equivalent circuit model for the GaN-on-Si HEMTs with hybrid drain and substrate effect.

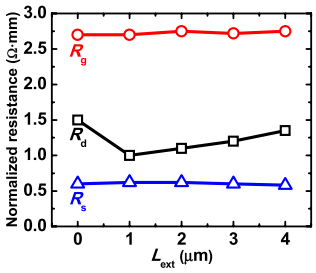



Fig. 7. Extracted parasitic resistances of the GaN-on-Si HEMTs with various $L_{\text{ext}}$ based on the small-signal model.

physical structure, the Schottky drain is modeled as an additional capacitance $C_d$ (due to Schottky depletion) in parallel with the drain resistance. The substrate-related parameters are modeled by $R_{\text{sub}}$ and $C_{\text{sub}}$, which are important for the devices grown on an LR silicon substrate. The extraction procedure of the substrate parameters is similar with that reported for CMOS transistors [22]. The delay $\tau$ associated with transconductance (see Fig. 6) is important for modeling at high frequencies, which can be extracted based on the method reported in [23]. The measurement of S-parameters was performed on-wafer by using the Agilent E8361C performance network analyzer. The cold-FET (CF) measurements ($V_{\text{DS}} = 0$ V) are used to extract the pad capacitances ($V_{\text{GS}} \ll 0$) and extrinsic parasitics ($V_{\text{GS}} \gg 0$ V). After deembedding of the pad capacitances, the extrinsic parasitics of the device can be obtained based on the method reported in [23]. Fig. 7 shows the normalized parasitic resistances $R_s$, $R_g$, and $R_d$ as a function of different values of $L_{\text{ext}}$, extracted under the zero bias condition ($V_{\text{GS}} = V_{\text{DS}} = 0$ V). It should be mentioned that the dependence of $R_d$ on $V_{\text{DS}}$ is difficult to be determined due to the appearance of intrinsic parasitic elements when $V_{\text{DS}} > 0$ V (i.e., hot-FET measurement). Nevertheless, the extraction of $R_d$ with CF measurement gives an initial value that helps to understand and find the trend of the extrinsic parameters. As can be seen, $R_d$ of the hybrid drain devices is smaller compared with that of the reference device, indicating the source–drain distance is effectively reduced by the Schottky drain extension. In addition, the drain resistance increases linearly with $L_{\text{ext}}$, which could be explained as the increased distance from the gate to the actual ohmic drain. The results suggest that the design parameter $L_{\text{ext}}$ should be kept relatively small to prevent $R_d$ degradation. Compared with the device without Schottky extension, $R_d$ is reduced up to 26% and 20% for the device with $L_{\text{ext}}$ of 2 and 3 $\mu$m, respectively.

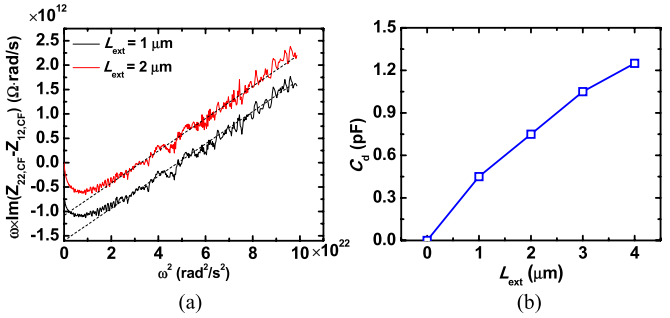



Fig. 8. (a) Parameter extraction procedure of $C_d$ for $L_{\text{ext}} = 1$ and 2 $\mu$m. (b) Extracted $C_d$ as a function of $L_{\text{ext}}$.

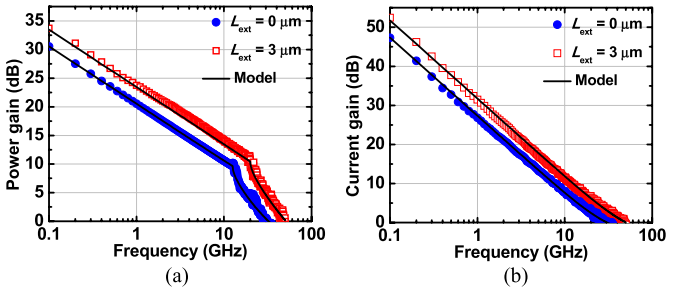



Fig. 9. GaN-on-Si HEMTs with/without Schottky extension for (a) power gain and (b) current gain comparison ($V_{\text{GS}} = -3$ V and $V_{\text{DS}} = 10$ V).

Note that the high-frequency signal could capacitively couple through Schottky extension, which reduces the effective $R_d$ and results in a weaker dependence of $R_d$ on the increased $L_{\text{ext}}$. This may be the origin of the discrepancy between the estimated $R_{\text{sh}}$ of $\sim$130 $\Omega/\square$ with the Schottky extension based on the slope of $R_d$ and the measured $R_{\text{sh}}$ by TLM.

It is also of great interest to investigate the dependence of $C_d$ on $L_{\text{ext}}$. The imaginary part of Z-parameters based on the CF measurement can be written as

$$\text{Im}(\omega Z_{12,\text{CF}}) = \omega^2 L_s - \frac{1}{C_s} \tag{1}$$

$$\text{Im}(\omega Z_{22,\text{CF}}) = \omega^2 (L_d + L_s) - \left(\frac{1}{C_s} + \frac{1}{C_d}\right) \tag{2}$$

where CF stands for cold FET and $C_s$ is the intrinsic source capacitance under the CF condition. Fig. 8(a) shows the $\omega \times \text{Im}(Z_{22,\text{CF}} - Z_{12,\text{CF}})$ as a function of $\omega^2$ and the drain capacitance $C_d$ can be extracted by the intercept point with the $y$-axis. The extracted $C_d$ increases with $L_{\text{ext}}$ as shown in Fig. 8(b), which agrees well with our prediction. The simulated results based on the small-signal model reveals that the introduction of $C_d$ can simultaneously improve $f_T$ and $f_{\text{MAX}}$. Improved $f_T$ of $\sim$10% (from 44.8 to 49.3 GHz) and $f_{\text{MAX}}$ of $\sim$7.5% (from 46.2 to 49.7 GHz) can be observed as $C_d$ increases from 0 ($L_{\text{ext}} = 0$ $\mu$m) to 1.25 pf ($L_{\text{ext}} = 4$ $\mu$m), which can be attributed to the reduced effective output capacitance (since $C_d$ is connected in series with $C_{\text{ds}}$, see Fig. 6), as can be observed from the increased imaginary part of $Z_{22}$.

Fig. 9 shows the measured and modeled power gain and current gain of the devices for $V_{\text{GS}} = -3$ V and $V_{\text{DS}} = 10$ V

TABLE I
SUMMARY OF INTRINSIC SMALL-SIGNAL MODEL PARAMETERS FOR THE 2 × 50 $\mu$m DEVICES

| $L_{ext}$ ($\mu$m) | $C_d$ (pf) | $R_i$ ($\Omega$·mm) | $C_{gs}$ (fF/mm) | $R_{gd}$ ($\Omega$·mm) | $C_{gd}$ (fF/mm) | $C_{ds}$ (fF/mm) | $g_{ds}$ (mS/mm) | $R_{sub}$ ($\Omega$·mm) | $C_{sub}$ (fF/mm) | $g_{m,int}$ (mS/mm) | $\tau$ (ps) | $f_{T\_model}$ /$f_{T\_meas.}$ (GHz) | $f_{MAX\_model}$ /$f_{MAX\_meas.}$ (GHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 | 1.25 | 0.3 | 671 | 9.5 | 74 | 41.5 | 26.5 | 5.9 | 24.7 | 202 | 1.6 | 46.7 /47.2 | 48.7 /47.9 |
| 3 | 1.05 | 0.3 | 671 | 9.5 | 77 | 41.5 | 27.1 | 5.7 | 25.6 | 218 | 1.5 | 49.1 /49.9 | 49.7 /49.2 |
| 2 | 0.75 | 0.3 | 663 | 9.5 | 88 | 41.5 | 28.2 | 5.5 | 26.5 | 198 | 1.6 | 44.8 /46.1 | 45 /45.2 |
| 1 | 0.45 | 0.3 | 689 | 9.5 | 82 | 41.5 | 29.5 | 5.4 | 27.1 | 185 | 1.7 | 39.7 /41.2 | 41.5 /40.5 |
| 0 | 0 | 0.3 | 672 | 11.5 | 65 | 34.5 | 25.5 | 9.1 | 22.7 | 146 | 2.2 | 31.1 /32.7 | 36.1 /35.8 |

with and without Schottky extension. The results based on the small-signal model are also included. Compared with the devices without the Schottky extension, $f_T$ and $f_{MAX}$ can be improved by 52.6% (from 32.7 to 49.9 GHz) and 37.4% (from 35.8 to 49.2 GHz), respectively. Fig. 10(a) shows $f_T$ and $f_{MAX}$ as a function of $L_{ext}$ measured at $V_{DS} = 10$ V and $V_{GS} = -3$ V, which indicates that $f_T$ and $f_{MAX}$ both increase with $L_{ext}$. Also, $f_T$ and $f_{MAX}$ both achieve the maximum values for $L_{ext} = 3$ $\mu$m, and the trend saturated when $L_{ext}$ increases further. The extracted intrinsic parameters are summarized in Table I. Note the $R_i$ of 0.3 $\Omega$·mm extracted by the approach reported in [24] results in the calculated sheet resistance of ~500 $\Omega/\square$ as taking $L_G + L_{GS}$ (see Fig. 1) into account, which is close to the obtained result from our TLM. It should be mentioned that the calculation of $R_i$ with $L_G + L_{GS}$ leads to a more accurate estimation as can also be observed in [1], [3], and [8]. Based on the extracted results of small-signal model in Table I, the transit time $\tau_{transit}$ [$\cong(C_{gs}+C_{gd})/g_{m,int}$] can be estimated as 5 and 3.4 ps for $L_{ext} = 0$ and 3 $\mu$m, respectively. The result indicates that the increased $g_{m,int}$ contributes to the reduced $\tau_{transit}$ and thus improved RF characteristics. Also, the increased $g_{m,int}$ indicates the enhanced electron velocity ($v_e$) with Schottky extension, since the intrinsic transconductance increases with $v_e$ [25]. In addition, the extracted $g_{m,int}$ gradually increases with the extension length ($L_{ext} = 1, 2, 3$ $\mu$m), which suggests that the $E$-field redistribution due to Schottky drain is helpful for the enhanced $v_e$. Using $f_T$ of 49.9 GHz and the three-terminal gate–drain breakdown voltage of 38 V ($L_{ext} = 3$ $\mu$m), a J-FOM of 1.9 THz · V can be obtained.

From the simulated results as shown in Fig. 10(b), it can be found that the Schottky extended device for $V_{GS} = -3$ V and $V_{DS} = 10$ V shows a significantly enhanced $E$-field between (b) and (c) (i.e., the gate–drain spacing) due to the $E$-field redistribution by Schottky extension compared with the conventional device. Also, the increased $E$-field between (a) and (b) (i.e., under the gate electrode) for the extended devices can be observed. Both of them suggest that the enhanced electron velocity can be achieved with the hybrid drain structure for improved frequency response. On the other hand, the relatively small dependence of the $E$-field change under the gate and at the gate–drain spacing on different values of $L_{ext}$ makes it difficult to explain the enhanced electron

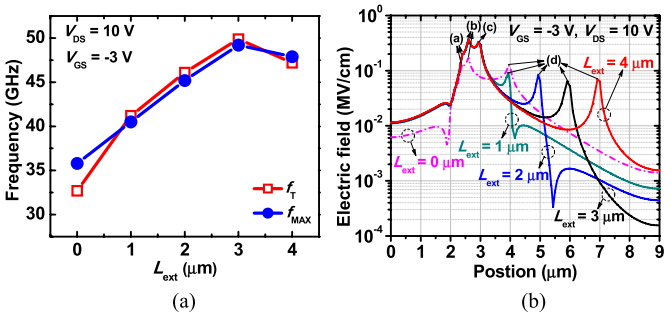
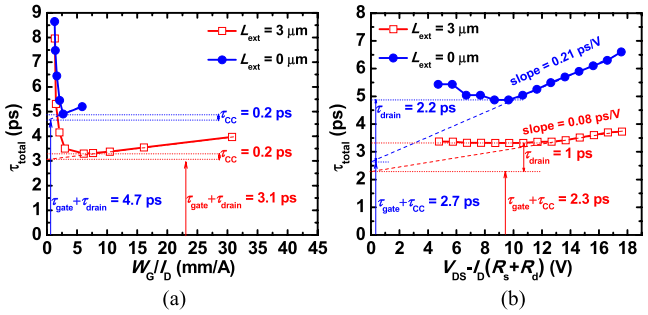



Fig. 10. (a) Measured $f_T$ and $f_{MAX}$ for the GaN-on-Si HEMTs ($W_G = 2 \times 50$ $\mu$m). (b) Simulated $E$-field distribution for $V_{GS} = -3$ V and $V_{DS} = 10$ V with different values of $L_{ext}$.

velocity as $L_{ext}$ increases. Based on the TCAD simulation, the observed trend of enhanced $f_T$ and $f_{MAX}$ with $L_{ext}$ in the experiments may be explained as follows. With the dual electrodes in the hybrid drain devices, some of the carriers are collected at the Schottky drain, while some continue to propagate and reach the ohmic drain. Taking the devices for $L_{ext} = 1$ and 2 $\mu$m up to position at 5 $\mu$m [see Fig. 10(b)] as an example, some of the electrons are under a high field up to ~4 $\mu$m to have a large carrier velocity, but the field suddenly drops and some of the electrons will be slow down for $L_{ext} = 1$ $\mu$m. In contrast, the electrons can still be accelerated between 4 and 5 $\mu$m under a high field for devices with $L_{ext} = 2$ $\mu$m device, which may result in a higher average electron velocity, and hence an increased $g_{m,int}$ with $L_{ext}$. To further investigate the impact of Schottky extension on device frequency response, the details of each delay component will be given by the analysis of delay time in the Section IV-B.

### B. Analysis of Delay Time

The analysis of delay time is performed by the measured $f_T$ with different values of $V_{GS}$ and $V_{DS}$, where the total delay $\tau_{total}$ can be deduced from (3) as the sum of channel charging delay $\tau_{cc}$, drain delay $\tau_{drain}$, and gate delay $\tau_{gate}$ [26]. $\tau_{cc}$ shown in (4) is associated with the $RC$ delays, which is proportional to the channel resistance [25]. $\tau_{drain}$ shown in (5) is the time required for the electrons to transport through the depletion region between the gate and the drain, where $\Delta L_G$




(a) (b)

Fig. 11. Total delay time $\tau_{\text{total}}$ as a function of (a) Inverse drain current density and (b) Voltage across the channel under the gate.

is the width of drain depletion and $\alpha$ is the effect of image charges of carrier transport in the depletion region [6]. Note that $\tau_{\text{drain}}$ increases with the drain bias due to the increased depletion region toward the drain, which is an important parameter for high-frequency characteristics of the device. As shown in (6), $\tau_{\text{gate}}$ is the time required for electrons to traverse under the gate, where $L_G$ is the gate length

$$\tau_{\text{total}} = \frac{1}{2\pi f_T} = \tau_{\text{cc}} + \tau_{\text{drain}} + \tau_{\text{gate}} \tag{3}$$

$$\tau_{\text{cc}} = (R_s + R_d) \cdot C_{\text{gd}} + (C_{\text{gs}} + C_{\text{gd}}) \cdot (R_s + R_d) \cdot \frac{g_{\text{ds}}}{g_{m,\text{int}}} \tag{4}$$

$$\tau_{\text{drain}} = \frac{\Delta L_G}{\alpha \cdot v_e} \tag{5}$$

$$\tau_{\text{gate}} = \frac{L_G}{v_e}. \tag{6}$$

Fig. 11(a) shows $\tau_{\text{total}}$ as a function of the inverse drain current density ($W_G/I_D$) with $V_{\text{GS}}$ varied from $-4$ to 1 V ($V_{\text{DS}} = 10$ V). The transit delay time $\tau_{\text{transit}}$ ($=\tau_{\text{gate}} + \tau_{\text{drain}}$) can be extrapolated at $W_G/I_D = 0$, and $\tau_{\text{cc}}$ is the difference between $\tau_{\text{total}}$ and $\tau_{\text{transit}}$. The intercept points of $\tau_{\text{transit}}$ of 3.1 and 4.7 ps are obtained for the device with and without Schottky extension, respectively. Also, $\tau_{\text{cc}}$ of 0.2 ps for both devices is obtained, which is in the same order of the calculated results of 0.32 ps according to the extracted model parameters in Table I. Fig. 11(b) shows the delay time as a function of the voltage across the channel underneath the gate with $V_{\text{DS}}$ varied from 5 to 18 V ($V_{\text{GS}} = -3$ V). The sum of $\tau_{\text{gate}}$ and $\tau_{\text{cc}}$ can be extrapolated at $V_{\text{DS}}$–$I_D \times (R_s + R_d) = 0$ and $\tau_{\text{drain}}$ can be determined based on $\tau_{\text{total}}$. Note that $R_d$ is assumed to be independent of $V_{\text{DS}}$ for simplicity. Also, the term $I_D \times (R_s + R_d)$ is much smaller than $V_{\text{DS}}$, and the simplification has a negligible effect on delay time analysis. The intercept points of $\tau_{\text{gate}} + \tau_{\text{cc}}$ of 2.3 and 2.7 ps and $\tau_{\text{drain}}$ of 1 and 2.2 ps can be obtained for the devices with and without Schottky extension, respectively. $\tau_{\text{gate}}$ of 2.1 and 2.5 ps are then calculated self-consistently for the device with and without Schottky extension. Note that the obtained $\tau_{\text{gate}}+\tau_{\text{drain}}$ ($=3.1$ ps) value of the Schottky extended device is close to the calculated transit time of 3.4 ps based on the small-signal model. Also, $\tau_{\text{drain}}$ shown in Fig. 11(b) for the devices with and without extension increases with the slopes of 0.08 and 0.21 ps/V, respectively. The smaller slope can be attributed to

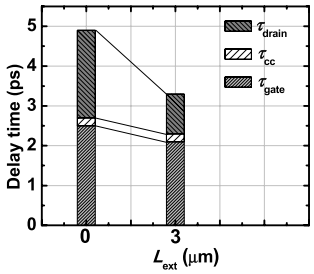
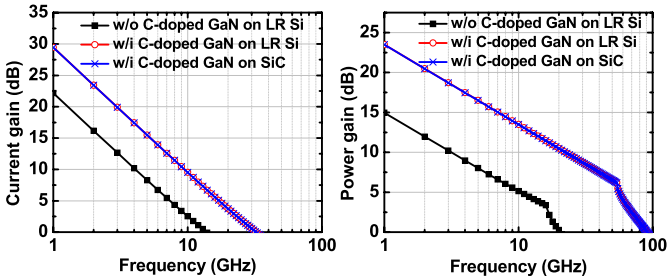



Fig. 12. Comparison of each delay component of the HEMTs with/without Schottky extension.




(a) (b)

Fig. 13. Comparison of simulated (a) Power gain and (b) Current gain for GaN HEMTs on different substrates with/without the C-doped buffer layer.

the reduced $\Delta L_G$ in the Schottky-extended devices, along with the enhanced $v_e$. The observed trend suggests that an increased drain delay at higher drain–source voltage has a significant contribution to the total delay in the reference devices, thus limits the RF performance. In contrast, the extended devices with a smaller slope promise the devices to be operated at high bias voltage but can still maintain an excellent RF performance.

Fig. 12 shows the total delay time divided into channel charging delay, drain delay, and gate delay time for the devices with $L_{\text{ext}} = 0$ $\mu$m and $L_{\text{ext}} = 3$ $\mu$m. The channel charging time is just about 4% $\sim$ 6% of the total delay time for both devices. Also, $\tau_{\text{gate}}$(16%) and $\tau_{\text{drain}}$ (54.5%) are simultaneously improved for the Schottky-extended devices. The significantly reduced $\tau_{\text{drain}}$ is due to a combination of the enhanced electron velocity and reduced width of drain depletion.

### *C. Effect of Substrate Parasitics*

The simulated TCAD results shown in Fig. 13 compare the HEMTs using GaN on LR silicon substrate and SiC substrate to investigate the parasitic loading effects from the different substrates. Note that the C-doped concentration of the GaN buffer layer is $10^{19}$ cm$^{-3}$ (similar with the case in this paper) and the buffer thickness is 4 $\mu$m for the both SiC and LR silicon substrate. As can be observed, the substrate resistivity becomes insignificant as the C-doped GaN buffer layer is inserted between the 2DEG channel and substrate, which suggests that $f_{\text{MAX}}$ and $f_T$ can be improved by using the C-doped GaN layer and become very similar to the case of SiC substrate. The result indicates that the GaN on an LR silicon substrate is suitable for RF applications if a high-resistivity interlayer is formed by the C-doped buffer layer.

Also, it can be expected that the proposed hybrid drain design should also be good for improving the performance of the GaN-on-SiC devices. To exam the dependence of the parasitic capacitance on the buffer thickness, we also performed the S-parameters analysis based on the TCAD simulation, which shows a trend of reduced $C_{\text{sub}}$ with increased buffer thickness. The thick buffer layer with C-doped GaN on silicon substrate ($\sim$4 $\mu$m in this case) results in a smaller buffer capacitance ($C_{\text{sub}}$) of $\sim$24 fF/mm compared that of $\sim$41 fF/mm with the thinner buffer layer ($\sim$1.5 $\mu$m) typically used for SiC substrate. Note that $C_{\text{sub}}$ extracted from the measurement in our small-signal model parameters as shown in Table I agrees well with $C_{\text{sub}}$ obtained by the TCAD simulation. Based on the analysis of established small-signal model, we also found that the frequency response is sensitive to $C_{\text{sub}}$ if $R_{\text{sub}}$ is relatively small. As shown in this paper, the degradation of high frequency characteristics can be alleviated with C-doped buffer to increase $R_{\text{sub}}$ although with the LR substrate. Also, we believe that a thick buffer layer with reduced $C_{\text{sub}}$ is helpful to obtain a good frequency response. It should be emphasized that $f_T \times L_G$ obtained here is 9.98 GHz $\cdot$ $\mu$m, which is comparable to the values (in a range of 9–11.4 GHz $\cdot$ $\mu$m) reported for AlGaN/GaN HEMTs on high resistivity Si substrate [1]–[3], [27].

## V. Conclusion

In this paper, the 0.2-$\mu$m line-gate AlGaN/GaN HEMTs on an LR silicon substrate for RF applications were demonstrated using the hybrid drain structure. The impacts of extended Schottky electrode on transistors were investigated in detail by dc and RF characteristics. Both the leakage current and the breakdown voltage can be improved owing to the reduced $E$-field peak intensity of hybrid drain structure. In addition, the TCAD simulation, small-signal model parameters and delay time analysis provided the insight of the physics behind the observed trends. Owing to the enhanced electron velocity and reduced width of drain depletion region, significantly improved transconductance and reduced transit time can be obtained, leading to much enhanced frequency response. With a properly designed Schottky extension of 3 $\mu$m, $f_T$ and $f_{\text{MAX}}$ can be improved up to 52.6% and 37.4% with ON–OFF ratio and $V_{\text{BK}}$ enhancements by four orders of magnitude and 80.9%, respectively.

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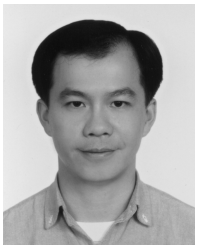

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