Drain E-Field Manipulation in AlGaN/GaN HEMTs by Schottky Extension Technology

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***Abstract*— The proposed hybrid Schottky–ohmic drain structure is analyzed in detail for AlGaN/GaN power high-electron mobility transistors on the Si substrate. Without any additional photomasks and process steps, the hybrid drain design can alter the electric field distribution to improve the breakdown voltage V_{BK}. In addition, it provides an additional current path to achieve zero onset voltage and reduce the ON-resistance. It was found that the Schottky extension L_{ext} is critical to V_{BK}, R_{ON}, and also the current collapse phenomena of the transistors. The extended Schottky electrodes for optimized transistor characteristics are investigated, and the physics behind are discussed. With an $L_{ext} \sim$ 2–3 μm, V_{BK} can be improved up to 60% with an R_{ON} degradation below 3%.**

***Index Terms*— Breakdown voltage, GaN-on-Si, high-electron mobility transistor (HEMT), leakage current, Schottky contact.**

I. Introduction

With the increasing demand of high-efficiency and compact power conversion circuits and systems, the power devices capable of low loss and high-speed operation have attracted much attention recently. The GaN-based high-electron mobility transistors (HEMTs) are a promising candidate to satisfy such requirements owing to the large bandgap ($E_g = 3.4$ eV) and high electron saturation velocity ($v_{sat} \sim 2.5 \times 10^7$ cm/s) of the material, and also high carrier density ($n \sim 1 \times 10^{13}$ cm^{-2}) in the 2-D electron gas channel in the transistor. In addition, recent progress of material engineering allows high-quality GaN layers to be grown on large-scale silicon substrates (on an 8-in wafer was reported [1]–[3]), making it possible to achieve low-cost and high-performance GaN power devices. Previous studies have shown that high-performance AlGaN/GaN HEMTs exhibit low storage charge and high $V_{BK}^2/R_{ON,SP}$ [Baliga's figure-of-merit (FoM)], which can be employed for power conversion systems to achieve high switching speed and high efficient [4]–[6].

However, one issue raised for the GaN-on-Si devices is the rapid increase of buffer leakage current when a large drain voltage is applied, which causes transistor breakdown [7]. Significant efforts on buffer growth technology of GaN-on-Si structure have been made to enhance breakdown voltage, such as increasing the buffer thickness and using compensated C- or Fe-doped buffer layers [8]–[13]. In addition to the study in material side, it has been shown that the source/drain metallic contact is also critical to device premature breakdown [14]–[16]. The alloy spikes underneath the ohmic contact could cause the undesired local E-field peaks, resulting in leakage current [17]. Different approaches of contact engineering were proposed to manipulate the E-field near contacts to improve the buffer breakdown and gate–drain breakdown, such as Si-doping [17] and Schottky contact technology [14]. The Schottky drain device exists a nonzero onset voltage V_{ON} (typical $\sim$1 V) even with recess technique, which causes the increased ON-resistance R_{ON} [14], [15]. In general, using Schottky contact to replace ohmic contact in HEMTs will encounter the problem of increased ON-resistance, but the overall performance can still be effectively improved, especially for high-voltage applications. In our previous studies, we proposed using the hybrid Schottky–ohmic drain contact to enhance breakdown voltage without obvious degradation of R_{ON} for GaN-on-Si HEMTs by manipulating the electric field distribution near the contact edge [18]. A zero V_{ON} can be also obtained.

In this paper, we further focus on the analysis and optimization of Schottky–ohmic drain design. More physical insight of the observed trends is provided, and how the E-field is manipulated around the drain electrode is explained. The transistors with various Schottky electrode extensions L_{ext} are characterized using different measurements, such as breakdown voltage, ON-resistance, and gate lag. The tradeoffs among different transistor parameters are discussed, and the design for improved overall device performance is recommended.

II. Device Design and Fabrication

The cross sections of the AlGaN/GaN HEMTs on Si substrate with the proposed hybrid ohmic–Schottky drain structure are shown in Fig. 1. The epitaxial layer of AlGaN/GaN heterostructure was grown on a 3-in Si substrate (provided by Nippon Telegraph and Telephone Corporation-Advanced Technology). The wafer consists of a 1-μm unintentionally doped (UID) layer (including buffer and GaN channel), followed by a 24-nm UID $Al_{0.25}Ga_{0.75}N$ barrier layer. The hall mobility and the sheet carrier concentration are 1519 cm^2/V$\cdot$s and 8.6×10^{12} cm^{-2} (provided by the vendor), respectively, which results in a calculated sheet resistance of 478 $\Omega/\square$.

The mesa isolation was done by inductively coupled plasma using Cl_2/Ar mixture gas with an etching depth

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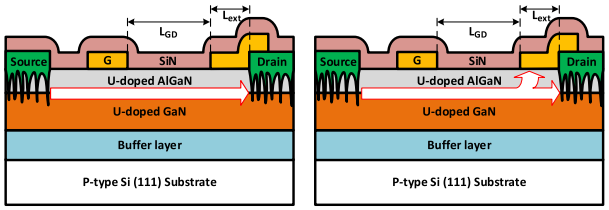

Fig. 1. ON-state current mechanism of AlGaN/GaN HEMTs with hybrid Schottky–ohmic drain. (a) When Schottky drain diode is OFF ($V_{DS} < V_{ON,SK}$), the current flows only via ohmic conduction. (b) When Schottky drain diode is ON ($V_{DS} > V_{ON,SK}$), the current via Schottky electrode rapidly increases.

of approximately 300 nm. The ohmic metal was deposited with Ti/Al/Ti/Au by e-beam evaporation and liftoff process, followed by rapid thermal annealing at 800 °C for 30 s in the N_2 ambient. The metal stack of Ni/Au was deposited to form the Schottky gate contact. Finally, a multilayer surface passivation composed of SiN/SiO/SiN was deposited by Plasma-Enhanced Chemical Vapor Deposition at 300 °C (with a total thickness of ∼0.5 μm). Note that the devices with conventional ohmic drain, pure Schottky drain, and hybrid Schottky–ohmic drain electrodes were all fabricated on the same die simultaneously and in a close proximity to ensure a fair comparison. In addition, the square-gate layout was adopted to suppress the gate leakage current and mitigate trapping effect originating from the dry etching damage at the sidewall of mesa edge [19]. It should be emphasized that the Schottky gate metal was also utilized as the Schottky drain metal by the same photomask. This self-aligned Schottky extended technique is an effective way to avoid the lateral metal overflow near the edge of drain ohmic contact during the process.

As shown in Fig. 1, the Schottky portion of the drain metal is directly deposited above the ohmic contact with an extension length L_{ext} toward the gate. The metal spikes underneath the ohmic contact are also emphasized in the figure. Note that the hybrid drain contact can be viewed as a Schottky diode in parallel connection with the ohmic contact at the drain terminal, which forms dual conductive paths and results in a nearly zero drain onset voltage. The extended Schottky drain metal has a smooth interface with the AlGaN layer, functioning similar to a Γ-shaped drain field plate. As a result, it can provide a more uniform E-field distribution at the edge of drain contact, alleviate the E-field crowding at the sharp points of the spikes, and improve V_{BK}.

III. Results and Discussion

The fabricated GaN-on-Si HEMTs are with a gate length L_G and a gate–source spacing L_{GS} both of 2 μm. The gate–drain spacing L_{GD} varies from 5 to 20 μm, but with the same total gate width of 400 μm. All the devices are depletion mode with a threshold voltage V_{TH} of ∼−3 V.

A. ON-State Characteristics

Fig. 2 compares I_{DS}–V_{DS} characteristics at $V_{GS} = 1$ V for different type devices, where L_{ext} varies from 1 to 5 μm,

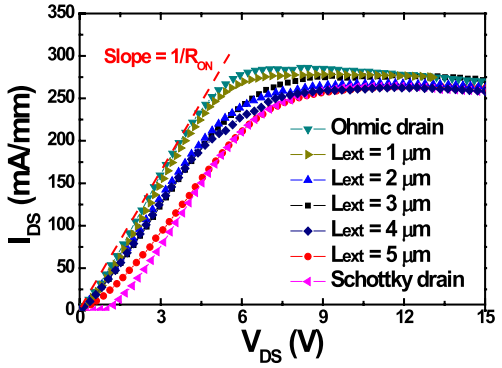

Fig. 2. Comparison of I_{DS}–V_{DS} characteristics for three types of devices with $L_{GD} = 5$ μm at $V_{GS} = 1$ V.

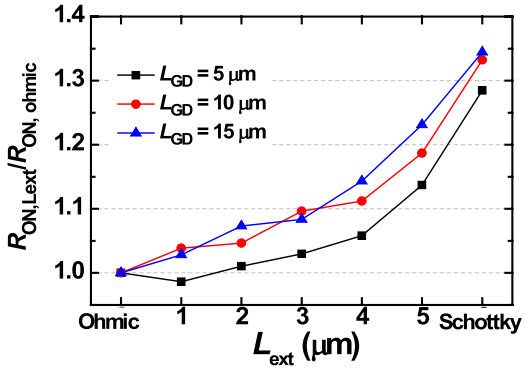

Fig. 3. Normalized R_{ON} as a function of L_{ext} for L_{GD} of 5, 10, and 15 μm.

but L_{GD} keeps identical to 5 μm. With a pure Schottky drain, the device shows a typical onset voltage of ∼1 V, and V_{ON} is zero for the conventional ohmic drain device as expected. With the additional Schottky metal in the hybrid drain transistor, zero onset voltages can also be obtained due to the dual current paths. Note that the GaN HEMTs showed $V_{ON} \sim 0.5$ V even with Schottky–ohmic drain electrode due to the additional F^- ions underneath the Schottky drain [20].

In the low V_{DS} bias region, the knee voltage gradually increases with L_{ext}, while the drain current changes in an opposite trend due to the increased voltage drop in the drift region underneath the extended Schottky electrode, as shown in Fig. 2. In addition, a dual-slope I–V characteristic in the linear region can be observed for the hybrid drain devices due to the combination of linear ohmic and nonlinear Schottky behaviors. When V_{DS} further increases to the high V_{DS} bias region, similar saturation current levels can be achieved for both Schottky drain and hybrid drain devices, compared with the ohmic drain devices. The results are consistent with [14] and [15].

The $R_{ON,sp}$ (specific ON-resistance) can be calculated from the I–V curves, as shown in Fig. 2. The active area between the source and the drain is used for $R_{ON,SP}$ calculation, where a transfer length from the source/drain pads of 1.5 μm is included. Fig. 3 shows the normalized R_{ON} (defined as $R_{ON,Lext}/R_{ON,ohmic}$) with $L_{GD} = 5$, 10, and 15 μm for the three type devices as a function of L_{ext}. Note that the $R_{ON,ohmic}$ is 1.32, 1.72, and 2.12 $m\Omega \cdot cm^2$, respectively, for the

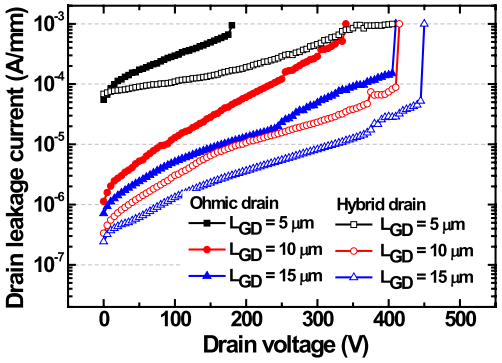

Fig. 4. OFF-state drain leakage current with $L_{ext} = 2\ \mu$m ($V_{GS} = -5$ V).

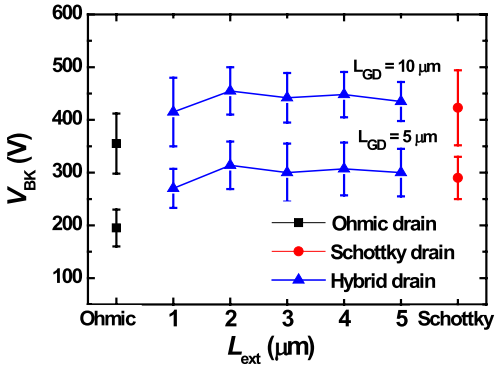

Fig. 5. Measured OFF-state breakdown voltage V_{BK} ($V_{GS} = -10$ V) as a function of the extended Schottky drain length L_{ext}.

three different L_{GD}. Based on the measured results from the Transmission Line Model test, the contact resistance R_C is in the range of 1–2 $\Omega \cdot$mm, which is one important factor for the observed relatively high ON-resistance.

The ON-resistance increases with L_{ext} from the pure ohmic drain devices (i.e., $L_{ext} = 0$) toward the pure Schottky drain devices. It should be pointed out that $R_{ON,sp}$ increases relatively slow with smaller L_{ext}. However, the increase of $R_{ON,sp}$ becomes more significant as L_{ext} increases up to ~4–5 μm. For example, the degradation of R_{ON} in the hybrid drain devices ($L_{GD} = 5\ \mu$m) is kept below 3% as $L_{ext} \leq 3\mu$m, whereas that increases up to ~13% as L_{ext} becomes 5 μm. This trend is similar for devices with $L_{GD} = 10$ and 15 μm. As the Schottky drain portion of the total electrode increases, more E-field lines will concentrate on the Schottky drain metal, and the ratio of Schottky conduction in the total drain current gradually becomes dominant. In addition, the effective drift length is increased ($L_{drift,eff} = L_{ext} + L_{GD}$) for ohmic conduction. Both factors lead to increased channel resistance and knee voltage. Once the Schottky extension L_{ext} exceeds a certain length, the E-field lines across the ohmic contact are shielded effectively. As a result, the decreased ohmic current and increased knee voltage and hence R_{ON} become more significant. The result suggested that the design parameter L_{ext} should be kept relatively small to prevent significant R_{ON} degradation.

B. OFF-State Characteristics

The OFF-state breakdown voltage V_{BK} (defined by the drain current at 1 mA/mm) and I_{DS}–V_{DS} curves were measured under the three-terminal condition with a floated substrate in the Fluorinert liquid. Fig. 4 shows the leakage current of the ohmic drain and hybrid drain ($L_{ext} = 2\ \mu$m) devices with three different L_{GD}. Compared with the ohmic drain devices, the hybrid drain structure can suppress the drain leakage current by about one order of magnitude. Fig. 5 shows the dependence of measured V_{BK} (at $V_{GS} = -10$ V) on L_{ext} for $L_{GD} = 5$ and 10 μm, and also the results of pure ohmic and Schottky drains (average from three typical devices with the error bar shown). With $L_{ext} = 2\ \mu$m, V_{BK} can be improved by ~119 V (60%) and ~100 V (28%) for $L_{GD} = 5$ and 10 μm, respectively. The enhanced V_{BK} of the hybrid drain devices will eventually saturated as $L_{ext} \geq 3\ \mu$m, and the value is similar to that of the pure Schottky drain devices. With the optimized extended length ($L_{ext} = 2$–3 μm in this experiment), the twin peaks of E-field at the edge of Schottky drain metal and at the sharp point of spike around the edge of ohmic contact can be somehow balanced, which leads to the highest improvement of V_{BK}. Although not shown in Fig. 5, the devices with $L_{GD} = 15$ and 20 μm have a similar improvement in V_{BK} of ~30 V compared with the ohmic drain devices.

The measured results suggest that the device breakdown is dominated by the gate leakage current (gate–drain breakdown) in the devices with a relatively small L_{GD} (i.e., L_{GD} of 5 and 10 μm). As the device becomes limited by the buffer leakage, i.e., V_{BK} saturates even with further increased L_{GD}, improved V_{BK} can still be observed in the hybrid drain devices but not as significant. The results imply that the lateral E-field between the gate and drain electrodes does not dominant V_{BK} anymore. Instead, the vertical E-fields between the contact electrodes and the substrate at both source/drain sides determine the breakdown voltage. However, the manipulated E-field around the drain side with alleviated E-field peak values around the spikes can still help to suppress the buffer leakage to a certain extent, and therefore the devices still show an improved breakdown voltage even when $L_{GD} \geq 15\ \mu$m. Although the V_{BK} of the GaN-on-Si devices will eventually be limited by the buffer, the proposed hybrid drain design demonstrates a significantly improved device breakdown voltage with only slightly increased R_{ON} before the device reaching the buffer breakdown limitation. It should be emphasized that this approach can also work for devices to achieve higher breakdown voltages if a thicker buffer is employed, which has been demonstrated in [18] with a 4.8 μm buffer thickness.

Fig. 6 plots the measured V_{BK} versus $R_{ON,SP}$ of the three types of devices with $L_{ext} = 2\ \mu$m. Compared with the ohmic drain devices, the hybrid drain devices with $L_{ext} = 2\ \mu$m achieve 60% and 28% improvements in V_{BK} with small degradations of 1.3% and 4.4% in R_{ON} for $L_{GD} = 5$ and 10 μm, respectively. Fig. 7 compares the Baliga's FoM of this paper with the previously published GaN-based devices [3], [14], [20], [21]. The FoM of the proposed devices can be further improved by optimization of the contact resistance and also with improved epitaxial layer quality of lower sheet resistance.

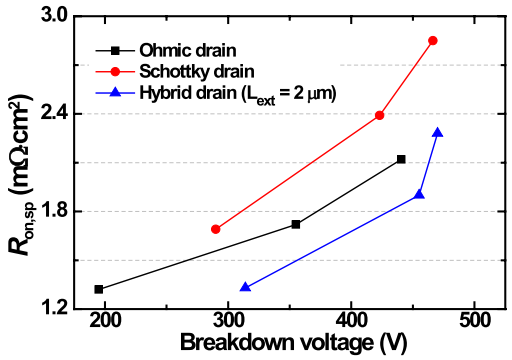

Fig. 6. Measured V_{BK} versus $R_{ON,sp}$ of the Schottky drain, ohmic drain, and hybrid drain devices with $L_{ext} = 2$ μm and $L_{GD} = 5$, 10, and 15 μm for comparison.

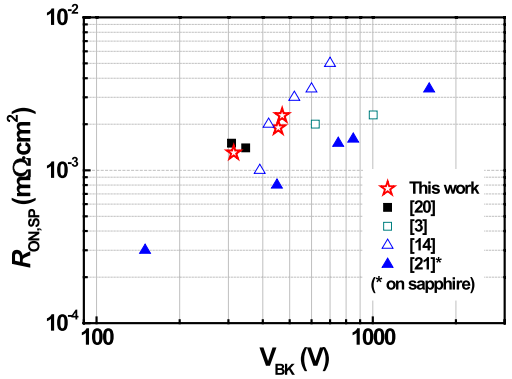

Fig. 7. Comparison of the FoM ($V_{BK}^2/R_{ON,sp}$) for the proposed hybrid drain devices ($L_{ext} = 2$ μm and $L_{GD} = 5$, 10, and 15 μm) with other GaN-based devices in the previous publications.

C. Gate-Lag Measurements

The current collapse characteristics and surface trapping effects for AlGaN/GaN HEMTs with different drain electrode structures were investigated by gate-lag measurements using the Tektronics curve tracer 370B. It is important to investigate the impact of hybrid drain design on trapping effect and current collapse, which is closely related to device reliability [22]. Two different gate pulsewidths of 80 and 300 μs were applied for the measurements (default values available from the curve tracer). The gate voltage was pulsed from -5 V ($\sim V_{TH} - 2$ V) to 1 V, and the drain voltage V_D was applied within 16 V under a fixed power compliance. To avoid the complications of device self-heating effect at high V_{DS}, the normalized R_{ON} is used to analyze the surface trapping effect in these measurements. The normalized R_{ON} is defined as $R_{ON,pulse}/R_{ON,DC}$, where $R_{ON,pulse}$ is obtained at $V_{GS} = 1$ V.

Fig. 8 shows the dependence of normalized R_{ON} on L_{ext}. As can be observed, the ohmic drain device shows a relatively small current collapse phenomenon. On the other hand, the reduction of drain current in the linear region and shift of the knee voltage can be clearly observed for the Schottky drain devices leading to a much increased R_{ON} dispersion. In addition, the trend becomes more obvious as the pulsewidth reduces. Note that the gate lag with a relatively small V_D was used to investigate the surface trapping effect for devices with

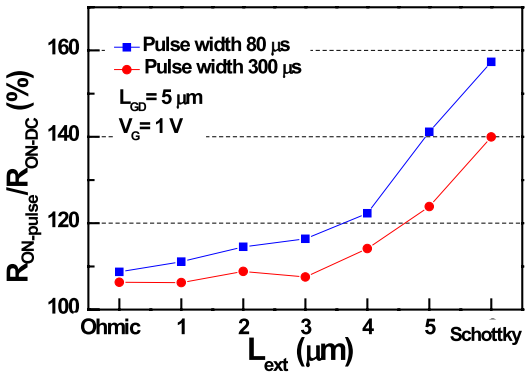

Fig. 8. Normalized R_{ON} versus L_{ext} in pulsewidths of 80 and 300 μs.

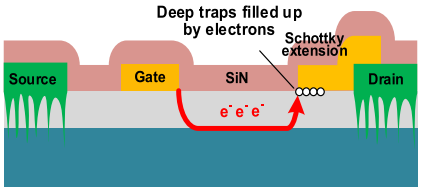

Fig. 9. Location of surface traps in hybrid drain devices responsible for the observed current collapse when the device is in OFF-state.

three different drain contacts. It is believed that the drain lag or gate lag under a higher drain bias condition is more sensitive to the deep traps near the buffer layer [23]. Similarly, it has been reported that the dynamic R_{ON} is mainly related to the trapping states in the buffer layer [24], [25], and hence it is strongly dependent on the drain voltage. In this paper, the devices are all with the same buffer layer but different metal/GaN interface in the drain side. It is reasonable to exam the gate-lag effect with a relatively small drain voltage to identify the impact of various drain contacts on surface trapping effects.

In typical AlGaN/GaN HEMTs, the surface trapping effect mainly comes from the surface traps in the gate–drain drift region and/or underneath Schottky gate, which can be mainly attributed to the issue of surface passivation and the locations of peak E-field. The measured results of conventional ohmic drain devices indicate that the contribution of traps in the gate–drain region and those underneath the Schottky gate are not significant, which may be attributed to the careful passivation process in our devices. The results suggest that the main location of traps should be at around the Schottky drain contact, as shown in Fig. 9. Note that the asymmetric band diagram for electrons injection due to different gate and drain bias conditions could be responsible for the occurrence of trapping effects in the drain Schottky electrode instead of the Schottky gate in these devices, considering both electrodes are processed at the same time and the process variation is not an issue here. It should be mentioned that the dispersion of $R_{ON-Pulse}$ becomes more significant as L_{ext} increases up to $\sim$4–5 μm. This trend is similar with the dependence of $R_{ON,DC}$ on L_{ext} (Fig. 3), which may also be attributed to the manipulated E-field around the hybrid drain contact. Once L_{ext} exceeds a certain value, in addition to the drain-side gate edge, the high E-field also occurs at the edge of Schottky

drain extension. The high E-field region can easily induce severe surface trapping effect, since the carriers sufficiently gain high energy and jump into the deep-level traps. The trapping effects in the Schottky drain or a hybrid drain structure have not been clearly discussed in previous studies. With also a hybrid Schottky–ohmic drain electrode but F^- ion implemented in the channel, Zhou *et al.* [20] reported that the devices did not show adverse effects in current collapse, compared with conventional HEMTs.

IV. Conclusion

In this paper, the hybrid Schottky–ohmic drain structure in GaN-on-Si HEMTs was analyzed in detail. The effects of extended Schottky electrode on transistor characteristics were investigated by various transistor parameters, such as $R_{\rm ON}$, $V_{\rm BK}$, and leakage current. In addition, the correlation between the extended Schottky drain and the trapping effects was examined by gate-lag measurements. The physics behind the observed trends were explained and discussed. The results suggested that $L_{\rm ext}$ of 2–3 μm was the optimized design for the most improved transistor performance. Without any additional photomasks and process steps, the hybrid drain design forms a Γ-shaped electrode to improve the breakdown voltage up to 60% with only 3% $R_{\rm ON}$ degradation.

References

[1] K. Cheng *et al.*, "AlGaN/GaN/AlGaN double heterostructures grown on 200 mm silicon (111) substrates with high electron mobility," *Appl. Phys. Exp.*, vol. 5, no. 1, pp. 011002-1–011002-3, Dec. 2011.

[2] A. R. Boyd *et al.*, "Growth of GaN/AlGaN on 200 mm diameter silicon (111) wafers by MOCVD," *Phys. Status Solidi C*, vol. 6, no. S2, pp. S1045–S1048, Jan. 2009.

[3] D. Christy *et al.*, "Uniform growth of AlGaN/GaN high electron mobility transistors on 200 mm silicon (111) substrate," *Appl. Phys. Exp.*, vol. 6, no. 2, pp. 026501-1–026501-4, Jan. 2013.

[4] B. Huges, Y. Y. Yoon, D. M. Zehnder, and K. S. Boutros, "A 95% efficient normally-off GaN-on-Si HEMT hybrid-IC boost-converter with 425-W output power at 1 MHz," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp.*, Oct. 2011, pp. 1–3.

[5] Y. Wu, M. Jacob-Mitos, M. L. Moore, and S. Heikman, "A 97.8% efficient GaN HEMT boost converter with 300-W output power at 1 MHz," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 824–826, Aug. 2008.

[6] K. S. Boutros *et al.*, "Normally-off 5 A/1100 V GaN-on-silicon device for high voltage applications," in *Proc. IEEE IEDM*, Dec. 2009, pp. 1–3.

[7] Z. Tang, S. Huang, Q. Jiang, S. Liu, C. Liu, and K. J. Chen, "600 V 1.3m$\Omega\cdot$cm^2 low leakage low current collapse AlGaN/GaN HEMTs with AlN/SiN_x passivation," in *Proc. 25th Int. Symp. Power Semiconductor Devices IC's*, May 2013, pp. 191–194.

[8] S. L. Selvaraj, T. Suzue, and T. Egawa, "Breakdown enhancement of AlGaN/GaN HEMTs on 4-in silicon by improving the GaN quality on thick buffer layers," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 587–589, Jun. 2009.

[9] I. B. Rowena, S. L. Selvaraj, and T. Egawa, "Buffer thickness contribution to suppress vertical leakage current with high breakdown field (2.3 MV/cm) for GaN on Si," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1534–1536, Nov. 2011.

[10] S. Iwakami *et al.*, "20 mΩ, 750 V high-power AlGaN/GaN heterostructure field-effect transistors on Si substrate," *Jpn. J. Appl. Phys.*, vol. 46, pp. L587–L589, Jun. 2007.

[11] A. Able, W. Wegscheider, K. Engl, and J. Zweck, "Growth of crack-free GaN on Si(111) with graded AlGaN buffer layers," *J. Crystal Growth*, vol. 276, nos. 3–4, pp. 415–418, 2005.

[12] C. Poblenz, P. Waltereit, S. Rajan, S. Heikman, U. K. Mishra, and J. S. Speck, "Effect of carbon doping on buffer leakage in AlGaN/GaN high electron mobility transistors," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 22, no. 3, pp. 1145–1149, May 2004.

[13] Y. C. Choi, M. Pophristic, H.-Y. Cha, B. Peres, M. G. Spencer, and L. F. Eastman, "The effect of an Fe-doped GaN buffer on off-state breakdown characteristics in AlGaN/GaN HEMTs on Si substrate," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2926–2931, Dec. 2006.

[14] B. Lu, E. L. Piner, and T. Palacios, "Schottky-drain technology for AlGaN/GaN high-electron mobility transistors," *IEEE Electron Device Lett.*, vol. 31, no. 4, pp. 302–304, Apr. 2010.

[15] E. Bahat-Treidel, R. Lossy, J. Würfl, and G. Tränkle, "AlGaN/GaN HEMT with integrated recessed Schottky-drain protection diode," *IEEE Electron Device Lett.*, vol. 30, no. 9, pp. 901–903, Sep. 2009.

[16] Q. Zhou *et al.*, "Schottky-contact technology in InAlN/GaN HEMTs for breakdown voltage improvement," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 1075–1081, Mar. 2013.

[17] Y. Dora *et al.*, "Effect of ohmic contacts on buffer leakage of GaN transistors," *IEEE Electron Device Lett.*, vol. 27, no. 7, pp. 529–531, Jul. 2006.

[18] Y.-W. Lian, Y.-S. Lin, H.-C. Lu, Y.-C. Huang, and S. S. H. Hsu, "AlGaN/GaN HEMTs on silicon with hybrid Schottky–ohmic drain for high breakdown voltage and low leakage current," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 973–975, Jul. 2012.

[19] Y.-S. Lin, J.-Y. Wu, C.-Y. Chan, S. S. H. Hsu, C.-F. Huang, and T.-C. Lee, "Square-gate AlGaN/GaN HEMTs with improved trap-related characteristics," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 3207–3211, Dec. 2009.

[20] C. Zhou, W. Chen, E. L. Piner, and K. J. Chen, "Schottky-ohmic drain AlGaN/GaN normally off HEMT with reverse drain blocking capability," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 668–670, Jul. 2010.

[21] N. Tipirneni, A. Koudymov, V. Adivarahan, J. Yang, G. Simin, and M. A. Khan, "The 1.6-kV AlGaN/GaN HFETs," *IEEE Electron Device Lett.*, vol. 27, no. 9, pp. 716–718, Sep. 2006.

[22] J. Joh, J. A. del Alamo, and J. Jimenez, "A simple current collapse measurement technique for GaN high-electron mobility transistors," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 665–667, Jul. 2008.

[23] W. Mickanin, P. Canfield, E. Finchem, and B. Odekirk, "Frequency-dependent transients in GaAs MESFETs: Process, geometry and material effects," in *Proc. IEEE GaAs IC Symp.*, Oct. 1989, pp. 211–214.

[24] G. Verzellesi *et al.*, "Influence of buffer carbon doping on pulse and AC behavior of insulated-gate field-plated power AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 443–445, Apr. 2014.

[25] M. J. Uren *et al.*, "Intentionally carbon-doped AlGaN/GaN HEMTs: Necessity for vertical leakage paths," *IEEE Electron Device Lett.*, vol. 35, no. 3, pp. 327–329, Mar. 2014.

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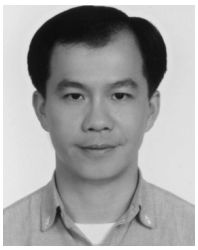

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