101-GHz InAlN/GaN HEMTs on Silicon With High Johnson's Figure-of-Merit

Chuan-Wei Tsou, Chen-Yi Lin, Yi-Wei Lian, and Shawn S. H. Hsu, *Member, IEEE*

***Abstract*— In this brief, the InAlN/GaN high-electron mobility transistors (HEMTs) on silicon substrate with high Johnson's figure-of-merit (J-FOM) are presented. A trilayer photoresist of polymethylmethacrylate (PMMA)/copolymer/PMMA associated with a T-shaped gate is used to reduce the parasitic resistance while maintaining high current gain cutoff frequency. The small dc-to-RF transconductance dispersion of only 1.1% suggests a good quality SiN_x passivation layer, and the f_{MAX} of 101 GHz and f_T of 60 GHz can be simultaneously obtained with a 0.11-μm foot length and 1.5-μm source–drain distance. In addition, the three-terminal OFF-state breakdown measurements reveal a source–drain breakdown voltage (BV_{DS}) of 21 V (V_{DG} = 31 V). The results lead to a high J-FOM of 1.3 THz · V, which has not been reported for the InAlN/GaN HEMTs on silicon substrate.**

***Index Terms*— Gallium nitride (GaN), high-electron mobility transistors (HEMTs), InAlN, Johnson's figure-of-merit (J-FOM), silicon.**

I. Introduction

IN RECENT years, gallium nitride (GaN) has attracted much attention for various applications due to the wide bandgap and high electron saturation velocity, which make it possible to achieve high speed and high breakdown voltage (BV) operation simultaneously. The AlGaN/GaN high-electron mobility transistors (HEMTs) on silicon substrate with excellent microwave performance and large BV have been reported [1]–[4]. The epitaxial structures with an Al-rich barrier layer such as AlN/GaN [5] and $In_xAl_{1-x}N$/GaN [6]–[8] can have high polarization-induced electric field, allowing for high current density and large aspect ratio of $L_G/T_{barrier}$ (gate length/barrier layer thickness) [9]. In addition, the lattice-matched heterostructure of $In_{0.17}Al_{0.83}N$/GaN can produce high spontaneous polarization and unstrained barrier, which leads to improved device reliability [10], [11].

Various substrates have been applied to the GaN-based heterosturcture, including sapphire, silicon carbide (SiC), and silicon (Si). Compared with SiC, the Si substrate offers low cost, availability of large-area wafers, and well-established processing techniques. In addition, the GaN-on-Si devices promise the potential to be combined with CMOS technologies [12]. Table I summarizes the recent advances of InAlN/GaN HEMTs with T-shaped gate on different substrates. As can be seen, InAlN/GaN HEMTs on SiC with f_T and f_{MAX} > 300 GHz and BV of 11 V have been achieved [13]. High power gain and current gain cutoff frequencies (f_T/f_{MAX} = 114/177 GHz) with the BV of 95 V were also demonstrated in InAlN/GaN heterostructure on SiC [14]. In addition, InAlN/GaN HEMTs grown on silicon with f_T of 102 GHz and f_{MAX} of 104 GHz have been reported [16]. A combined result of 143 GHz f_T and 176 GHz f_{MAX} in InAlN/GaN HEMTs on silicon has also been published [17]. While the InAlN/GaN HEMTs on silicon showed a comparable microwave performance to that of InAlN/GaN HEMTs on SiC, less attention has been given to the breakdown characteristics. In the case of lateral access region scaling for high-speed applications, GaN-based HEMTs generally encounter a tradeoff between the increased operating speed and sacrificed BV, which limits the high power applications, such as the power amplifier at microwave frequencies (0.3–300 GHz).

TABLE I
RECENT ADVANCES OF InAlN/GaN HEMTs WITH T-SHAPED GATE ON DIFFERENT SUBSTRATES

Ref.	Sub.	L_G (nm)	f_T (GHz)	BV (V)	$f_{MAX(U)}$ (GHz)	$f_T \times BV$ (THz·V)	$f_{MAX(U)} \times L_G$ (GHz·μm)
[13]	SiC	27	302	11.8	301	3.6	8.1
[14]	SiC	80	114	95	177	10.8	14.2
[15]	SiC	55	205	-	191	-	10.5
[16]	Si	100	102	-	89	-	8.9
[17]	Si	80	143	-	176	-	14.1
[18]	Si	170	64	-	72	-	12.2
This work	Si	110	60	21	101	1.3	11.1

In this brief, we demonstrate the InAlN/GaN HEMTs on silicon with T-gate for simultaneously achieving high f_{MAX} and high Johnson's figure-of-merit (J-FOM), which has not been discussed previously for the InAlN/GaN HEMTs on silicon substrate. The details of dc-to-RF transconductance dispersion and possible breakdown mechanism are also analyzed.

II. Device Fabrication

The epitaxial layer as shown in Fig. 1(a) was grown by Metalorganic Chemical Vapor Deposition on high resistivity (>6000 Ω · cm) silicon substrate (provided by NTT Advanced Technology Corporation). The layer consists of a 1.2-μm Unintentional Doped (UID) layer (including buffer and GaN channel) and followed by a 1-nm AlN spacer layer

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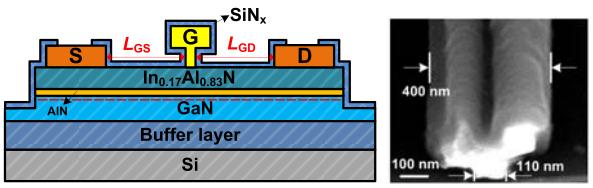
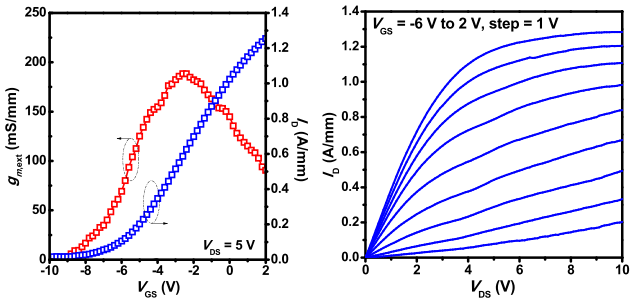


(a) (b)

Fig. 1. (a) Cross section of the InAlN/GaN HEMTs on silicon. (b) SEM micrograph of the T-gate.



(a) (b)

Fig. 2. Measured dc characteristics of InAlN/GaN HEMT with a gate width of (2 × 12.5) μm (a) I_D and extrinsic g_m ($g_{m,\mathrm{ext}}$) with V_{GS} varied from −10 to 2 V. (b) I_D versus V_{DS} with V_{GS} varied from −6 to 2 V.

and a 12-nm UID $In_{0.17}Al_{0.83}N$ barrier layer. The ohmic contact was first fabricated with the optimized recess time of 3 min (etching rate ∼3 nm/min) to reduce the contact resistance, and followed by metal deposition of Ti/Al/Ni/Au (15/100/40/50 nm) using e-gun evaporation and then followed by rapid thermal annealing at 800 °C for 30 s in N_2 ambient. After ohmic contact formation, mesa isolation was performed using dry etching with chloride-based gas for an etching depth of 100 nm. The trilayer photoresist of polymethylmethacrylate (PMMA)/copolymer/PMMA was coated to define the T-shaped gate with two different doses, followed by the metal deposition of Ni/Au (30/300 nm) and liftoff process. The sample was then immersed in dilute HCl:H_2O (1:10) for 50 s, followed by Deionized water for 10 s prior to SiN_x passivation. Plasma Enhanced Chemical Vapor Deposition SiN_x of 80 nm was then deposited at 300 °C. After passivation, the sample was selectively etched using reactive ion etching with CHF_3/O_2 mixture gas for pad opening. Finally, a pad connection for RF measurement was deposited with the metal stack of Ti/Au. The contact resistance R_c of 0.36 Ω · mm and the sheet resistance R_{sh} of 365 Ω/□ were measured by the transmission line method after passivation. The source–drain distance (L_{SD}) and gate–drain distance (L_{GD}) were 1.5 and 0.7 μm, respectively.

III. Results and Discussion

The dc characteristics of fabricated InAlN/GaN HEMTs were measured using the Agilent B1500A semiconductor device analyzer. The T-gate with a 0.11-μm foot and 0.4-μm head was examined by SEM, as shown in Fig. 1(b). Fig. 2 shows the measured I–V curves (I_D–V_{GS} and I_D–V_{DS}) and extrinsic transconductance ($g_{m,\mathrm{ext}}$) characteristics. As shown in Fig. 2(a), the device exhibits a maximum drain current density of 1.25 A/mm at $V_{\mathrm{GS}} = 2$ V and an extrinsic peak $g_{m,\mathrm{ext}}$ of 189 mS/mm at $V_{\mathrm{GS}} = -2.5$ V.

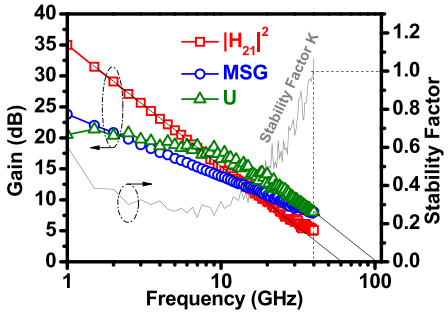


Fig. 3. Measured microwave characteristics of InAlN/GaN HEMT at $V_{\mathrm{DS}} = 5$ V and $V_{\mathrm{GS}} = -2$ V.

TABLE II
Small-Signal Model Parameters of the InAlN/GaN HEMT

Extrinsic parameters	C_{pad} (fF)	30	R_G (Ω·mm)	0.06
	R_D (Ω·mm)	1.03	L_G (pH)	10
	R_S (Ω·mm)	0.98		
Intrinsic parameters	Intrinsic g_m ($g_{m,\mathrm{int}}$) (mS/mm)	220	G_{DS} (mS/mm)	28.4
	C_{GS} (fF/mm)	660	R_i (Ω·mm)	3.6
	C_{GD} (fF/mm)	110	τ (ps)	1.1
	C_{DS} (fF/mm)	40		

An ON-resistance (R_{on}) of 2.5 Ω · mm was extracted at $V_{\mathrm{GS}} = 2$ V, as shown in Fig. 2(b).

The small-signal microwave measurements were performed using the Agilent E8361C PNA network analyzer. The system was calibrated with a short-open-load-thru calibration method. Fig. 3 shows the measured current gain and power gain versus frequency range of 1–40 GHz at the bias of $V_{\mathrm{GS}} = -2$ V and $V_{\mathrm{DS}} = 5$ V. The deembedded f_T of 60 GHz and f_{MAX} of 101 GHz was extracted by extrapolation with a −20 dB/decade roll-off. The product of $f_{\mathrm{MAX(U)}} \times L_G$ is 11.1 GHz · μm, which is slightly lower than that reported in the InAlN/GaN HEMT on silicon substrate [18]. Table II summarizes the extracted parameters of small-signal model from the cold-FET and hot-FET measurements [19]. The calculated f_T and f_{MAX} based on the model are 59.4 and 100.4 GHz, respectively, which shows an excellent agreement with the measured results

$$g_{m,\mathrm{ext}} = \frac{g_{m,\mathrm{int}}}{1 + g_{m,\mathrm{int}} \cdot R_S}. \quad (1)$$

The dc-to-RF dispersion of transconductance can be analyzed according to (1). The calculated RF $g_{m,\mathrm{ext}}$ based on the small-signal model is 181 mS/mm for the HEMT biased at $V_{\mathrm{GS}} = -2$ V and $V_{\mathrm{DS}} = 5$ V, which is very close to the measured dc $g_{m,\mathrm{ext}}$ of 183 mS/mm at the same bias, as shown in Fig. 2(a). The result indicates that the dc-to-RF dispersion is only 1.1%. The intrinsic gate capacitance $C_G (= C_{\mathrm{GS}} + C_{\mathrm{GD}})$ extracted from the small-signal model is 19.3 fF. On the other hand, the calculated value based on $C_G = \varepsilon_{r(\mathrm{InAlN})} \times \varepsilon_0 \times L_G \times W_G / T_{\mathrm{barrier}}$ is 18.3 fF, which is also very close to the extracted result. The values of $\varepsilon_{r(\mathrm{InAlN})}$ and T_{barrier} used here are 9.8 and 13 nm [20], respectively, and $L_G \times W_G$ corresponds to the gate contact area. Owing to the very small dc-to-RF dispersion, the f_T of 60 GHz is achieved even with a relatively low dc $g_{m,\mathrm{ext}}$. In addition, a high f_{MAX}/f_T ratio can be obtained, suggesting the low gate resistance and high $C_{\mathrm{GS}}/C_{\mathrm{GD}}$ ratio.

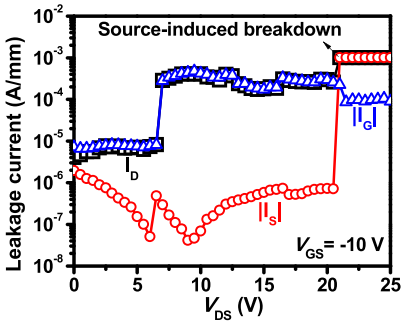


Fig. 4. Measured three-terminal OFF-state breakdown characteristics at $V_{GS} = -10$ V for the HEMT with $L_{GD} = 0.7$ μm.

Fig. 4 shows the measured three-terminal OFF-state breakdown characteristics of the device with L_{GD} of 0.7 μm. The definition of BV is at the gate or drain leakage current reaches 1 mA/mm. No gate–drain breakdown was observed even with V_{DG} up to 31 V, suggesting the passivation layer is with good quality. This may also be the reason for small dc-to-RF dispersion. The source-induced breakdown occurs when V_{DS} exceeds 21 V, which indicates that the electrons could inject from the source to the high field region (under the gate edge on the drain side) through the buffer layer. This could induce impact ionization in the channel at large drain bias [21]. Therefore, the rapid increase of source and drain leakage current can be observed simultaneously. The influence of buffer can also be observed by the decreased source leakage current. Due to the dislocations and crystal imperfections, especially for GaN-on-Si devices [22], the decreased source leakage current could be attributed to the trapped electrons in the buffer, forming a space charge region and then blocking the flow of electrons toward the buffer. Once the trap states were filled up completely, the electrons can flow through the buffer and the source leakage current increases gradually until breakdown. It has been reported that the BV can be improved if the buffer conductivity is reduced [16]. In addition, we observe that the gate leakage current dominates the overall leakage current before the hard breakdown occurs, and a soft breakdown occurred when V_{DS} is >7 V (V_{DG} > 17 V). The use of a gate-insulating layer on the top of the InAlN barrier layer is a potential solution to this problem. In addition, the preSiN treatment of surface might be effective to suppress the leakage current [23]. With a source–drain BV (BV_{DS}) of 21 V, a J-FOM of 1.3 THz·V can be achieved using the product of $f_T \times BV_{DS}$.

IV. Conclusion

The InAlN/GaN HEMTs on silicon with high J-FOM have been reported. A high f_{MAX} of 101 GHz and a high f_T of 60 GHz were simultaneously achieved. The dc-to-RF transconductance dispersion and breakdown mechanism were also discussed, which exhibited a dispersion of only 1.1% and a source-induced BV of 21 V. The combination of f_T and BV_{DS} yields a J-FOM of 1.3 THz·V, which has not been reported and discussed for the InAlN/GaN HEMTs on silicon substrate.

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