Fully Symmetric 3-D Transformers With Through-Silicon via IPD Technology for RF Applications

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***Abstract*— This article presents the design, characterization, and modeling for the novel 3-D transformer structures based on the in-house developed 3-D integrated circuit (3-D IC) via-last backside-through-silicon via (TSV) interposer process. Differing from the conventional 2-D planar structure, the 3-D TSV design allows achieving a fully symmetric transformer with a compact size. The equivalent circuit model parameters are extracted based on the S-parameters to investigate the design tradeoff. With an inner diameter of 40 μm in the 3-D 1:1 transformer, the measured inductances of the primary and second coils are 439 and 482 pH with the Q factors of 4.59 and 5.11, respectively, and the coupling coefficient is 0.136.**

***Index Terms*— 1:N transformer, 3-D, heterogeneous integration, integrated passive device (IPD), interposer, symmetry, through-silicon via (TSV).**

I. Introduction

THE 3-D integrated circuit (3-D IC) technology is an attractive approach for the emerging microelectronics applications, which enables heterogeneous integration for complex functions with a compact form factor. The 3-D IC technology provides a promising solution in the "More than Moore" era. Various types of chips can be designed individually using the most appropriate front-end-of-line (FEOL) process to complete the circuits or even systems. By using the through-silicon via (TSV), micro bump, redistribution metal layer (RDL), and other back-end-of-line (BEOL) technologies to integrate different chips, 3-D ICs can achieve heterogeneous integration of sensors, memory, power management, and various analog and digital ICs, as shown in Fig. 1. Using 3-D stacking configuration not only can shorten the metal wires between the chips to reduce the parasitic effects for high-speed operation but can also minimize the overall footprint, leading to the subsystems/systems with high integration level, high efficiency, low power consumption, and low fabrication cost [1]–[10].

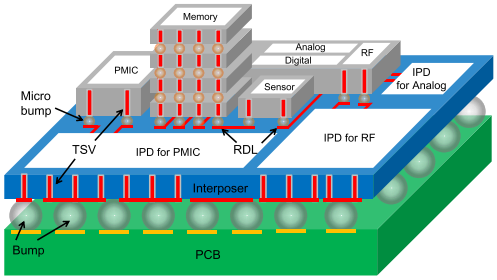

Fig. 1. Conceptual plot of heterogeneous 3-D IC integration with an interposer IPD.

Using the traditional FEOL process, the passive elements, such as resistor, inductor, and capacitor, can be realized. These on-chip lumped elements can achieve highly integrated subsystems. However, as the gate length of transistor keeps scaling down, the cost per unit chip area increases significantly. Integration of the area consuming passive elements with the active transistors becomes an issue in the advanced CMOS technology, especially the inductive components for RF applications. One attractive solution is to separate the process of passive elements in a different substrate as the integrated passive device (IPD) technology. Fig. 1 also shows the advantages of using the 3-D IC TSV interposer process, which allows minimizing the more expensive FEOL area by integrating the passive elements with the IPD process. As a result, a low-cost and compact 3-D IC can be achieved with a complex functionality [1]–[10].

The transformer is a crucial passive component in many RF integrated circuit (RFIC) applications, which has been widely used for the design of filters, baluns [11], [12], couplers, matching networks for the low-noise amplifiers (LNAs) [13], [14], voltage-controlled oscillators (VCOs) [15]–[17], and power amplifiers (PAs) [18]–[20]. Compared with the discrete inductors, the on-chip transformers offer the advantages of large inductance density, de-coupled dc signal, and high design flexibility; also, transformers are suitable for the circuits operating with the differential signal. With the increasing demand for low-voltage and low-power operations of circuits

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and systems, the signal level becomes relatively small, which is more vulnerable to noise interference. The transformers can be easily accommodated to the RFICs with a differential topology for improved noise immunity. The metrics for transformers in practical design include coil inductance, quality factor, turns ratio, coupling coefficient, self-resonant frequency (SRF), and area [21]. In addition, the metrics of the transformer-based baluns and filters consist of bandwidth, insertion loss, return loss, stopband rejection, and area [11], [22]. In general, area is a major concern in practical IC implementation, which is the main advantage of the proposed 3-D TSV approach. However, one challenge remains in the proposed 3-D TSV transformer is the relatively low coupling coefficient, which is limited by the design rules of the technology. With a conventional 2-D spiral transformer on the silicon substrate, a coupling coefficient up to ∼0.8 can be achieved, which is considerably higher than the 3-D TSV transformer reported here. More details will be elaborated in Sections III and IV.

The on-chip transformers can be implemented in the standard IC processes by utilizing multiple metal layers [23]–[29]. Due to the different thicknesses of the metal layers, it is difficult to realize a truly symmetric transformer in the typical silicon-based IC process. The imbalance in the two signal paths can cause not only the above-mentioned noise rejection problem but also the phase delay difference for the differential signal. These concerns will become more serious as the operating frequency increases, and also, the planar structure of the conventional on-chip transformer design makes it difficult to achieve a compact size. Efforts have been made to improve the symmetry of the transformer in the conventional planar IC process [23]–[27]. Previous studies reported the 3-D transformer by combining two 3-D solenoid inductors with the 3-D vertical front and backside RDL trace and complete TSV windings [28], [29]. However, the reported 3-D transformers are still not completely symmetric and difficult to be integrated with practical differential circuits. In addition, the size of the transformer is still relatively large.

In this article, we propose novel fully symmetrical 3-D transformer structures using the IPD process in the silicon substrate with TSV. Two 3-D structures are demonstrated for the fully symmetric 1:1 and 1:N transformers, which can be operated in a wide bandwidth with a compact chip size. This article is organized as follows. Section II describes the in-house developed 3-D IC TSV interposer process for the proposed transformers. Section III introduces the design details of the 3-D transformers. Section IV presents the parameter extraction of equivalent circuit model and the comparison among electromagnetic (EM) simulation, measurement, and model of the proposed 3-D transformers. Section V concludes this article.

II. 3-D Interposer Process With TSV

Fig. 2 shows the process flow of the proposed 3-D transformer based on a via-last backside-TSV interposer technology. The silicon oxide/silicon nitride as the front-side interlayer dielectric (ILD) layer is deposited on the front side of a blanket silicon wafer first by plasma-enhanced chemical vapor deposition (PECVD). The front-side pattern of lithography, etching, and Ta barrier and Cu seed layer are processed by the 12-in contact aligner, 12-in physical vapor deposition (PVD), and 12-in copper electrochemical plating (ECP) process, respectively. The front-side RDL can be formed on top of the ILD, and then the silicon oxide/silicon nitride as the front-side RDL passivation layer is deposited on top of the RDL by PECVD. For pad formation, the front-side opening (FO) is formed on top of the front-side RDL passivation layer by the etching process. After that, the Ti/TiN/Ti and aluminum pads (APs) are patterned by both the lithography and etching processes, as shown in Fig. 2(a). The patterned wafer needs to be trimmed at the edge before wafer bonding and grinding to prevent wafer crack during the grinding process. The adhesive glue is employed to bond with the silicon carrier wafer for supporting the bonded wafer. With the silicon carrier, the bonded wafer can be thinned by the grinding process down to only 50 μm preparing for the 5 $\times$ 50 μm backside TSV process. Note that the silicon oxide/silicon nitride as the backside ILD layer and the backside RDL passivation layer are sequentially deposited on the backside of Si wafer, as shown in Fig. 2(b).

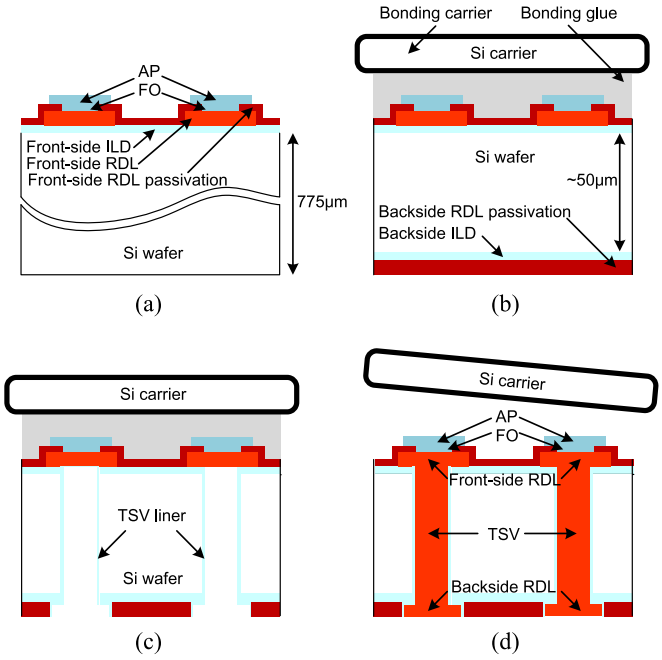

Fig. 2. Process flow of the in-house developed 3-D IC via-last backside-TSV interposer. (a) Front-side process. (b) Wafer thinning and backside layer deposition. (c) TSV etching. (d) Carrier removing.

The backside RDL region is then patterned and etched after the TSVs with a 5-μm diameter formed by Bosch-type deep reactive-ion etch (DRIE), followed by depositing the insulator (TSV liner) with the silicon oxide on the sidewall using the semiatmosphere chemical vapor deposition (SACVD), as shown in Fig. 2(c). For TSV formation, the Ta barrier and Cu seed layer are deposited by the PVD, and the Cu electroplating is used to fill the TSVs, followed by using the CMP process for RDL and TSV planarization. Finally, the bonding glue and the carrier are removed, as shown in Fig. 2(d). Fig. 3 shows the scanning electron microscope (SEM) cross

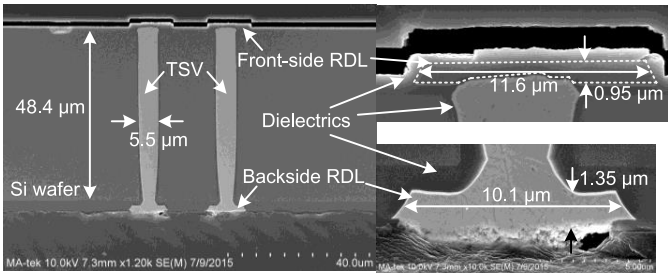

Fig. 3. Cross-sectional SEM image of the TSV region of the 3-D transformer.

TABLE I
TECHNOLOGY PARAMETERS FOR TSV INTERPOSER PROCESS

Parameter	Unit	Value
Silicon substrate resistivity	ohm-cm	10
Silicon substrate dielectric constant	N/A	11.9
TSV and RDL conductivity	S/m	5.8×10^7
TSV liner dielectric constant	N/A	4
Front-side RDL thickness	μm	0.95
Backside RDL thickness	μm	1.35
TSV diameter	μm	5.5
TSV height	μm	48.4
TSV liner thickness	μm	0.5

section of the fabricated TSV, which has a diameter of about 5.5 μm and a height of about 48.4 μm. The technological parameters of the in-house developed via-last backside-TSV interposer process are summarized in Table I.

The structure that we proposed can also be implemented on the laminate and glass substrates, but the transformer characteristics will change accordingly, depending on the design rule and substrate material properties. The IPD using the typical laminate process can only achieve a minimum feature size in tens of micrometers at present. As a result, the transformers can consume a much larger area with a relatively low operating frequency compared to the silicon process. On the other hand, the glass substrate has low loss and high-Q characteristics, but the material properties make it more difficult for the through-glass-via (TGV) process, and the heat dissipation on the glass substrate is also an issue [30], [31]. At present, the IPD process under the silicon substrate is more mature with low cost, which can achieve a smaller feature size and a compact transformer design. In addition, the high-resistance silicon substrates also allow for obtaining high-quality factors at high operating frequencies. It should be emphasized that the proposed silicon-based TSV process can be better integrated with the CMOS technology to achieve a compact system.

III. 3-D FULLY SYMMETRIC TSV TRANSFORMERS

A. Design of 1:1 3-D Transformer

Fig. 4 shows the structure of the proposed fully 3-D symmetrical 1:1 transformer. The transformer is routed by a single-layer RDL of the front side and back side together with the TSV in the 3-D IC process. Compared with the traditional planar transformer, increased inductance per unit area with enhanced coupling area can be attained by the extra TSV vertical path of the transformer. Also, it can be easily seen that

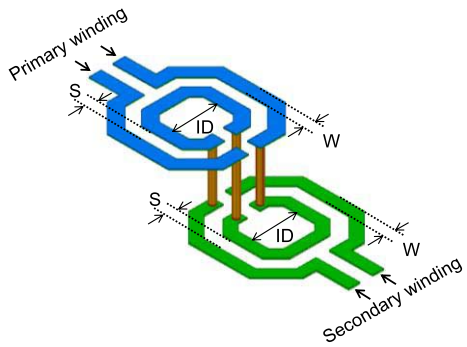

Fig. 4. Primary and secondary windings of the proposed 3-D fully symmetric TSV monolithic (1:1) transformer.

the structure is perfect mirror symmetrical with the identical primary and secondary windings.

The main design parameters of the 1:1 3-D TSV transformer are the width (W) and spacing (S) of RDL metal trace and the inner diameter of transformer (ID), as shown in Fig. 4. In a typical design procedure, the inner diameter and number of turns of the coil are designed first to obtain the required inductance values for a specific circuit, which could be a part of the matching network or loading in the circuit. The inductance increases with the inner diameter and turn number. The transformer is then optimized for a specific frequency with a high quality factor Q. Note that a proper selection of the linewidth also plays an important role in the transformer characteristics. In general, a wider line could result in high Q but consume more area with a lower SRF. The required coupling characteristics could be adjusted by the spacing between the traces. However, the spacing is limited by the design rule in the proposed 3-D TSV transformer, which results in a relatively small coupling coefficient. In a practical design, it is essential to perform iteration by the computer-aided design (CAD) tools to see the tradeoff among these parameters to achieve the desired transformer characteristic. Based on the previously described 3-D IC 5 $\times$ 50 μm backside TSV process, different transformers have been designed with a fixed W of 10 μm but various other design parameters. The transformers with ID of 40 and 60 μm and S of 10 and 1 μm are designed and analyzed. The characteristics of the transformers, including inductance and Q factor, coupling coefficient K, and turn ratio N, are extracted from the S-parameters obtained by the 3-D EM simulator HFSS, as shown in Fig. 5(a)–(c).

Fig. 5(a) shows the inductance of the primary coil (identical with the secondary coil) as a function of frequency for different inner diameters and metal trace spacings. By increasing ID and S, the inductance increases mainly due to a longer coil length. Note that the SRF also varies with ID and S. The SRF reduces with S, which can be attributed to the increased coupling parasitic capacitances.

Fig. 5(b) shows the Q factors of the primary coil. As can be seen, the Q factors are similar at low frequencies with different ID but the same S, whereas Q becomes higher with smaller ID due to less resistive parasitics with a shorter metal trace. In contrast, the lower Q factors with smaller S result

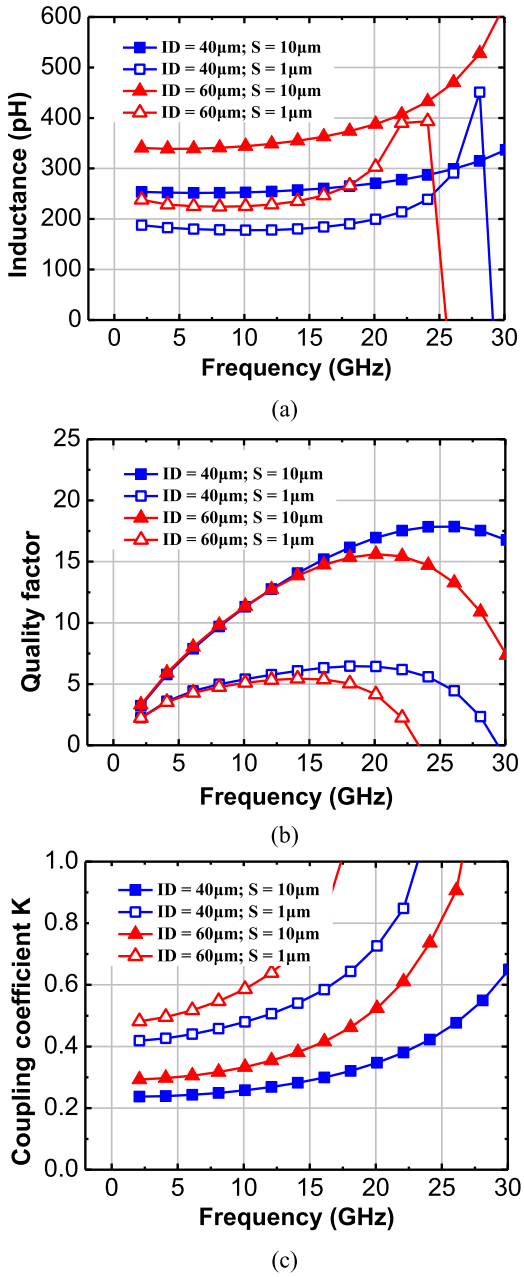

Fig. 5. Simulated results of the proposed fully 3-D symmetrical TSV (1:1) transformers with different geometries, including (a) inductance, (b) Q factor, and (c) coupling coefficient K.

mainly from the smaller inductance and also the higher parasitic coupling capacitance between the coils. Fig. 5(c) shows the coupling coefficient K also as a function of frequency for different inner diameters and metal trace spacings. With the same ID, it is expected that the coupling coefficient increases as S reduces. Also, the coupling is enhanced with ID if S keeps the same, which can be attributed to the increased coupling distance with a longer metal trace.

By the 3-D EM simulation, the 3-D fully symmetric 1:1 transformer property can be verified. As shown in Fig. 5, with an inner diameter of 40 μm and a trace spacing of 1 μm in the transformer, the inductances of both the primary and second coils are about 196 pH with the Q factor and coupling

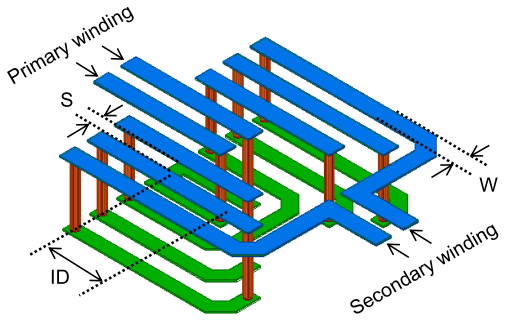

Fig. 6. Proposed 3-D TSV 1:N transformer, where the primary winding is one and that for the secondary coil is 3.

coefficient of around 7 and 0.72 at 20 GHz, respectively. It should be mentioned that a high coupling coefficient cannot be achieved in the actual design due to the limitation of metal trace spacing (minimum S is 10 μm) in the developed process, as will be shown in Section IV with the measured results.

B. Design of 1:N 3-D Transformer

The 3-D symmetrical 1:N transformer is also investigated in the proposed design with different turn ratios. Fig. 6 shows the 3-D TSV transformer with a 1:3 turn ratio, in which the key design parameters include W, S, ID, and the turn ratio N. Note that the turn ratio here is simply based on the layout in our design, as shown in Fig. 6. Similarly, the 3-D EM simulation is performed for the transformer based on the previously described 3-D TSV process technology. Transformers with different geometries are investigated with the fixed W and ID of 10 and 40 μm, respectively, while S is also with the two values of 1 and 10 μm. The characteristics of the transformers, including inductance, Q, K, and N, are extracted from the S-parameters by 3-D EM simulation, as shown in Fig. 7. Fig. 7(a) and (b) shows the inductance and Q factor, respectively, of both the primary and secondary coils as a function of frequency. As can be seen, the three times of turn ratio result in a nearly nine-times actual inductance ratio in the low-frequency range. Also, the secondary coil has a much lower SRF. The observed trends for inductance and Q are similar to those for the above-mentioned fully symmetric 1:1 transformer. The inductance, Q, and SRF increase with S, as shown in Fig. 7.

Fig. 7(c) shows the coupling coefficient K as a function of frequency for different metal trace spacings of 1 and 10 μm. As expected, K increases with reduced S due to the more tightly coupling between the metals traces. Note that the relatively small K can be attributed to the process limitation, which only provides two RDL for transformer routing. The coupling between the coils mainly contributes to the lateral direction. As a result, the metal thickness (only about 1 μm) and spacing limit the achievable coupling coefficient of the transformer. Fig. 7(c) also shows the turn ratio between the primary and secondary coils. The calculated turn ratio here is defined as follows [32]:

$$\text{Turn ratio} = \sqrt{\frac{L_{\text{Sec}}}{L_{\text{Pri}}}} \tag{1}$$

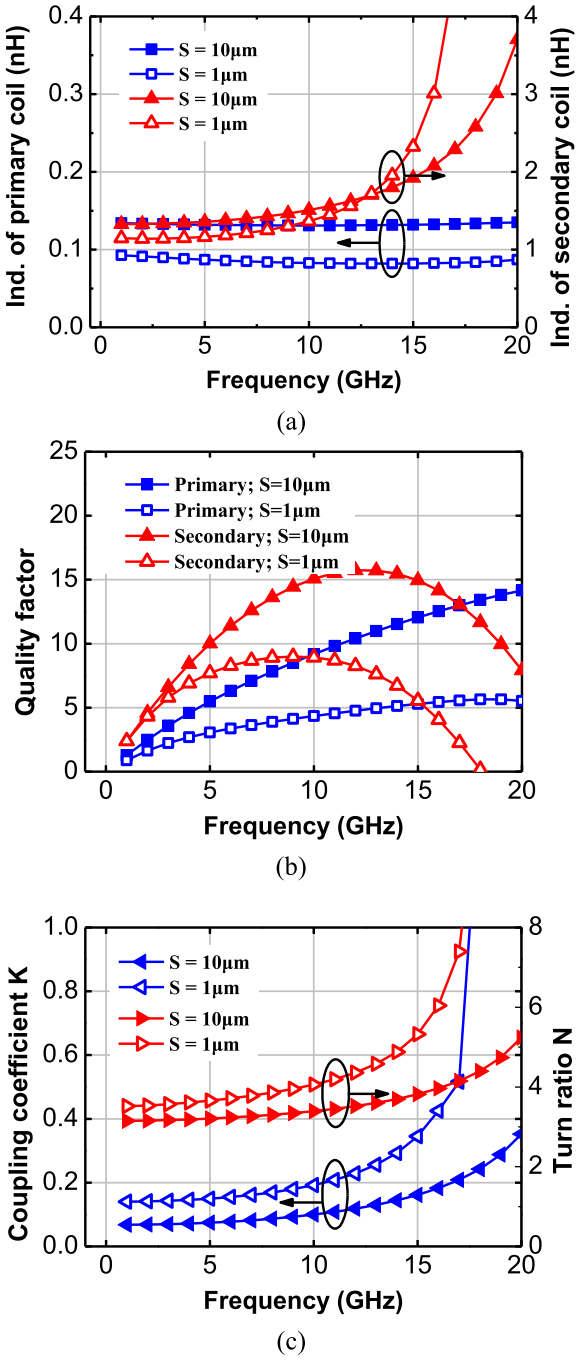

Fig. 7. Simulated results of the proposed differential symmetrical TSV monolithic (1:3) transformer. (a) Inductance. (b) Q factor. (c) Coupling coefficient K and turn ratio with various geometries.

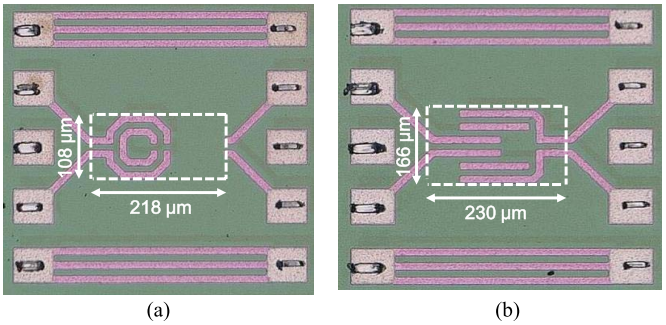

Fig. 8. Chip photograph of (a) fully 3-D symmetrical TSV 1:1 transformer with an inner diameter of 40 μm. (b) Differential symmetrical TSV 1:3 transformer.

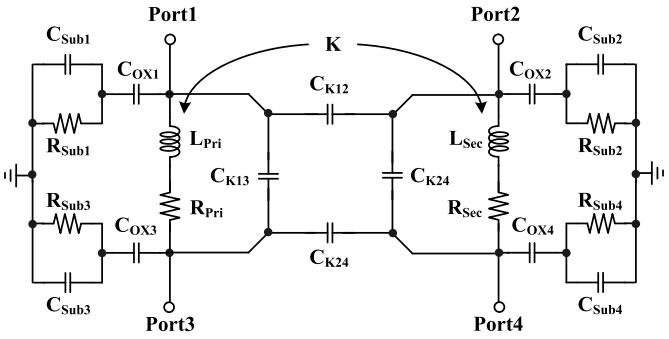

Fig. 9. Equivalent-circuit model of 3-D symmetrical TSV 1:1 transformer.

where L_{Pri} and L_{Sec} represent the inductance of the primary and secondary coils, respectively. The calculated turn ratio of the proposed design is around 3 at low frequencies, which is consistent with the physical layout. Also, a trend can be observed that the effective turn ratio increases with frequency since L_{Sec} has a lower SRF, and hence, the inductance increases faster compared with L_{pri} when frequency increases [see Fig. 7(a)]. With an inner diameter of 40 μm and 1-μm trace spacing in the transformer of 1:3 turn ratio, the inductances of the primary and second coils are 87 and 1167 pH with the Q factors of 3.03 and 7.60 at 5 GHz, respectively, and the coupling coefficient is only about 0.15. As mentioned, the coupling coefficient can be further improved by increasing metal thickness and reducing trace spacing to enhance the lateral coupling. With the metal thickness increased to 5 μm and spacing reduced to 0.5 μm, a coupling coefficient improved by 2.7× (0.34 at 9.3 GHz) can be obtained based on the 3-D EM simulation.

IV. Measured Results and Model Extraction

Fig. 8(a) and (b) shows the chip photographs of the in-house fabricated 3-D TSV transformers with the turn ratios of 1:1 and 1:3, respectively. As can be seen, the core areas of the transformers are only 218 μm × 108 μm and 230 μm × 166 μm. The devices were measured on-wafer using Network Analyzer (Agilent N5245A) from 1 to 25 GHz. The measured results will be discussed later, compared with the equivalent circuit model and also the full-wave EM simulations.

A. Equivalent-Circuit Model Extraction of Transformer

Various compact models and extraction methods of monolithic transformers were proposed previously for the 2-D planar structures [33]–[37]. This article establishes a simple equivalent circuit model for the proposed 3-D symmetric transformers based on the physical structure, as shown in Fig. 9. Note that the parasitics introduced by the TSV have been included as a part of the primary and secondary coils in the model for simplicity. The values of model parameters are analytically

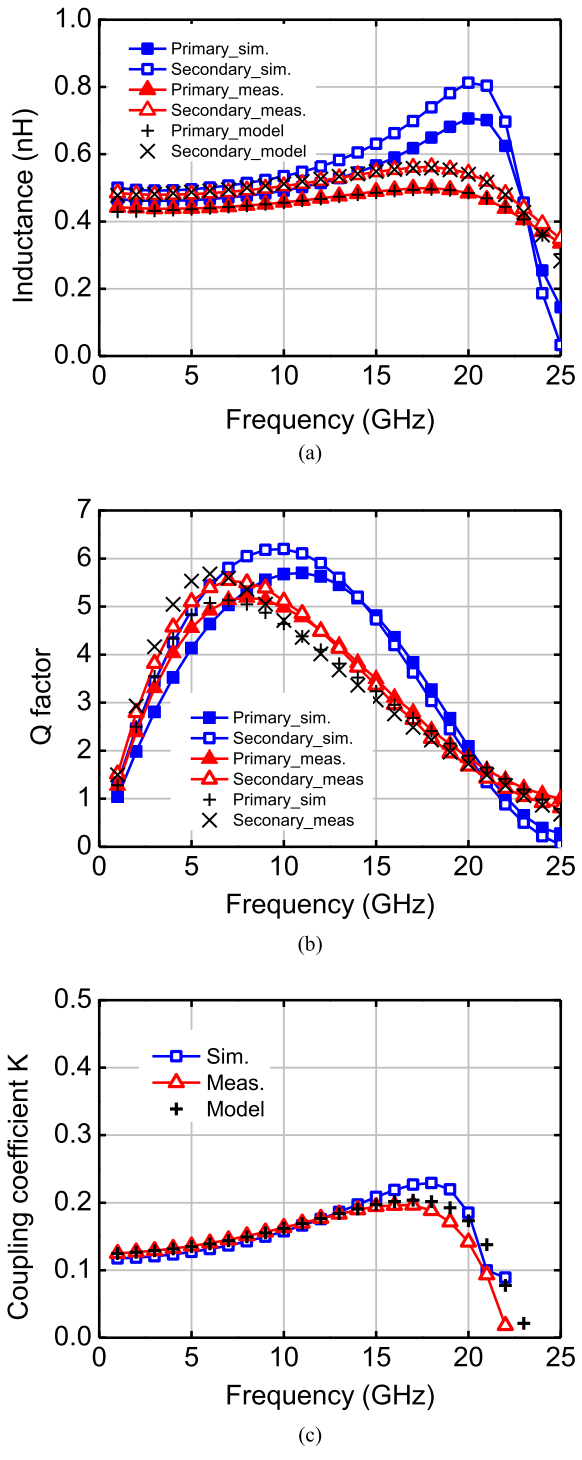

Fig. 10. EM simulated, measured, and modeled characteristics of fully 3-D symmetrical TSV 1:1 transformer with an inner diameter of 40 μm. (a) Inductance. (b) Q factor of the primary and secondary windings. (c) Coupling coefficient K.

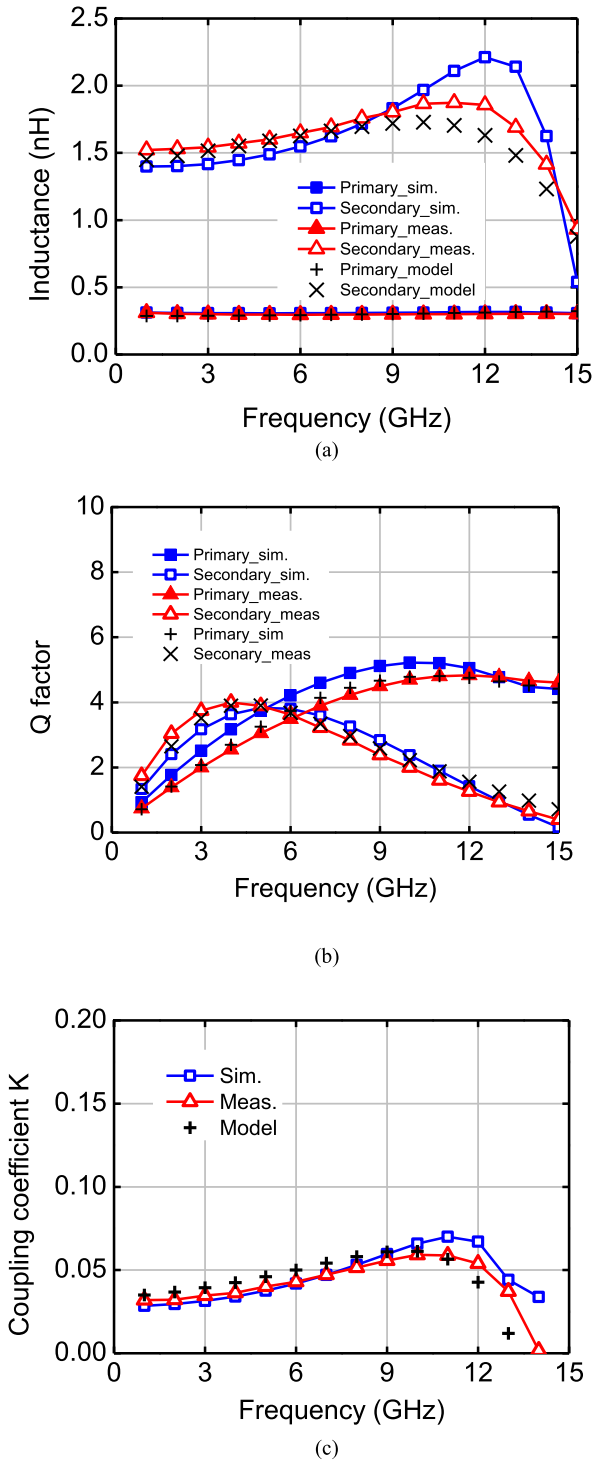

Fig. 11. EM simulated, measured, and modeled characteristics of differential symmetrical TSV monolithic (1:3) transformer. (a) Inductance. (b) Q factor of primary and secondary windings. (c) Coupling coefficient K.

extracted from the S-parameters measured by the four-port test structures [37]. Each component is described as follows, where L_{Pri} and L_{Sec} represent the inductance of the primary and the secondary windings, respectively, and the corresponding parasitic resistances are R_{Pri} and R_{Sec}. C_{OX1}, C_{OX2}, C_{OX3}, and C_{OX4} are the equivalent capacitances of the oxide layer, and R_{Sub1}, R_{Sub2}, R_{Sub3}, R_{Sub4}, C_{Sub1}, C_{Sub2}, C_{Sub3}, and C_{Sub4} represent the substrate parasitic RC components. C_{Kij} represents four-port coupling effect between ports i and j.

By using the deembedding procedure with the open pad, the intrinsic transformer characteristics can be extracted and modeled. The extracted component values in different designs are listed in Table II. It should be mentioned that the silicon substrate parasitics as presented by R_{SubN} and C_{SubN} in the

TABLE II
EXTRACTED VALUES OF THE MODEL PARAMETERS FOR THE PROPOSED TRANSFORMERS

		Fully 3-D symmetrical TSV (1:1) structure (S = 10 μm)	Differential symmetrical TSV (1:3) structure (S = 10 μm)
Parameter	Unit	*ID* = 40 μm	*ID* = 40 μm
L_{Pri}	pH	420	288
L_{Sec}	pH	457	1482
R_{Pri}	Ω	2.074	2.521
R_{Sec}	Ω	1.882	5.228
C_{OX1}	fF	190.4	124.0
C_{OX2}	fF	200.3	190.5
C_{OX3}	fF	203.6	181.6
C_{OX4}	fF	186.4	188.8
R_{SUB1}	Ω	240.4	316.6
R_{SUB2}	Ω	244.9	213.0
R_{SUB3}	Ω	247.0	331.2
R_{SUB4}	Ω	241.2	255.4
C_{SUB1}	fF	42.0	40.4
C_{SUB2}	fF	45.4	50.3
C_{SUB3}	fF	42.5	32.3
C_{SUB4}	fF	43.3	45.2
K	N/A	0.123	0.050
$C_{K12} = C_{K34}$	fF	19.3	18.4
C_{K13}	fF	4.6	3.9
C_{K24}	fF	5.0	4.3

TABLE III
COMPARISON OF 1:1 3-D TSV TRANSFORMERS

Reference	Unit	[28]*	[29]#	This work+
Lp	pH	551	177	439
Qp	N/A	18.79	7.99	4.59
SRFp	GHz	28.5	32.89	23.7
Ls	pH	456	177	482
Qs	N/A	21.50	7.99	5.11
SRFs	GHz	35.0	32.89	24.0
K	N/A	0.853	0.900	0.136
Core area	mm^2	0.16	1.0	0.024

* Simulated results; # estimated from the provided model; + measured results.

model should have a constant product independent of device geometry (for example, R_{Sub1} and C_{Sub1}) [38], which can also be verified by the extracted parameters in Table II.

Fig. 10 shows the results of the fully symmetrical (1:1) design with the *ID* of 40 μm and *S* of 10 μm. As can be seen, a good agreement among the simulated, measured, and modeled parameters of the transformer can be observed. At the operating frequency of 5 GHz, the 1:1 transformer has the primary winding inductance (*Lp*) of 439 pH, the secondary winding (*Ls*) of 482 pH, *Q* values (*Qp* and *Qs*) of 4.59 and 5.11, SRFs (SRF*p* and SRF*s*), respectively, and the coupling coefficient (*K*) of 0.136. Compared with the previously reported works, our chip has a symmetric advantage but with a relatively low coupling coefficient. It should be mentioned that a high coupling coefficient can be achieved in the actual design with a reduced metal trace spacing and increased metal thickness by improving the technology. Table III compares the proposed work with other state-of-the-art results from different transformers based on the 3-D TSV technology.

The discrepancy between the EM simulated results and by the other methods especially at relatively high frequencies could be mainly attributed to the process variation from the ideal structure. For example, the diameter and also the thickness of TSV liner have an issue of nonuniformity, and the formed TSV is not an ideal cylinder.

Fig. 11 shows the verification of the 1:3 turn ratio transformer, which also shows good agreement among the simulated, measured, and modeled results. The measured results at 5 GHz show that the 1:3 transformer has a primary winding inductance of 295 pH, the secondary winding inductance of 1.61 nH, both with *Q* factors larger than 3, and the coupling coefficient is 0.037. Note that the main reasons of the low coupling coefficient are the limitation of lateral coupling due to the limitation of the thin metal thickness (1 μm) and a relatively large spacing (10 μm) between the metal traces of the in-house developed 3-D IC TSV process. As mentioned earlier, the same structures with increased thicknesses and reduced spacing can effectively improve the coupling coefficient.

V. CONCLUSION

This article successfully demonstrated novel fully symmetric TSV 3-D transformers with a very compact area using the in-house developed processes. Both the 1:1 and 1:*N* transformers were designed, characterized, and modeled. The equivalent-circuit model parameters are extracted based on the measured S-parameters and compared with the EM simulated results. The proposed 3-D transformers show excellent symmetry property and are suitable for differential circuit applications. The coupling coefficient of the proposed structure can be further enhanced by reduced the metal trace spacing and also thickened metal thickness with more RDL layers.

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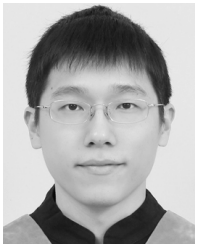

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