A 0.01-to-2.6-GHz Two-Fold Current Reuse Dual Noise-Canceling LNA Achieving 6.8-K Noise Temperature for Quantum Applications

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***Abstract*—This brief presents a cryogenic inverter-based two-fold current reuse with a dual noise-canceling low-noise amplifier (LNA) in 40-nm CMOS. The proposed LNA consists of three stages: a current-reuse inverter-based input stage with shunt-resistive feedback and self-body bias (SBB) to mitigate the V_{th} increase and boost r_{out} under cryogenic temperature. The second stage is the dual auxiliary noise-canceling stage with an additional current reuse parallel transistor to enhance transconductance and suppress the noise of both the main amplifier and auxiliary amplifier. The last stage is a common-source post-amplifier for further gain enhancement. At 4 K, the LNA achieves a measured peak gain (S_{21}) of 31 dB, with a large 3-dB bandwidth from 10 MHz to 2.6 GHz and a minimum NF of 0.1 dB (corresponding to noise temperature T_N of 6.8 K) at 0.6 GHz under power dissipation of 8.6 mW. The circuit occupies a core area of 0.117 mm^2.**

***Index Terms*—Cryogenic, CMOS, current reuse, low-noise amplifier (LNA), noise canceling, quantum computing, self-body bias.**

I. Introduction

LARGE scale quantum computers have immense potential and advantages to address intractable challenges and solve refractory problems that would be impossible with the cope of classical computers, such as the simulation of molecules, synthesis of drugs and materials, and quantum cryptography [1], [2], [3]. With the large number of qubits integrated to achieve quantum supremacy, a high level of integration of the qubits with the peripheral readout circuitry would be one of the major obstacles to achieving a practical quantum computing system. Furthermore, to augment the fidelity of qubit operations and simplify the system, it is proposed that the control and readout circuitry should operate at cryogenic temperatures near the qubits [4], [5]. CMOS-based qubits and circuits are an appealing technology to tackle this problem by providing promising solutions for a high level of integration, low cost, and compatibility to integrate control and readout circuitries for a large number of qubits fabrication on a single chip [6], [7], [8]. This helps to improve the system fidelity and qubits coherence due to the reduction of a larger number of bulky RF cables, delay time, filters, and isolators.

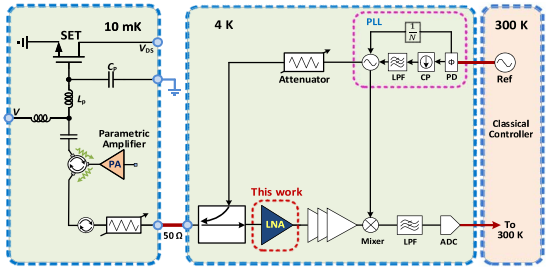

Fig. 1. Simplified block diagram of the qubits readout system.

Fig. 1 shows a simplified block diagram of the qubit's readout circuits. As shown in the figure, a parametric amplifier is employed at a base temperature near qubits whose noise temperature can reach below 1 K with power consumption smaller than 1 mW [9], [10]. The parametric amplifier alleviates the noise temperature requirements of the second-stage low-noise amplifier (LNA) operating at 4 K for the qubit's readout as indicated in the figure. However, the noise temperature required for the readout LNA is still a challenge, which is in a range of only several kelvins to detect the immensely weak signals from qubits. Owing to the superior RF characteristics at the cryogenic temperatures, additional readout signal amplification is primarily achieved by the III-V compound semiconductors HEMTs or SiGe HBT technologies, which can achieve a very high gain, a few kelvins of noise temperature operating at relatively low power consumption [11], [12], [13]. Nevertheless, these solutions eventually will encounter problems as the qubit number keeps increasing for a practical large-scale quantum computer. Prior published cryo-CMOS in 40-nm showed a relatively high-power consumption of 39 mW at 4.2 K [14]. An LNA in 40-nm CMOS dissipated 19.4 mW at 4 K [15], and also an LNA realized in 28-nm CMOS had a power consumption of 4.2 mW at 4.2 K [16].

In this brief, we propose using CMOS technology to realize the LNA for the spin qubit-based RF reflectometry of the readout receiver stage in the sub-GHz frequency range. The

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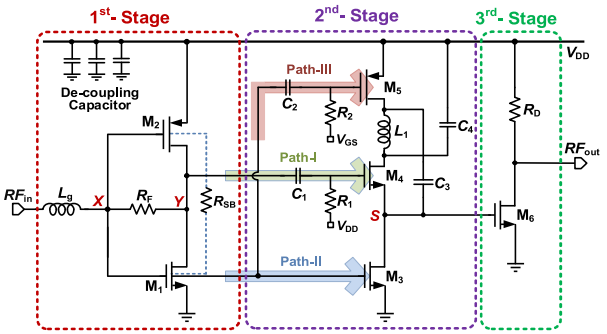


Fig. 2. Schematic of the proposed two-fold current-reuse dual noise canceling LNA.

proposed LNA is designed using 40-nm CMOS technology and operates at 4 K ambient temperature for quantum computing applications.

II. Circuit Design and Topology

Fig. 2 shows the circuit topology of the proposed common-source (CS) inverter-based, two-fold current-reuse, and dual noise-canceling (NC) LNA. Noise-canceling is an effective design technique to mitigate the channel thermal noise of the main amplifier, achieved by utilizing an auxiliary amplifier path that generates a correlated, out-of-phase noise signal [17]. A dual noise-canceling auxiliary transistor is utilized to further cancel the channel noise of the main amplifier. However, the thermal noise effect of the NC auxiliary amplifier itself is reduced due to the parallel configuration.

A. First Stage Main Amplifier Design

The first stage consists of an inverter-based current-reuse configuration formed by the CS transistors M_1 and M_2. A large shunt feedback resistor R_F is employed for self-bias/matching, while the gate inductor L_g is helpful for simultaneous noise and input matching to achieve wideband S_{11}. Consequently, low power, low noise figure (NF), and wideband S_{11} and S_{21} can be achieved by combining inductive impedance matching with self-bias feedback resistor R_F to control the overdrive voltage of transistors M_1, M_2, and M_3. It should be emphasized that a self-body bias (SBB) resistor, R_{SB}, is employed to connect the bodies of the input transistors M_1 and M_2. The threshold voltage (V_{th}) of the MOS transistor increases at the cryogenic temperature due to an increase in fermi-potential and widening of the gap between the semiconductor bands, leading to changes in circuit characteristics which result in less headroom for LNA at 4 K [16]. To alleviate the increment in threshold voltage (V_{th}) at cryogenic temperature, it should be emphasized that a self-body bias resistor R_{SB}, is used to mitigate V_{th} increase at cryogenic temperatures by keeping V_{th} similar to the room temperature (RT) and alleviate the short channel effect by improving the output resistance r_{out} of the transistors. With a properly designed R_{SB}, the supply voltage is divided equally between the bodies of M_1 and M_2 through a voltage-divider self-bias loop for the source body diodes, and the substrate leakage current can be reduced [15]. The first-stage transistors (NMOS and PMOS) have a size ratio of 1:1 for simultaneous noise and input matching, which helps to improve the transconductance efficiency (g_m/I_d) for low-power operation while keeping the desired value of the bias voltage at node X.

TABLE I
Passive Component Values in the Proposed LNA

L_g	R_F	R_{SB}	R_1
1 nH	1.13 kΩ	2 kΩ	6 kΩ
R_2	$C_{1\text{-}4}$	L_1	R_D
6 kΩ	2.5 pF	1.2 nH	64 Ω

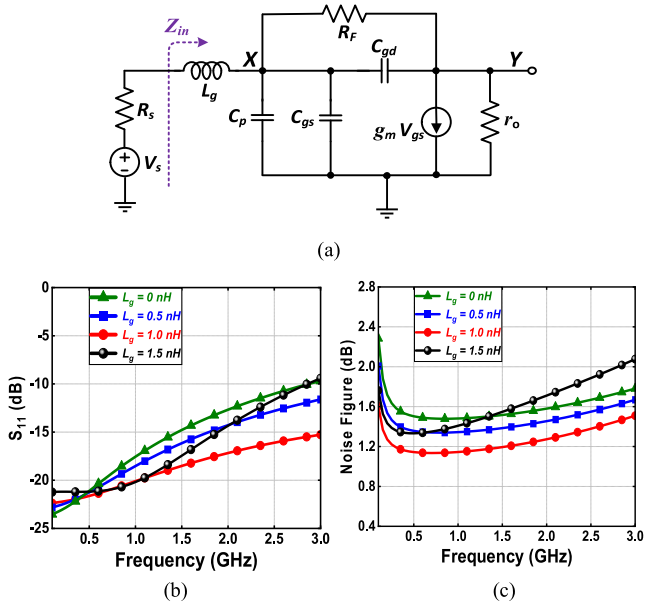


Fig. 3. (a) Simplified small-signal equivalent circuit model of the input stage (b) Simulated results of different L_g vs. S_{11} (c) Simulated results of different L_g vs. NF.

B. Input Impedance and Noise Analysis

Fig. 3(a) shows the simplified small-signal equivalent circuit model with the design parameters used for input impedance calculations. In the input inverter-based current-reuse stage, NF and gain can be improved by using a larger value of the feedback resistor R_F, but with the cost of input matching. A gate inductor L_g can be employed to improve input matching while maintaining a high transconductance of the inverting stage. Fig. 3(b) and (c) show how the input matching S_{11} and NF vary as a function of L_g based on the final designed LNA. As shown in the figures, the input matching bandwidth of the circuit improves as L_g increases, also NF decreases as L_g increases. Also, a higher value of L_g allows a smaller size of the inverting input transistors for simultaneous noise and input matching, which helps to mitigate the channel thermal noise and reduce the power consumption of the input transistors. However, after L_g reaches a certain value, matching and NF start to degrade. The input impedance Z_{in} of the proposed LNA by neglecting the C_{gd} can be expressed as

$$Z_{in} = \left[\left\{R_T \left\| \left(\frac{1}{sC_p} \left\| \frac{1}{sC_{gs}}\right.\right)\right.\right\} + s(L_g)\right] \tag{1}$$

where $C_{gs} = C_{gs1} \| C_{gs2}$, $C_p = C_{gs3} \| C_{gs5}$ and R_T is calculated as:

$$R_T = \left[\frac{(r_{01} \| r_{02}) + R_F}{\{1 + (g_{m1} + g_{m2})(r_{01} \| r_{02})\}}\right] \tag{2}$$

From Fig. 2, the noise source of the inverting input stage and noise-canceling (NC) stage are analyzed. The total noise factor F of the proposed LNA can be expressed as

$$F = 1 + F_1 + F_2 + F_{R_F} \tag{3}$$

where "1" represents noise due to the source. F_1, F_2, and F_{RF} represent the noise factor of transistors (M_1, M_2) and (M_3, M_4, M_5) and feedback resistor R_R, respectively. The noise factor in terms of channel thermal noise current can be calculated as:

$$F = \frac{\overline{I^2_{n,T}}}{4k_B T R_S G^2} \tag{4}$$

where k_B is Boltzmann's constant, T is the absolute temperature, R_S is the source resistance, and G is the transconductance. F_1, F_2, and F_{RF} can be calculated as

$$F_1 = \frac{\gamma(g_{m1} + g_{m2})}{\alpha R_S G^2_{\text{core}}} \left[\frac{g_{m4}(R_F + R_S) - R_S(g_{m3} + g_{m5})}{1 + R_S(g_{m1} + g_{m2})} \right]^2 \tag{5}$$

$$F_2 = \frac{\gamma\{g_{m4} + (g_{m3} + g_{m5})\}}{\alpha R_S G^2_{\text{core}}} \tag{6}$$

$$F_{R_F} = \frac{R_F g^2_{m4}}{R_S G^2_{\text{core}}} \tag{7}$$

where γ is noise parameter, and $\alpha = g_m/g_{d0}$. g_{m1} to g_{m5} are the transconductance of transistors M_{1-5}, and G_{core} is the transconductance of the core LNA.

$$G_{\text{core}} = \left[g_{m4}\{1 - (g_{m1} + g_{m2})R_F\} - (g_{m3} + g_{m5}) \right] \tag{8}$$

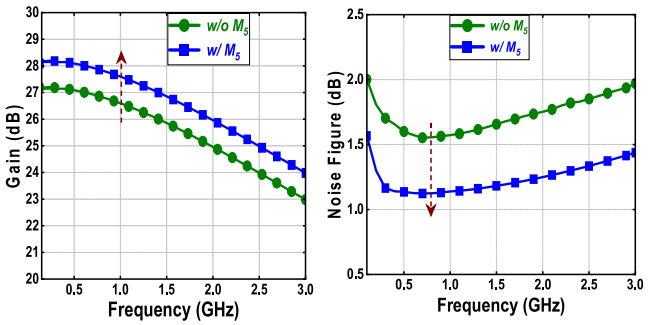
The NC condition is achieved by satisfying the following conditions:

$$1 + \frac{R_F}{R_S} \cong \frac{(g_{m3} + g_{m5})}{g_{m4}} \tag{9}$$

where g_{m3}, g_{m4}, and g_{m5} are the transconductance of transistors M_3, M_4, and M_5, respectively. Fig. 4(a) and (b) show the simulated gain and noise figure of the proposed LNA with and without the auxiliary transistor M_5, respectively. The gain and NF can be improved by around 1 dB and 0.4 dB respectively at 0.7 GHz (frequency with minimum NF), compared to that without M_5.

C. Second Stage Auxiliary Amplifier Design

As shown in Fig. 2, the second stage is a current reuse and dual noise-canceling auxiliary stage formed by CS transistors M_3 and M_5 for eliminating the channel thermal noise of transistors M_1 and M_2 in the inverting input main stage. The source-follower transistor M_4 then combines the signal from different paths at node S for signal summation and noise canceling. Note that the noise current of the main transistors M_1 and M_2 (inverting configuration) flows toward its gate through the feedback resistor R_F, creating in-phase noise voltage at nodes X and Y, while with the out-of-phase signal voltage at nodes X and Y. Noise and signal voltage at node X follow path II and path III and are further amplified and then inverted through the auxiliary transistors M_3 and M_5, respectively. On the other hand, the in-phase noise and phase-inverted signal voltage at node Y follow path I and appear at node S through M_4. As a result, the noise voltage is canceled out due to the opposite polarity, while the signal voltage is added up. Note that the V_{th} variation of M_4 at cryogenic temperatures could be an issue for the level of in-phase noise at the output node S. In the proposed design, a relatively high gate bias voltage of V_{DD} is applied for M_4, which can mitigate this effect at 4K.



(a) (b)

Fig. 4. Simulated results of LNA with and without noise-canceling auxiliary transistor M_5 (a) Gain (S_{21}) (b) Noise-figure (NF).

It should be emphasized that transistor M_5 (pMOS) and inductor L_1 play a pivotal role in the proposed topology, which allows reusing the current of M_3 and creates an effective inverter stage. Note that a 3-D inductor L_1 is employed to minimize the chip area. Using five metal layers (from metal 5 to metal 9) in a stacked format, the inductor has an area of only 0.01 mm^2 (100 μm $\times$ 100 μm), but with a large inductance of 1.2 nH. The combination of L_1 and C_4 provides a relatively high impedance (> 100 Ω up to ∼ 600 MHz) to block the RF signal while allowing the DC current to flow to the drain of M_4. Also, the capacitor C_3 provides an alternative path for the RF signal to flow to node S. As a result, the signal of path III after being amplified and inverted by the transistor M_5 appears at node S through capacitor C_3. Effectively, M_3 and M_5 construct an inverter with the drain nodes connected at node S for current reuse. The proposed design creates a two-fold current reuse topology with the first and second stages by utilizing the same current of M_1 and M_3 respectively and facilitating double noise-canceling with the noises propagating via different transistors M_3 and M_5 for the auxiliary amplifier. The effective transconductance of the complementary transistors M_3 and M_5 in the auxiliary amplifier is added up due to the parallel configuration (ac-wise), which helps to increase gain and reduce channel thermal noise of the inverting input stage without burning more current.

Note that relatively long channel lengths are chosen for some of the transistors, 150-nm for (M_1 and M_2) and 100-nm for (M_3) in our design to lower the impact of shot noise at cryogenic temperature [16], [18]. Unlike thermal noise, shot noise cannot be eliminated by lowering the temperature [18]. Shot noise becomes more overriding in the short-channel devices at cryogenic temperatures. It primarily originated due to the discrete nature of electrons, because there is random fluctuation of the current in a conductor.

The third stage is a common-source post-amplifier stage (buffer stage) consisting of transistor M_6 and resistor R_D for gain enhancement and 50-Ω output impedance matching environments without using any additional gate biasing circuits, which reduces parasitics and chip area. The transistor size of the buffer stage is optimized to boost the gain and also for the output matching, which consumes a current of 2.5 mA at 4 K. Note that the power consumption of the buffer stage is included in the overall P_{DC}.

TABLE II
PERFORMANCE COMPARISON SUMMARY WITH THE STATE-OF-THE-ART CRYOGENIC CMOS LNAS

Ref.	This work		JSSC'18 [2]		JSSC'21 [14]		JSSC'23 [16]		MWCL'22 [22]	
Technology	40-nm CMOS		160-nm CMOS		40-nm CMOS		28-nm CMOS		65-nm CMOS	
Topology	Noise-Canceling + Two-fold Current reuse + SBB		Noise-Canceling		Cascode + R-C loading + XFMR load		Cascode Inverter + C-feedback + gate L		CS Folded-Cascode	
Supply Voltage (V_{DD})	1.2		1.4		1.4		1.04		1.2	
Frequency (GHz)	0.01 ~ 1.9	0.01 ~ 2.6	0.1 ~ 0.5		4.1 ~ 7.9	4.6 ~ 8.2	6 ~ 8		0.9 ~ 1.8	
Meas. Temp. (K)	300	4	300	4.2	300	4.2	300	4.2	300	20
Gain (dB)	24.8 ~ 28	26.6 ~ 31	35 ~ 40	50 ~ 58	35.5~36.5	39.2~44.8	54*	N/A	35^{+}	37.2
Power (mW)	17.6	8.6	80	91	51.1	39	3.5	4.2	N/A	125
NF (dB)	1.16 ~ 1.7	0.1 ~ 0.48	0.8 ~0.125	0.1 ~ 0.85	0.73~1.26	0.23~0.65	2.5 ~ 3.5	0.4 ~ 0.7	N/A	0.03~0.13
S_{11} (dB)	-21.4~-15.2	-15.3~ -11.6	-9 ~ -5	-7 ~ -3	-22 ~ -12	-26 ~ -5.8	< -6	< -4	< -10^{+}	< -10
Area (mm^2)	0.117$^{\#}$		0.249$^{\#}$		0.72		0.2$^{\#}$		1	

$^{\#}$Core chip area; *Simulated gain; $^{+}$Estimated from figures.

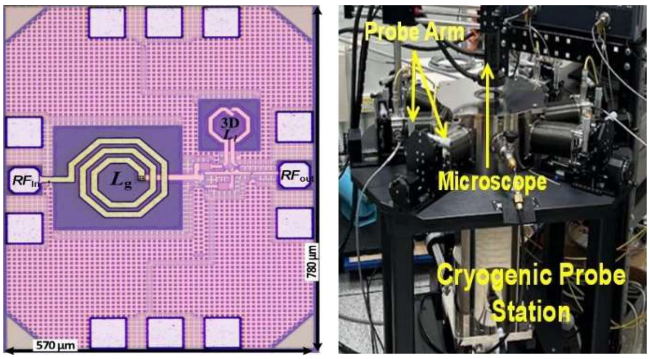
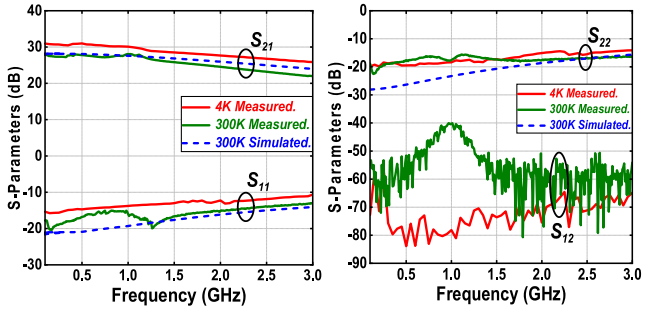


Fig. 5. Die photograph of the fabricated LNA (total chip area including pads is 0.45 mm^2) and the cryogenic Lakeshore on-wafer measurement setup.



(a) (b)

Fig. 6. S-parameters measured and simulated results at 300K and 4K (a) S_{21} and S_{11}. (b) S_{22} and S_{12}.

III. MEASUREMENT RESULTS AND DISCUSSION

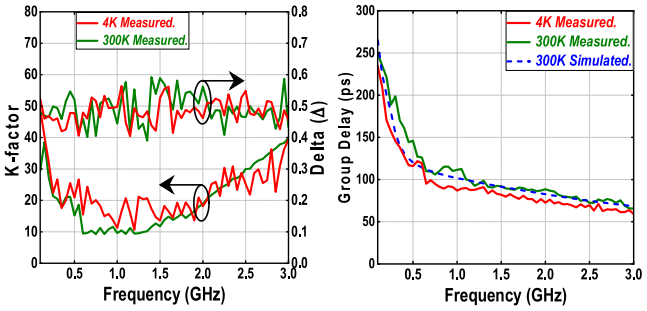
The proposed cryogenic LNA has been designed and fabricated in a bulk 40-nm CMOS technology with an active area of 0.117 mm^2 (390 μm × 300 μm). The chip microphotograph and the cryogenic Lakeshore on-wafer measurement setup are shown in Fig. 5.

S-parameters of the proposed LNA at the RT were measured by on-wafer probing by a Keysight vector network analyzer (PNA-X N5247B), consuming 17.6-mW from a 1.2-V DC power supply. A SOLT (Short-Open-Load-Through) de-embedding technique was used for calibration before real circuit measurements.

At cryogenic temperatures, LNA was measured using a Lakeshore on-wafer CRX-4K probe station for S-parameters measurement by Keysight N5227B PNA. Note that the power consumption of the proposed LNA is decreased to only 8.6 mW at 4 K. Fig. 6(a) and (b) show that at room temperature, LNA attains measured $S_{21,max}$ of 28 dB at 1 GHz over a 3-dB bandwidth of 10 MHz −1.9 GHz close to simulation results. Whereas, the input return loss (S_{11}) is (−21.4 ∼ −15.2 dB) and output return loss (S_{22}) is (−22.5 ∼ −17.6 dB) shows good agreement with the simulated results. While at 4 K, the LNA attains measured $S_{21,max}$ of 31 dB at 0.5 GHz over a 3 dB bandwidth of 10 MHz - 2.6 GHz well match with the simulated results. In addition, the measured result shows that the input return loss (S_{11}) is (−15.3 ∼ −11.6 dB) and S_{22} is (−19.3 ∼ −14.8 dB) and reserve isolation (S_{12}) is better than −60 dB within the 3-dB bandwidth. Fig. 7(a) shows the stability factor (K-factor), which is greater than 9.3 for both RT and 4 K, which indicates that LNA is unconditionally stable at both temperatures. Fig. 7(b) shows the measured results of group delay within the passband, which is less than 250 ps for both RT and 4 K, which is very close to the simulated results. The measured two-tone linearity (IIP3) and 1-dB compression points (input P_{1dB}) versus frequency at 300 K are shown in Fig. 8(a). The minimum IIP3 is −18.6 dBm at 0.5 GHz and the minimum input P1dB is −30 dBm at 1 GHz. It can be seen that the linearity level of LNA is sufficient for the weak reflected power of the quantum devices.

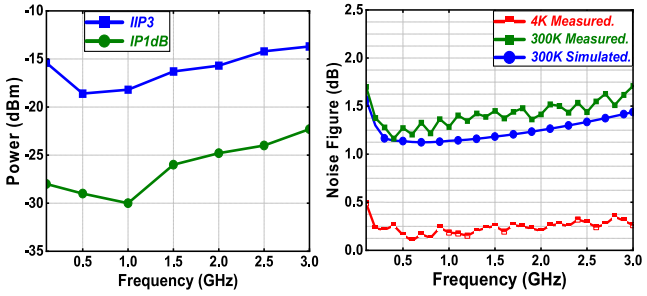
The measured and simulated results of NF at RT and 4K are shown in Fig. 8(b). At RT, LNA was measured by the on-wafer Y-factor method using a Keysight N8975B noise figure analyzer. The LNA achieves NF between (1.16 ∼1.7 dB) with a minimum NF of 1.16 dB at 0.4 GHz, across 3-dB bandwidth of 10 MHz–1.9 GHz. At 4 K, the NF measurement was conducted on-wafer by the Keysight N5242B PNA-X network analyzer with a specially designed GGB microwave probe using a vector-error-corrected cold-source method [19], [20], [21]. Calibration at 4 K was done with GGB CS-5 substrate by moving the reference plane to the probe tips plane, as also cited in [20]. To ensure thermal stability, a pair of copper braids anchored to the sample stage were used and waited for at least 10-15 minutes to cool down the probes. The LNA achieves NF of 0.1–0.48 dB across a 3-dB bandwidth of 0.01–2.6 GHz with a minimum NF of 0.1 dB (6.8 K noise temperature) at 0.6 GHz.

Table II summarizes the performance comparison with other published cryogenic LNAs. Compared to [14], the proposed current reuse topology achieved lower power dissipation,



(a) (b)

Fig. 7. Measured and simulated results at 300K and 4K (a) Stability factor (K-factor) and determinant (Δ). (b) Group delay (GD).



(a) (b)

Fig. 8. (a) Measured IIP3 and P1dB versus frequency at 300 K. (b) Measured and simulated NF at 300K and 4K of the proposed LNA.

and lower NF with a smaller chip area. Also, lower NF and improved input matching both at RT and 4 K with a smaller chip area has been attained compared with [16]. The proposed two-fold current reuse noise-canceling LNA shows low noise figures, high gain, and wide bandwidth under the low power consumption which is among the best compared to the published CMOS LNAs.

IV. Conclusion

In this brief, we present a 10 MHz–2.6 GHz wideband cryogenic LNA in 40-nm CMOS. A novel two-fold current reuse and double noise-canceling topology was proposed for the inverter-based input stage and dual-path noise-canceling auxiliary stage. In addition, LNA is also incorporated with self-body bias configuration at the input stage to compensate for threshold voltage improvement and mitigate the output impedance degradation at cryogenic temperatures. At 4 K, the LNA achieved a maximum gain of 31 dB with a minimum noise figure of 0.1 dB within a 3-dB bandwidth of 10 MHz - 2.6 GHz, under a power consumption of 8.6 mW, while the chip occupies a core area of 0.117 mm^2. The proposed LNA design exhibits promising performance, making it suitable for practical quantum computing applications.

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References

[1] E. Charbon, "Cryo-CMOS electronics for quantum computing: Bringing classical electronics closer to qubits in space and temperature," *IEEE Solid-State Circuit Mag.*, vol. 13, no. 2, pp. 64–68, Jun. 2021.
[2] B. Patra et al., "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018.
[3] A. Ruffini, Y. Peng, T.-Y. Yang, J. Michniewicz, M. F. G. Zalba, and E. Charbon, "A fully-integrated 40-nm 5-6.5 GHzCryo-CMOS system-on-chip with I/Q receiver and frequency synthesizer for scalable multiplexed readout of quantum dots," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, vol. 64, 2021, pp. 210–212.
[4] B. Pabowo et al., "A 6-to-8 GHz0.17mW/qubit cryo-CMOS receiver for multiple spin qubit readout in 40nm CMOS technology," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, vol. 64, 2021, pp. 212–214.
[5] S. J. Puka et al., "A cryogenic CMOS chip for generating control signals for multiple qubits," *Nat. Electron.*, vol. 4, pp. 64–70, Jan. 2021.
[6] S. Pellerano et al., "Cryogenic CMOS for qubit control and readout," in *Proc. IEEE Custom Int. Circuit Conf.*, 2022, pp. 1–8.
[7] F. Sebastiano et al., "Cryo-CMOS interfaces for large-scale quantum computers," in *Proc. IEEE Int. Electron Devices Meet. (IEDM)*, 2020, pp. 25.2.1–25.2.4.
[8] J. C. Bardin et al., "Design and characterization of a 28-nm bulk-CMOS cryogenic quantum controller dissipating less than 2 mWat 3 K," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3043–3060, Nov. 2019.
[9] J. Aumentado, "Superconducting parametric amplifiers: the state of the art in Josephson parametric amplifiers," *IEEE Microw. Mag.*, vol. 21, no. 8, pp. 45–59, Aug. 2020.
[10] S. Schaal et al., "Fast gate-based readout of silicon quantum dots using Josephson parametric amplification," *Phys. Rev. Lett.*, vol. 124, no. 6, Feb. 2020, Art. no. 67701.
[11] F. Heinz, F. Thome, and A. Leuther, "Monolithically integrated C-band low-noise amplifier for use in cryogenic large-scale RF systems," *IEEE Trans. Microw. Theory Techn.*, early access, Dec. 18, 2023, doi: 10.1109/TMTT.2023.3340519.
[12] E. Cha et al., "0.3-14 and 16-28 GHz wide-bandwidth cryogenic MMIC low-noise amplifiers," *IEEE Trans. Microw. Theory Techn*, vol. 66, no. 11 pp. 4860–4869, Nov. 2018.
[13] M. Hosseini and J. C. Bardin, "A 1 mW 0.1–3 GHz cryogenic SiGe LNA with an average noise temperature of 4.6 K," in *Proc. IEEE Int. Microw. Symp. (IMS)*, 2021, pp. 896–899.
[14] Y. Peng, A. Ruffino, and E. Charbon, "A cryogenic broadband sub-1-dB NF CMOS low noise amplifier for quantum applications," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2040–2053, Jul. 2021.
[15] M. K. Chaubey, Y. Liu, P.-C. Wu, H.-H. Tsai, and S. S. H. Hsu, "A miniature 10 MHz 3 GHz sub-1-dB NF cryogenic inductorless noise-canceling low-noise amplifier for qubit readout," in *Proc. IEEE Int. Microw. Symp. (IMS)*, 2023, pp. 668–671.
[16] A. Caglar, S. V. Winckel, S. Brebels, P. Wambacq, and J. Craninckx "Design and analysis of a 4.2 mW4 K 6-8 GHz CMOS LNA for superconducting qubit readout," *IEEE J. Solid-State Circuits.*, vol. 58, no. 9, pp. 1586–1596, Jun. 2023.
[17] M. Rahman and R. Harjani, "A 2.4 GHz, sub-1-V, 2.8-dB NF, 475-W dual-path noise and nonlinearity canceling LNA for ultra-low-power radios," *IEEE J. Solid-State Circuits.*, vol. 53, no. 5, pp. 1423–1430, May 2018.
[18] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and compact modeling of nanometer cmos transistors at deep-cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 996–1006, 2018.
[19] *High-Accuracy Noise Figure Measurements Using the PNA-X Series Network Analyzer (AN1408-20)*, Keysight Technol., Inc., Santa Rosa, CA, USA, Aug. 2014.
[20] *Microwave Measurements with Lake Shore Probe Stations*, Lake Shore Cryotron. Inc., Westerville, OH, USA, Jun. 2007.
[21] R. Hu and S. Weinreb, "A novel wide-band noise-parameter measurements method and its cryogenic application," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 5, pp. 1498–1507, May 2004.
[22] A. Sheldon and L. Belostotski, "A cryo-CMOS low-noise amplifier with 2.3-to-8.5-K noise temperature at 20 K for highly integrated radio-astronomy receivers," *IEEE Microw. Wireless Compon. Lett*, vol. 32, no. 11, pp. 1319–1322, Nov. 2022.