A Transformer-Based Current-Reuse QVCO With an FoM Up to −200.5 dBc/Hz

Ping-Yi Wang, Guan-Yu Su, Yin-Cheng Chang, Da-Chiang Chang, and Shawn S. H. Hsu, *Member, IEEE*

***Abstract*—A high performance X-band quadrature voltage-controlled oscillator (QVCO) is presented. The transformer feedback topology is proposed to combine with the interactive self-switching current bias technique, which can achieve a low phase noise while maintaining low power consumption simultaneously. The measured phase noise is −123.84 dBc/Hz at 1-MHz offset with a 10.56 GHz carrier frequency and the IQ phase error is less than 1.9°. Under a power consumption of 2.4 mW, the proposed QVCO in 0.18-μm CMOS achieves an excellent FoM up to −200.5 dBc/Hz, which is among the best compared with previous works using a similar technology.**

***Index Terms*—Quadrature voltage-controlled oscillator (QVCO), current-reuse, transformer feedback, self-switching biasing.**

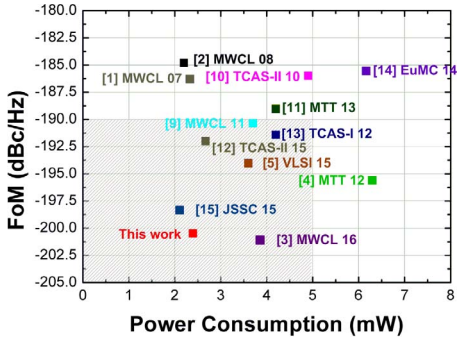

Fig. 1. Trend and performance comparison of low power QVCOs in the literature.

I. Introduction

MODERN RF transceivers using the direct conversion architecture require oscillators possessing accurate quadrature signals with low phase noise. Therefore, the quadrature voltage-controlled oscillator (QVCO) plays a key role to achieve high performance wireless communication systems. Different circuit topologies have been reported for the QVCO with a small phase error and a low phase noise [1]–[6]. The additional coupling transistors employed in conventional QVCO design introduces extra noise sources, resulting in poor phase noise performance. In addition, a tradeoff exists between the phase noise and phase error due to the coupling strength of transistors. Note that the coupling strength is defined as the width ratio of the coupled transistor to the core transistor in the conventional QVCO topology [6]. The drain-to-source feedback was proposed using a transformer for signal coupling in the QVCO for low power and low phase noise operation [4]. The current reuse topology was also employed for QVCO applications, which uses cross-coupled pairs with stacked nMOS and pMOS to reduce the power consumption. However, this configuration still suffers from flicker noise due to the constant current flow in the dc path. One recent study reported the interactive current reuse (ICR) topology with capacitor coupling self-switching sinusoidal current biasing (CSSCB) [5]. By self-switching of the tail current, flicker noise generated from the current source can be alleviated. In addition, using the sinusoidal signal for oscillator biasing can further enhance the power efficiency of the circuit.

Fig. 1 summaries the figure of merit (FoM) of the published QVCOs with low power dissipation based on measured results, where the patterned area indicates the circuits can operate below 5 mW and achieve an FoM up to −190 dBc/Hz.

In this brief, we propose an effective QVCO topology by combining both current-reuse with self-switching bias and the transformer feedback technique to achieve low phase noise and low power operation simultaneously. A 10-GHz QVCO is demonstrated in a standard CMOS process, which could be used for various X-band applications such as satellite communications and radars. The proposed design shows an improved FoM up to −200.5 dBc/Hz, compared with previously reported results using the same process technology. This brief is organized as follows. Section II describes the design concept and analysis of proposed QVCO. Measured results are shown in Section III, and Section IV concludes this brief.

II. Circuit Design and Analysis

Fig. 2(a) shows the proposed QVCO topology, which consists of stacked transistors ($M_{P1,2}$ and $M_{N1,2}$) as the current reuse core, the capacitors C_C to couple the signal, and the differential transformers (T_F) for feedback. With the pMOS and nMOS stacked in a single current path, the power dissipation can be reduced effectively, while maintaining the low phase noise characteristics. Also, the generation of quadrature phase is achieved through the coupling capacitor with negligible extra noise sources. The main idea of CSSCB operation is the transistors in one branch will not turn on simultaneously.

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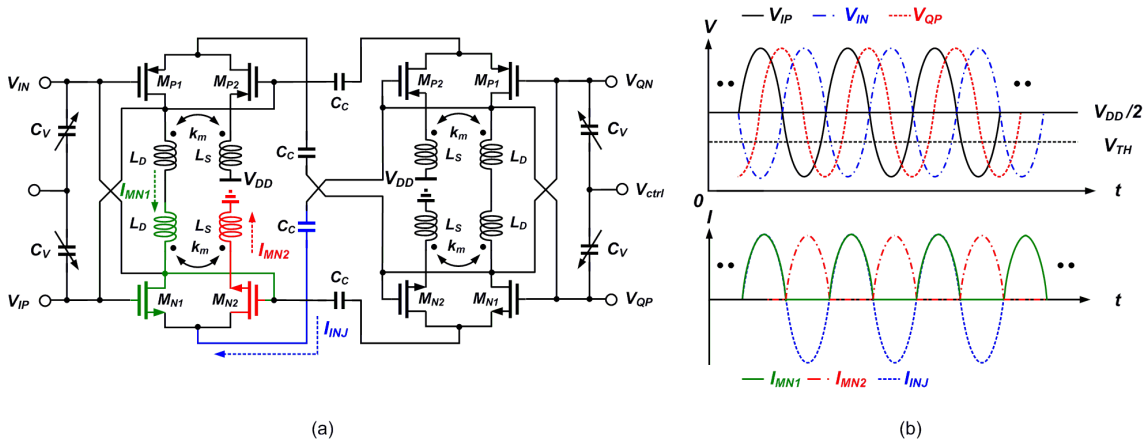

Fig. 2. (a) Circuit topology of the proposed QVCO (buffers not included). (b) Details of voltage and current waveforms during operation.

Fig. 2(b) illustrates the dependence of voltage and current waveforms, where I_{MN1} and I_{MN2} always alternately turn on resulting in the sinusoidal current biasing provided by I_{NJ} [5]. Therefore, no dc current conducting paths exist from power supply to ground, which is more efficient in converting the dc power to the oscillation signal compared with that using a constant current source. In addition, the dynamic switched biasing technique can suppress the flicker noise and improve the phase noise of oscillator. Note that the switched biasing technique can effectively reduce the $1/f$ noise itself of transistor rather than alleviate the effect of $1/f$ noise on circuits. By cycling the bias of MOS transistors from strong inversion to accumulation reduces the intrinsic $1/f$ noise [7]. Compared with the conventional design, the drawbacks in the proposed circuit is the more complicated topology and increased chip area.

The phase noise of oscillator can be estimated as [8]

$$\mathcal{L}(\triangle f) = 10log\left[\frac{2FkT}{P_{sig}}\left(1+\frac{f_c}{2Q\triangle f}\right)^2\right] \tag{1}$$

where k is Boltzmann constant, T is the absolute temperature, Q is the quality factor of LC tank, Δf is the offset frequency, and F is the device excess noise factor. The phase noise reduces with increased output signal power P_{sig} and the quality factor Q of LC tank. The transformer feedback topology used in QVCO cores allows enhancing the output voltage swing at low dc supply voltage. Also, properly designed transformers can have improved quality factor Q compared with two individual spiral inductors. In addition, it is also very critical to maintain high tank impedance to have large output swing for low phase noise. In the proposed topology, if both M_1 (M_{N1} and M_{P1}) and M_2 (M_{N2} and M_{P2}) are biased in the saturation region, the impedance looking into the LC tank $|\mathrm{Z_{tank}}|$ can reach a very high value due to the stacked configuration. However, the contribution of thermal noise from M_2 to the oscillator phase noise is also large. Differing from the typical design with all of the transistors of QVCO biased in the saturation region, the transistors M_2 are biased in the linear region on purpose to reduce phase noise in our design. With the reduced equivalent resistance as operated in the linear region, the transistor thermal noise voltage reduces to only $4kTR$, where R is in the range of tens of ohms, resulting in improved phase noise. It should be emphasized that $|\mathrm{Z_{tank}}|$ still maintains a very high value even M_2 operating in the linear region as can be verified by simulation. Fig. 3 compares the simulated tank impedances (half circuit) with four different circuit topologies, labeled as case I, II, III, and IV. As shown in the figure, case I and II are both with two individual inductors, while M_{N2} and M_{P2} are added in case II. In contrast, case III and IV are corresponding to case I and II but the inductors are replaced by transformers. The simulated results indicate that $|\mathrm{Z_{tank}}|$ increases by more than four times using the proposed configuration compared with that without M_2 and transformer. Note that the oscillation frequency, passive components, and dc power consumption are all identical. It should be mentioned that although the initial bias of the core transistors M_{N1} and M_{P1} are in the saturation region, these transistors could also enter the triode region during switching operation of QVCO, which can be observed in simulation.

Fig. 4 shows the simplified half circuit of the proposed QVCO to determine the startup condition and oscillation frequency, where R_{D} and R_{S} represent the loss of transformers. R_{M} functions as a variable resistor (M_2 operated in the linear region) and can be adjusted by the output voltage v_{O}. C_D is the equivalent output capacitance including MOS varactor C_{V} and parasitic capacitance C_{P}. By applying Kirchhoff's current law at the drain and source terminals,

$$v_o\left(\frac{1}{sL_D}+\frac{1}{R_D}\right) = i_d + \frac{M}{L_D}i_s \tag{2}$$

$$v_s\left(\frac{1}{sL_s+R_M+R_s}\right) = i_s + \frac{M}{L_s}i_d \tag{3}$$

$$i_d = -G_m(v_i - v_s) - sC_D v_o \tag{4}$$

$$i_s = G_m(v_i - v_s) \tag{5}$$

where M is the mutual inductance between the L_{D} and L_{S}. To simplify the analysis, the parasitic resistance R_{S} and the linear region resistance R_{M} are neglected. Also, if $G_m(L_s - M) \ll C_D R_D$, the transfer function can be approximated as

$$\frac{v_o}{v_i}(s) \approx \frac{sG_mR_DL_D\left(\frac{k_m}{N}-1\right)}{s^2R_DL_DC_D + s\left[G_mR_DL_D\left(\frac{k_m^2}{N^2}-\frac{k_m}{N}\right)+L_D\right]+R_D} \tag{6}$$

$$k_m = \frac{M}{\sqrt{L_DL_s}},\ N = \sqrt{\frac{L_D}{L_s}},\ and\ G_m = 2\frac{G_{mn}G_{mp}}{G_{mn}+G_{mp}} \tag{7}$$

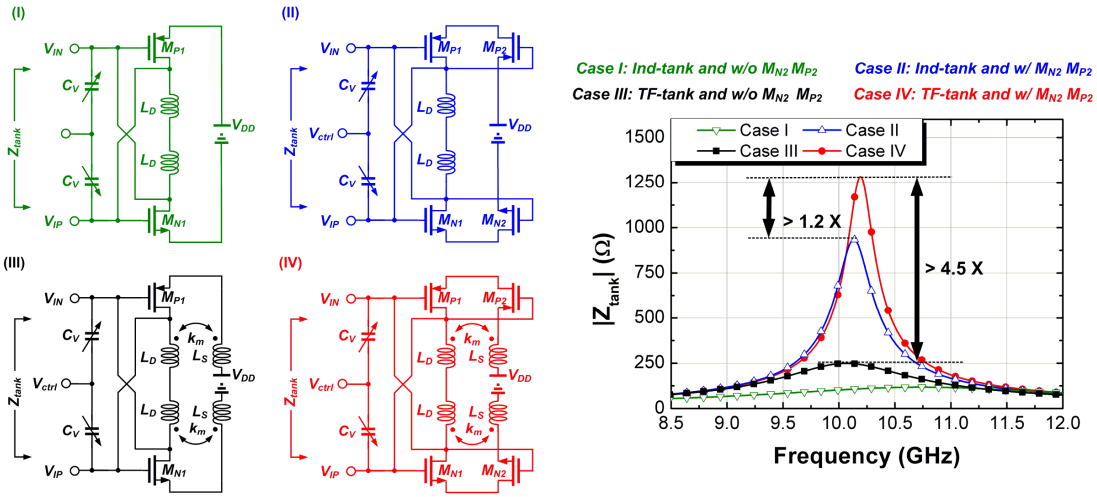

Fig. 3. Simulated magnitude response of tank impedance for different QVCO topologies.

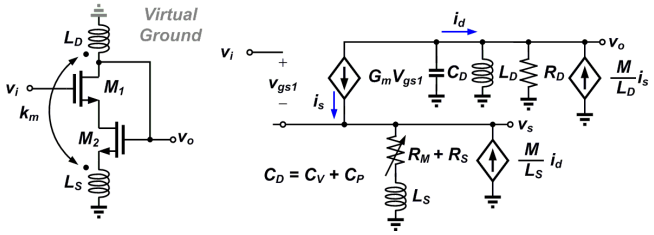

Fig. 4. Simplified small-signal equivalent circuit analysis.

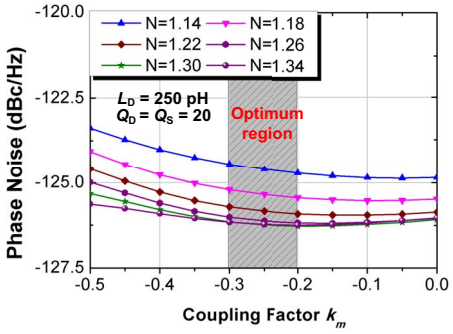

Fig. 5. Simulated phase noise of proposed QVCO versus N for different k_m.

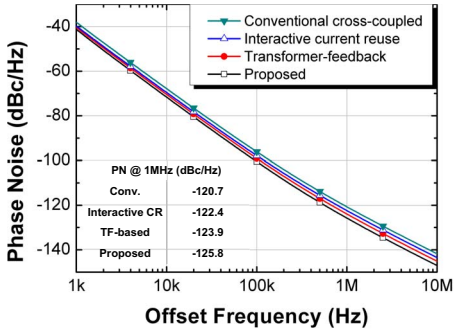

Fig. 6. Comparison of simulated phase noise for four different QVCO topologies.

where k_m and N are the coupling factor and turn ratio of the transformer, and G_{mn} and G_{mp} are the transconductances of the nMOS and pMOS, respectively. To solve the amplitude transfer function as unity, the oscillation frequency and startup condition can be obtained as

$$\omega_o \approx \sqrt{C_D L_D}, \text{ and } G_m R_D \geq 1/[1-(k_m/N)^2] \quad (8)$$

As can be seen, the oscillation frequency is mainly determined by the drain inductance and capacitance at the output node. Also, the coupling factor k_m and turn ratio N are critical to determine the required startup condition, which can be relaxed by reducing coupling factor or increasing turn ratio. The k_m and N are determined by simulation to achieve optimum phase noise in practical design. Fig. 5 shows the simulated dependence of phase noise (1-MHz offset) of QVCO on k_m and N. The optimum k ranges from −0.2 to −0.3 for low phase noise.

The ratio of (G_m/I_D) is also investigated for determining the transistors sizes and bias points to further reduce the power consumption with low phase noise, where G_m is the transistor transconductance. Assuming the transistor size is fixed, a high (G_m/I_D) ratio is preferred for low power operation, which can be obtained by reducing the overdrive voltage but at the expense of a lower unity current-gain frequency f_T of the device.

Therefore, we select relatively large transistor sizes to have sufficient G_m and keep lower overdrive voltage. As a result, low power operation of the circuit can be maintained, but the frequency tuning range becomes limited due to increased parasitic capacitances of the LC tank. The wider tuning range could be achieved if larger MOS varactors or multi-bit capacitor bank are employed in the tank design. Finally, the dimension of M_P is chosen to be about two times of M_N for symmetric rise time and fall time. Fig. 6 shows the simulated results for the phase noise to investigate the effectiveness of the applied design techniques. Compared with the conventional cross-coupled topology, the phase noise reduced by interactive current reuse is 1.7 dB, while that comes from transformer feedback can be up to 3.2 dB. By combining both techniques with further optimization, the overall phase noise improvement is about 5.1 dB. The results suggest that the transformer feedback technique contributes more than current reuse for the obtained low phase noise and good FoM.

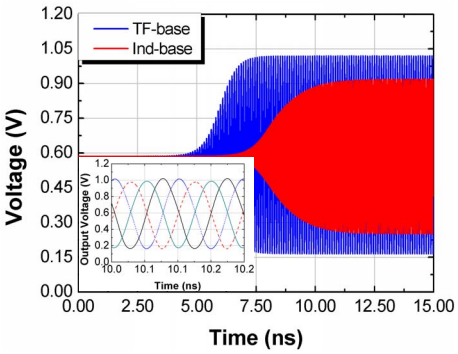

Fig. 7. Simulated QVCO startup behavior and output waveform of IQ signals.

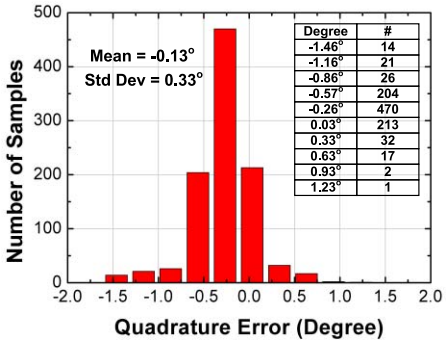

Fig. 8. Quadrature phase error by Monte Carlo simulation.

Fig. 7 shows the simulated waveforms of QVCO, which indicates the circuit requires about 7.5 ns for startup. The figure also presents the design by replacing the transformers with individual inductors. The results show that the output voltage swing increases by more than 30% and also with a reduced startup time in the proposed topology. The inset of Fig. 6 is the quadrature output signal of the proposed QVCO circuit, which indicates an average peak-to-peak amplitude of 0.82 V. To further evaluate the performance of the proposed QVCO, the Monte Carlo simulation is used with a 2 % gate width mismatch of the core device. Fig. 8 shows the quadrature error in the QVCO output nodes for 1000 samples. The simulated results indicate the average quadrature phase error is only around $-0.13°$ with a standard deviation of around 0.33°, and the maximum phase error is about $-1.5°$.

Fig. 9(a) shows the transformer layout in our design. The differential octagonal transformer is used for achieving high quality factor Q with a compact chip area. The line width W of both inner and outer coils are design as 25 μm. In addition, the line spacing is designed as 25 μm with a high self-resonance frequency (f_{SR}). The inner radium R_{ad} of the transformer is 130-μm. The pattern ground shield (PGS) is implemented with meal layer M_1 with 1-μm of both width and spacing to suppress the eddy current from the substrate and further enhance the Q factor of transformer. Note that the Q factor of transformer is defined by the two-port Z-parameters [16]. Based on full-wave EM simulation, L_D, L_S, Q_D, Q_S, k_m at 10 GHz are 238 pH, 153 pH, 23.6, 18.2, and -0.22, respectively, as shown in Fig. 9(b). Also, the MOS varactor is implemented by accumulation-mode devices (A-MOS) with a gate length of 0.5 μm and finger number of 15. The capacitance of varactor is 0.14 to 0.18 pF throughout the entire tuning curve.

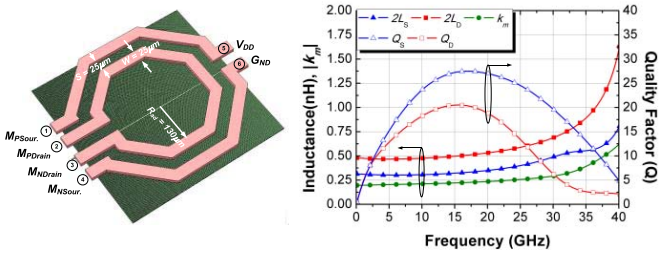

Fig. 9. (a) Layout and (b) simulated results of the proposed transformer.

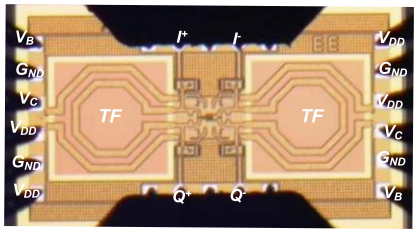

Fig. 10. Chip micrograph of the proposed QVCO.

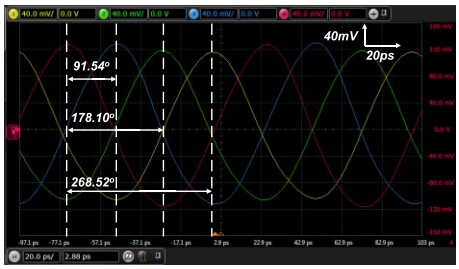

Fig. 11. Measured time domain waveforms.

The coupling capacitance C_C is designed as 0.12 pF to ensure M_{N2} and M_{P2} stay in the linear region.

III. Measured Results and Discussion

The proposed QVCO with both transformer feedback and current reuse techniques was fabricated in a 0.18-μm CMOS process. The chip micrograph is shown in Fig. 10 with a total chip size of 0.84 mm^2 including the RF and dc bias pads (core area: 0.75 mm^2). Under a 1.25-V supply voltage, the power consumption of the QVCO core circuit is only 2.4 mW. Fig. 11 shows the measured results of quadrature signals in time domain, as shown in Fig. 11. The result indicates that the phase errors are less than 1.9 degree including the mismatches in output buffers and cables. Fig. 12(a) shows the measured phase noise and output power of -123.84 dBc/Hz (1-MHz offset) at 10.56-GHz and -8.5 dBm, respectively. Fig. 12(b) shows the frequency tuning range of about 560-MHz over the control voltage V_{crtl}. Also, the phase noises are better than -120.5 dBc/Hz at 1-MHz offset and -95.1 dBc/Hz at 100-kHz offset when V_{crtl} varies from 0 to 1.8 V. Compared with previously reported measured results as shown in Table I, the proposed QVCO demonstrates an excellent phase noise. The FoM is also among the best compared with the reported results. It should be mentioned that a good power supply ripple rejection ratio (PSRR) about 50 dB can be achieved below 10 MHz based on simulation.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

Ref.	Technology	P_{diss} (mW)	Freq. (GHz)	Q factor TF/Ind.	Tuning Rang (%)	Phase Noise 1MHz (dBc/Hz)	FoM 100 kHz/1 MHz (dBc/Hz)	Phase Error (Degree)	Area(mm^2)
[2]	0.18 μm	2.2	7.13	15	4.6	-111.2	-177.6/-184.8	< 2	0.48[+]
[5]	0.18 μm	3.6	5.08	--	9.45	-125.84	-- /-194.0	–	0.93
[9]	0.18 μm	3.7	4.04	--	8.91	-123.42	-- /-190.4	< 0.48	0.58
[10]	0.18 μm	4.9	2.34	--	15	-126.11	-179.8[*]/-186	< 6	0.94
[12]	0.18 μm	2.67	2.39	--	13.46	-128.65	-183.4/-192	< 2	3.78
This work	0.18 μm	2.4	10.56	23.6	5.46	-123.84	-194.6/-200.5	< 1.9	0.75[+]

$\mathrm{FoM} = \mathrm{PN} - 20\log(f_{\mathrm{osc}}/\Delta\mathrm{f}) + 10\log(P/1\mathrm{mW})$; [+]core circuit; [*]estimated from measured results.

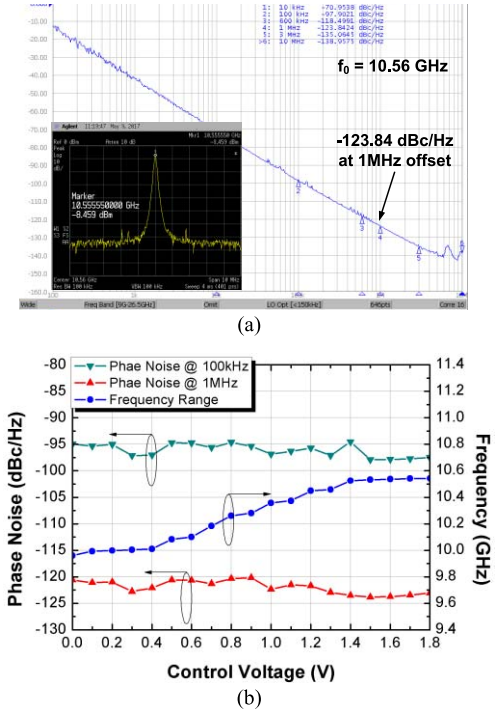

Fig. 12. Measured results of (a) phase noise and spectrum (b) phase noise and frequency tuning range verse control voltage.

The PSRR starts to degrade at higher frequencies, which could be attributed to the parasitic capacitances of the circuit.

IV. CONCLUSION

This brief successfully demonstrated an X-band QVCO with an excellent FoM up to −200.5 dBc/Hz. The proposed QVCO combined the current-reuse topology with interactive self-switching bias and the transformer feedback. The design methodologies were discussed for achieving low phase noise and low power operation simultaneously. The measured phase noise is −123.84 dBc/Hz at 1-MHz offset under a power consumption of only 2.4 mW. The proposed QVCO is suitable for high performance RF transceiver applications.

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REFERENCES

[1] J.-P. Hong, S.-J. Yun, N.-J. Oh, and S.-G. Lee, "A 2.2-mW backgate coupled LC quadrature VCO with current reused structure," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 4, pp. 298–300, Apr. 2007.

[2] T.-H. Huang and Y.-R. Tseng, "A 1 V 2.2 mW 7 GHz CMOS quadrature VCO using current-reuse and cross-coupled transformer-feedback technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 10, pp. 698–701, Oct. 2008.

[3] M. Jalalifar and G.-S. Byun, "A current-reused back-gate coupling QVCO using transformer feedback structure," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 7, pp. 534–536, Jul. 2016.

[4] H.-Y. Chang and Y.-T. Chiu, "K-band CMOS differential and quadrature voltage-controlled oscillators for low phase-noise and low-power applications," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 1, pp. 46–59, Jan. 2012.

[5] K.-I. Wu, I.-S. Shen, C. F. Jou, and C. C.-P. Chen, "A–194 dBc/Hz FOM interactive current-reused QVCO (ICR-QVCO) with capacitor-coupling self-switching sinusoidal current biasing (CSSCB) phase noise reduction technique," in *VLSI Circuits Dig. Symp.*, Kyoto, Japan, Jun. 2015, pp. 236–237.

[6] P. Andreani, A. Bonfanti, L. Romano, and C. Samori, "Analysis and design of a 1.8-GHz CMOS LC quadrature VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1737–1747, Dec. 2002.

[7] E. A. M. Klumperink, S. L. J. Gierkink, A. P. van der Wel, and B. Nauta, "Reducing MOSFET 1/*f* noise and power consumption by switched biasing," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 994–1001, Jul. 2000.

[8] G. D. Vendelin, *Microwave Circuit Design Using Linear and Nonlinear Techniques*, 2nd ed. New York, NY, USA: Wiley, 2005, ch. 10.

[9] S.-L. Jang, C.-C. Shih, C.-C. Liu, C.-W. Chang, and C.-W. Hsue, "CMOS quadrature VCOs using the varactor coupling technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 9, pp. 498–500, Sep. 2011.

[10] S.-Y. Lee, L.-H. Wang, and Y.-H. Lin, "A CMOS quadrature VCO with subharmonic and injection-locked techniques," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 11, pp. 843–847, Nov. 2010.

[11] Y.-C. Lo and J. Silva-Martinez, "A 5-GHz CMOS LC quadrature VCO with dynamic current-clipping coupling to improve phase noise and phase accuracy," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 7, pp. 2632–2640, Jul. 2013.

[12] C.-H. Hong, C.-Y. Wu, and Y.-T. Liao, "Robustness enhancement of a class-C quadrature oscillator using capacitive source degeneration coupling," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 1, pp. 16–20, Jan. 2015.

[13] F. Zhao and F. F. Dai, "A 0.6-V quadrature VCO with enhanced swing and optimized capacitive coupling for phase noise reduction," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 8, pp. 1694–1705, Aug. 2012.

[14] P.-Y. Wang, Y.-C. Chang, K.-H. Chuang, D.-C. Chang, and S. S. H. Hsu, "A low phase-noise 24GHz CMOS quadrature-VCO using pMOS-source-follower coupling technique," in *Proc. Eur. Microw. Conf.*, Rome, Italy, 2014, pp. 572–575.

[15] A. G. Roy, S. Dey, J. B. Goins, T. S. Fiez, and K. Mayaram, "350 mV, 5 GHz class-D enhanced swing differential and quadrature VCOs in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1883–1847, Aug. 2015.

[16] H. C. Luong and J. Yin, "Transformer design and characterization in CMOS process," in *Transformer-Based Design Techniques for Oscillators and Frequency Dividers.* Cham, Switzerland: Springer, 2016.