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STI-to-gate distance effects on flicker noise characteristics in 0.13 μm CMOS

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ABSTRACT

The geometry effect on the flicker noise characteristics and the variations in 0.13 μm CMOS transistors were studied. By symmetrically extending the distance between the shallow-trench-isolation (STI) to the gate, both NMOS and PMOS presented obvious improvement on the noise characteristics. As the distance increased from 0.6 μm to 10 μm, the average noise level reduced by more than one order of magnitude (NMOS) and the standard deviations σ_{dB} improved from 5.95 dB to 1.79 dB for NMOS and from 3.93 dB to 2.17 dB for PMOS, respectively. To further identify the noise mechanism, the devices with asymmetrical STI-to-gate distances were also investigated. It was found that the distance in the source side (*SA*) has a much higher impact on the observed noise characteristics. The results suggested that the noise characteristics were dominated by the STI stress induced traps for both NMOS and PMOS studied here. In addition, the carrier number fluctuation model with the correlated mobility scattering could be more suitable to describe the noise characteristics in these devices.

1. Introduction

In recent years, the shallow-trench-isolation (STI) is being extensively employed in the CMOS process to improve the isolation between the devices. As the device technology keeps advancing, the MOSFET characteristics have become very sensitive to the compressive stress introduced by the STI. It has been found that the device DC characteristics, e.g., threshold voltage (*V*th), transconductance (g_m), leakage current and drain current (I_{DS}) are all affected by the STI [1–4]. The compressive stress resulted from STI and the stress-control layers on flicker noise in CMOS have also been studied previously [5–6]. In addition, the device geometries can be crucial to the low-frequency noise characteristics under the impact of STI [7–8].

In this work, we study the 0.13 μm RF CMOS transistors with both symmetrical and asymmetrical layouts regarding various STI spaces. By extending the STI-to-gate space, the flicker noise level and the corresponding variation reduce significantly. To further investigate the impact of STI stress on the devices, the devices with asymmetrical layouts are designed to identify the flicker noise mechanisms. Each device type from many different chips is measured to obtain a statistical conclusion.

This paper is organized as follows. Section 2 describes the device layouts and the test structure. Section 3 presents the experimental results and discussion, including the *V*th, g_m, I_{DS}, flicker noise characteristics, and the noise variation model. Section 4 concludes this work.

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2. Devices layout design

Fig. 1 shows the typical layout of a MOSFET and the active region is surrounded by the STI structure, where *SA* and *SB* are defined as the distances from the gate edge to the STI for the source and drain sides, respectively. By changing the *SA*(*SB*) distance, the associated compressive stress introduced by STI in the active region can be different. Three STI-to-gate distances for symmetrical layout (*SA* = *SB*) of 0.6 μm (minimum rule), 1.2 μm, and 10 μm, and the asymmetrical structures (*SA* ≠ *SB*) of 0.6 μm/10 μm were designed. Both NMOS and PMOS used in this study were fabricated by a standard 0.13 μm CMOS process, with a gate oxide thickness of ~26 Å, and the *V*th of ~0.4 V. Table 1 lists all the device sizes under test and a fixed W/L = 10/0.13 (N_{finger} = 1) is employed for a fair comparison.

The test structure used in this study is GSG (ground-signal-ground) RF pads. Since the nanometer-scale devices often have very high low-frequency gain, the low-impedance RF terminals (50 ohm) can prevent the oscillation problems to obtain more reliable data. The flicker noise measurement setup in this work is depicted as described in [7]. The measurements are performed in a range of 10 Hz–100 KHz, and the noise floor of the system is well below the tested devices in the measured frequency range.

3. Results and discussion

3.1. DC characteristics

Fig. 2 shows the threshold voltages for the three designs of symmetrical devices (*SA* = *SB*). The results indicate that the average

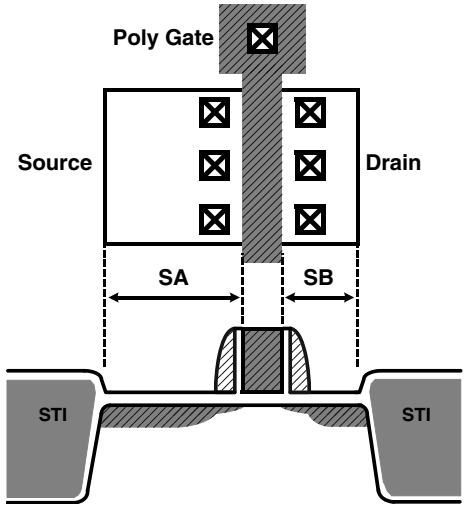

Fig. 1. Typical layout of a MOSFET surrounded by the STI structure and the corresponding cross section, where *SA*(*SB*) is the gate-to-STI distance.

Table 1
Different devices under test in this study

W/L = 10/0.13 (N_{finger} = 1)	Symmetrical devices		Asymmetrical devices	
	SA (μm)	*SB* (μm)	*SA* (μm)	*SB* (μm)
NMOS	0.6	0.6	0.6	10
	1.2	1.2	10	0.6
	10	10	–	–
PMOS	0.6	0.6	–	–
	1.2	1.2	–	–
	10	10	–	–

|*V*th| (five devices) shifts ~18 mV for NMOS and ~6.5 mV for PMOS, as *SA*(*SB*) reduces from 10 μm to 0.6 μm. The main reason can be attributed to the STI stress induced substrate doping modulation. As the STI edge becomes closer to the channel, the pocket implant (or halo implant) is affected by the stress leading to a higher effective substrate doping concentration [9–10] and therefore increased |*V*th| for both NMOS and PMOS.

Fig. 3 presents the transconductance (g_m) changes as a function of V_{GS} in the triode region, and an opposite trend can be observed for NMOS and PMOS. The maximum g_m of NMOS degrades by ~10%, while that of PMOS improves by ~12%, which can be explained by the following equation

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}\bigg|\text{triode region} = \mu_{eff} C_{ox} \frac{W}{L} V_{DS} \propto \mu_{eff} \quad (1)$$

where μ_{eff} is the effective carrier mobility. For a fixed V_{DS}, the change of g_m can be mainly attributed from the affected mobility due to the STI stress [11]. For NMOS devices, the compressive stress degrades the carrier mobility, while that improves the mobility for PMOS. Similar trends are also observed in the DC *I–V* characteristics. With the compressive stress, the split valance band results in light-hole-like energy levels leading to reduced hole effective mass and enhanced mobility in PMOS. Oppositely, the stress induced phonon scattering increases electron effective mass and thus the reduced mobility in NMOS [11].

Above discussions indicate that the devices with different STI-to-gate distances present different DC characteristics. Detailed investigations on flicker noise characteristics for different device geometries will be carried out in the following sections.

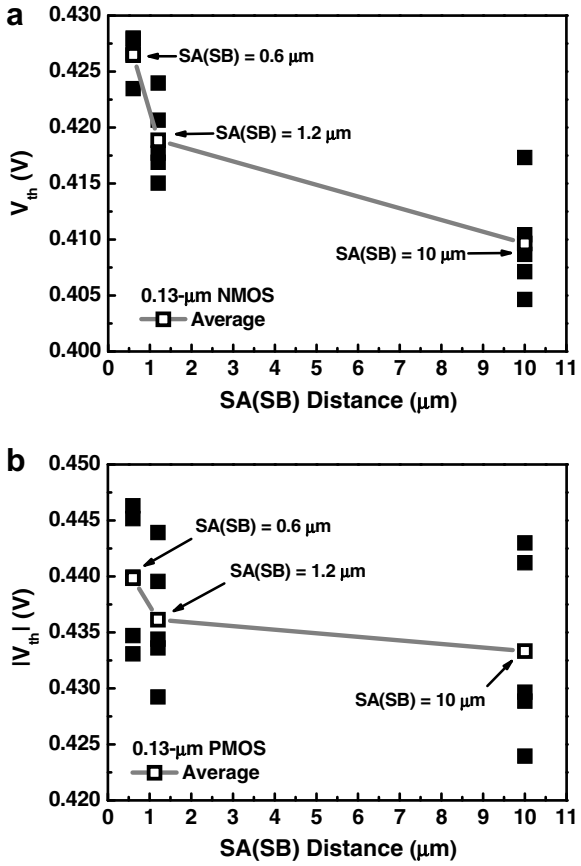

Fig. 2. Experimental results of |*V*th| as a function of the STI-to-gate distance *SA*(*SB*) for 0.13 μm (a) NMOS, and (b) PMOS.

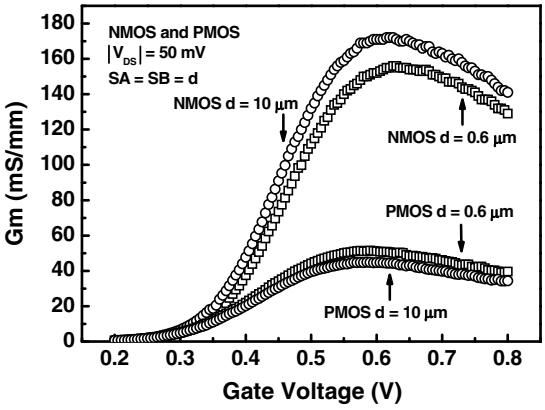

Fig. 3. Dependence of the transconductance g_m on the STI-to-gate distance *SA*(*SB*) for both 0.13 μm NMOS and PMOS.

3.2. Flicker noise characteristics

3.2.1. Symmetrical devices

Both carrier number fluctuation and mobility fluctuation models were employed to explain the flicker noise mechanisms in MOSFETs [12–19]. For NMOS transistors, the origin of the flicker noise was mainly attributed to the carrier number fluctuation [18–19]. However, some of the studies suggested that the mobility fluctuation model may be more suitable for PMOS [17,20]. Compared with the previous studies, it is even more interesting to clarify this point here since the STI effect has an impact on the carrier

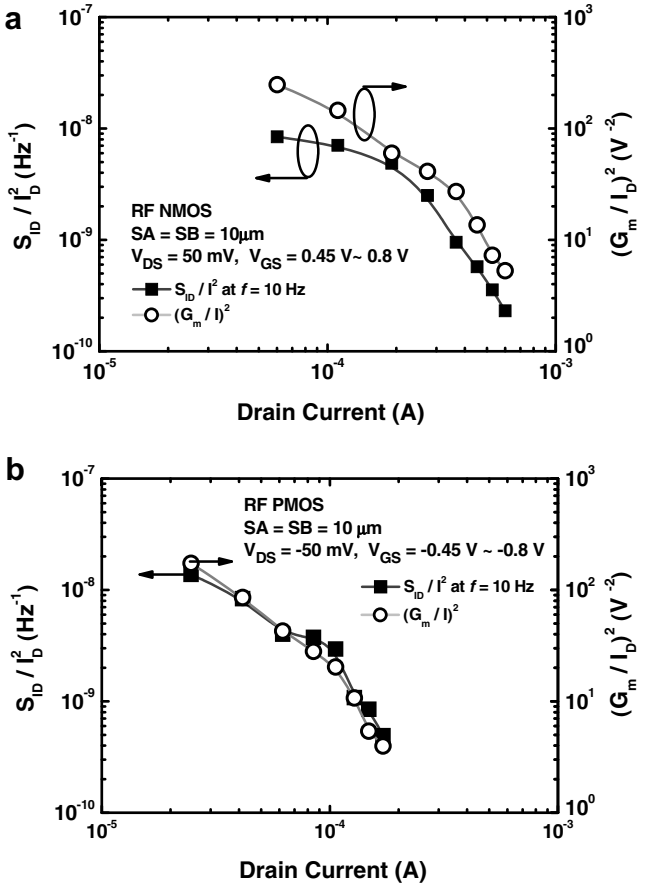

Fig. 4. Noise current spectral density S_{ID}/I^2 at 10 Hz and $(g_m/I_D)^2$ as a function of the drain current for 0.13 μm (a) NMOS, and (b) PMOS with $SA(SB)$ = 10 μm. Both devices are biased under $|V_{DS}|$ of 50 mV and $|V_{GS}|$ from 0.45 V to 0.8 V (50 mV/step).

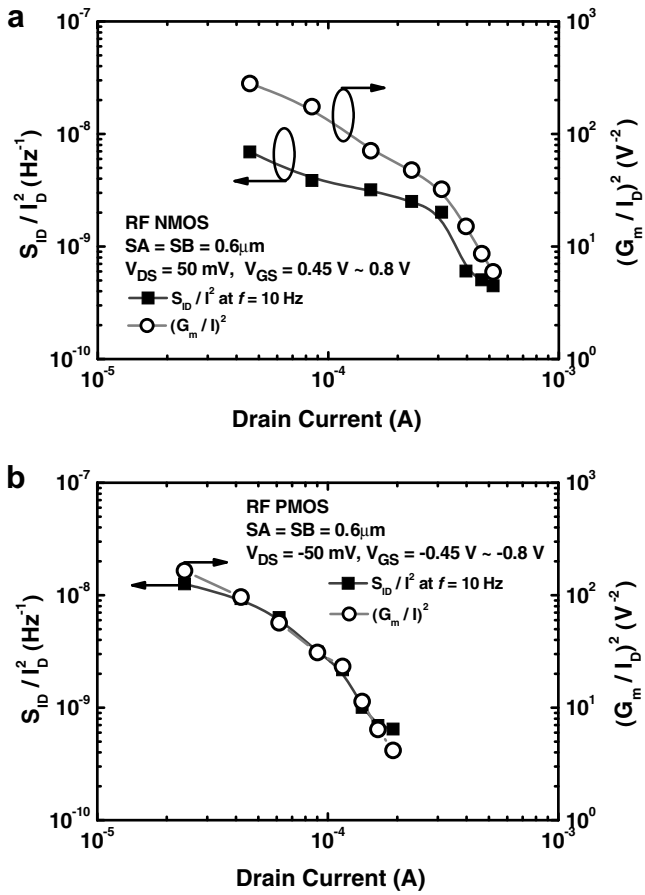

Fig. 5. Noise current spectral density S_{ID}/I^2 at 10 Hz and $(g_m/I_D)^2$ as a function of the drain current for 0.13 μm (a) NMOS, and (b) PMOS with $SA(SB)$ = 0.6 μm. Both devices are biased under $|V_{DS}|$ of 50 mV and $|V_{GS}|$ from 0.45 V to 0.8 V (50 mV/step).

mobility and also introduces traps simultaneously. Both types of devices were measured in the triode region (V_{DS} = 50 mV) to identify the flicker noise mechanisms. Fig. 4(a) and (b) plots the S_{ID}/I^2 curves versus $(g_m/I)^2$ for NMOS and PMOS ($SA = SB$ = 10 μm), respectively. As can be seen, these two curves follow the same trend when the drain current increases, which indicates that the carrier number fluctuation model is more suitable in both cases [21]. The results suggest that although the STI stress affects the carrier mobility, the main flicker noise mechanism is still the carrier number fluctuation. Fig. 5(a) and (b) shows the results for NMOS and PMOS of $SA = SB$ = 0.6 μm, respectively. Notice that a discrepancy between the S_{ID}/I^2 and the $(g_m/I)^2$ curves in both figures can be observed as the devices enter the high-current region, which can be explained by the following equation [21]

$$\frac{S_{ID}}{I_D^2} = \left[1 \pm \alpha\mu_{eff} C_{ox} \frac{I_D}{g_m}\right]^2 \frac{g_m^2}{I_D^2} S_{vfb}(f) \quad (2)$$

where α is the scattering parameter, μ_{eff} is the effective carrier mobility, and the S_{vfb} is flatband voltage spectral density [17]. As indicated in (2), the number fluctuation could induce correlated mobility scattering. As a result, when $SA(SB)$ becomes very small and with more effective traps, this effect is more significant leading to the deviation of the two curves as observed in Fig. 5.

Fig. 6–8, present the normalized drain noise current spectral densities for symmetrical NMOS devices ($SA(SB)$ = 0.6 μm, 1.2 μm, and 10 μm) biased in the saturation region (V_{DS} of 0.7 V and V_{GS} of 0.7 V). As shown in Fig. 6 with $SA(SB)$ = 0.6 μm, the noise level presents a wide variation up to almost two orders of magnitude

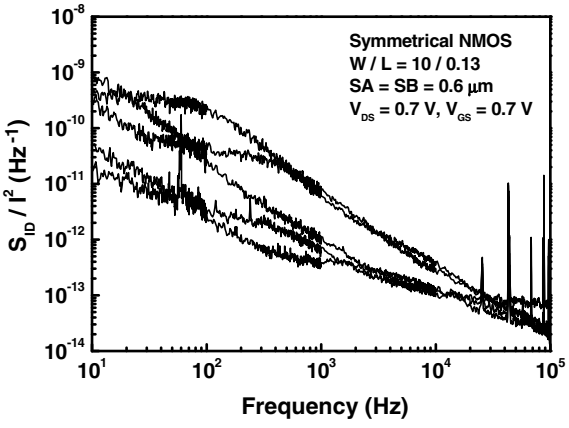

Fig. 6. Normalized noise current spectral density S_{ID}/I^2 for 0.13 μm NMOS with $SA(SB)$ = 0.6 μm under a V_{DS} of 0.7 V and V_{GS} = 0.7 V. The different traces are for different devices with the same W/L = 10/0.13 (N_{finger} = 1).

and obvious G–R components from different devices even under the same bias condition. On the other hand, the noise variation can be effectively reduced when $SA(SB)$ extended to 1.2 μm and beyond (10 μm) as shown in Fig. 7 and Fig. 8, in which the noise level variation is around one order of magnitude for the worst cases, and the G–R noise plateaus are not as obvious as those observed in Fig. 6 for the devices with $SA(SB)$ = 0.6 μm.

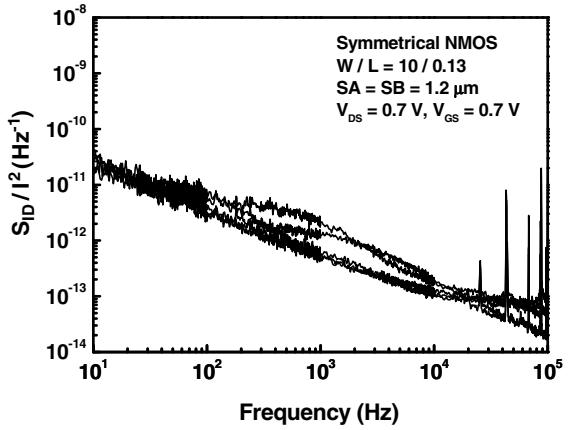

Fig. 7. Normalized noise current spectral density S_{ID}/I^2 for 0.13 μm NMOS with $SA(SB)$ = 1.2 μm under a V_{DS} of 0.7 V and V_{GS} = 0.7 V. The different traces are for different devices with the same W/L = 10/0.13 (N_{finger} = 1).

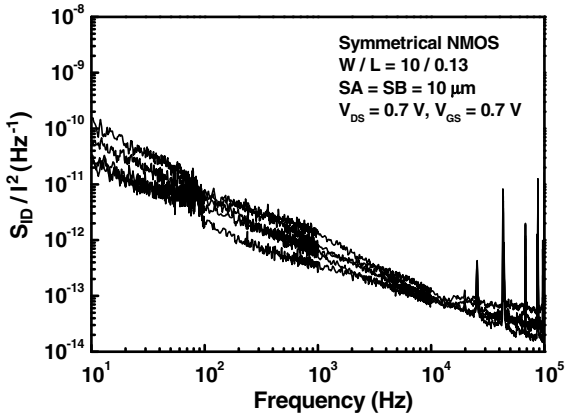

Fig. 8. Normalized noise current spectral density S_{ID}/I^2 for 0.13 μm NMOS with $SA(SB)$ = 10 μm under a V_{DS} of 0.7 V and V_{GS} = 0.7 V. The different traces are for different devices with the same W/L = 10/0.13 (N_{finger} = 1).

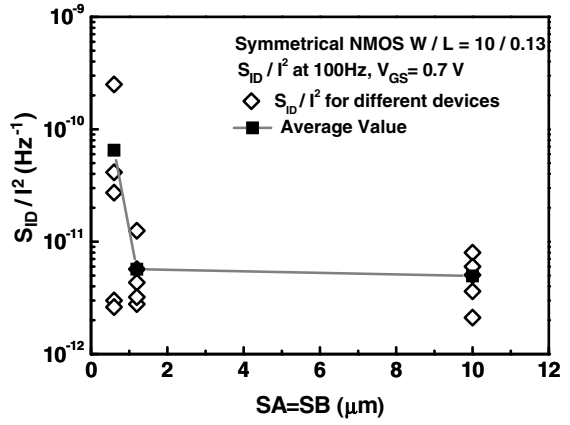

Fig. 9. The normalized noise current spectral density S_{ID}/I^2 at f = 100 Hz for NMOS as a function of the STI-to-gate distance $SA(SB)$. The devices were biased in the saturation region under a fixed V_{DS} of 0.7 V and V_{GS} = 0.7 V. The different points are for different devices with the same W/L = 10/0.13 (N_{finger} = 1).

Fig. 9 plots the noise current spectral density S_{ID}/I^2 at 100 Hz for the three types of NMOS devices together, which indicates that the averaged noise level and noise variation reduce significantly when $SA(SB)$ increases from 0.6 μm to 1.2 μm, while the changes are not that obvious as the $SA(SB)$ further extends to 10 μm. The results suggest that the noise variation and the noise level have a strong dependence on the STI around the active region. With the high compressive stress induced around the STI and the active area boundary, many defects can be generated during the process. The closer distance of STI to the device channel, the more severe effect on the device flicker noise characteristics can be observed. As observed from the experimental results, the $SA(SB)$ distance of 1.2 μm selected in this study seems a transition value for the lowered STI effect, which is consistent with those reported previously [2–3]. According to Miyamoto et al. [2], the simulation results indicated that the compressive stress in the x direction increased rapidly from 450 MPa to 750 MPa when the STI buffer space becomes less than ~1 μm. Also, Gallon et al. [3] showed that the critical distance for the STI having an impact on transistor characteristics onsets also from ~1 μm. The results suggest that the distance of 1.2 μm observed here is most likely a general case. However, this STI stress relax distance may depend on different technologies and better be determined by experiments. Various processes have been proposed to alleviate the STI induced stress in CMOS process [2,5].

The PMOS transistors presented a similar trend with that of NMOS as shown in Fig. 10. As mentioned, some previous studies suggested that the mobility fluctuation may be the dominant factor for PMOS transistors in the strong inversion [16–17]. However, based on the results of Fig. 4(b), Fig. 5(b), and the dependence of $SA(SB)$ on the noise spectral densities in Fig. 10, the noise characteristics of the PMOS transistors are similar with the NMOS devices. In other words, the noise mechanism is better described by the number fluctuation model and the noise characteristics are mainly determined by the STI effect in both types of transistors studied here.

3.2.2. Asymmetrical devices

Fig. 11 shows the normalized drain noise current spectral densities for the asymmetrical NMOS devices with SA = 0.6 μm (source side) and SB = 10 μm (drain side) in the saturation region, and Fig. 12 shows the results for the devices with SA = 10 μm and SB = 0.6 μm. As can be seen, an obvious improvement of noise variation and the reduced G–R noise bulges can be obtained when a large source side extension (SA) was used. Fig. 13 plots the noise current spectral densities at 100 Hz for both cases together. The results clearly indicated that the traps located in the source region have more impacts on the flicker noise characteristics than those

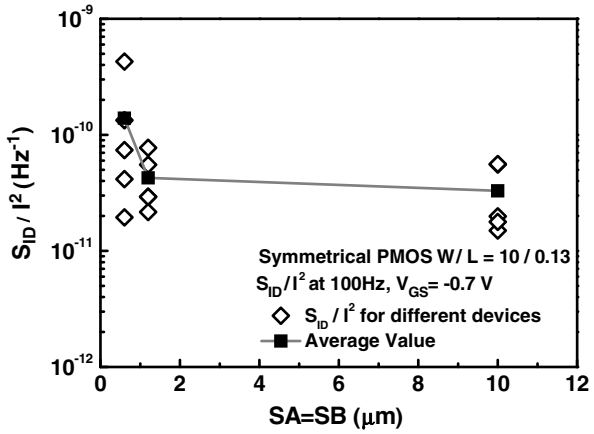

Fig. 10. The normalized noise current spectral density S_{ID}/I^2 at f = 100 Hz for PMOS as a function of the STI-to-gate distance $SA(SB)$. The devices were biased in the saturation region under a fixed V_{DS} of −0.7 V and V_{GS} = −0.7 V. The different points are for different devices with the same W/L = 10/0.13 (N_{finger} = 1).

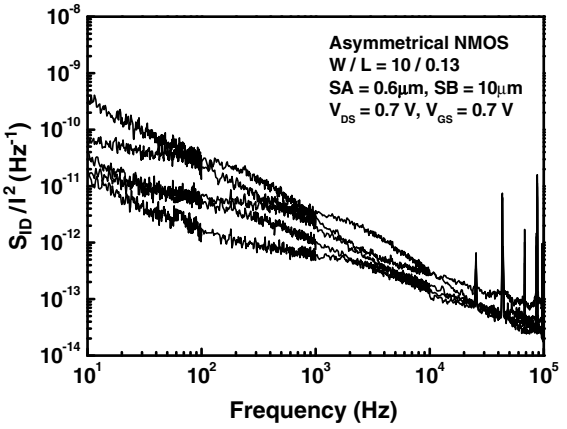

Fig. 11. Normalized noise current spectral density S_{ID}/I^2 for asymmetrical 0.13 μm NMOS with SA = 0.6 μm (source side), SB = 10 μm (drain side) under a V_{DS} of 0.7 V and V_{GS} = 0.7 V. The different traces are for different devices with the same W/L = 10/0.13 (N_{finger} = 1).

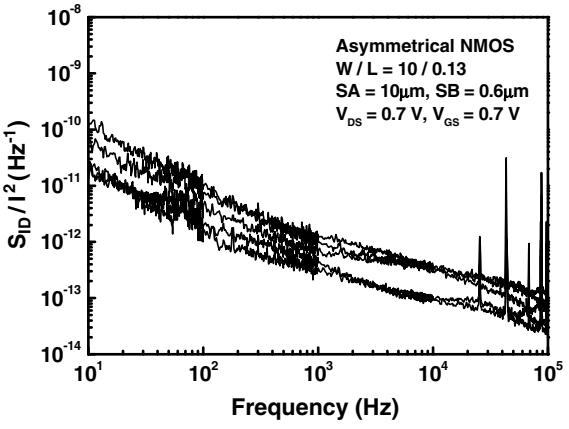

Fig. 12. Normalized noise current spectral density S_{ID}/I^2 for asymmetrical 0.13 μm NMOS with SA = 10 μm (source side), SB = 0.6 μm (drain side) under a V_{DS} of 0.7 V and V_{GS} = 0.7 V. The different traces are for different devices with the same W/L = 10/0.13 (N_{finger} = 1).

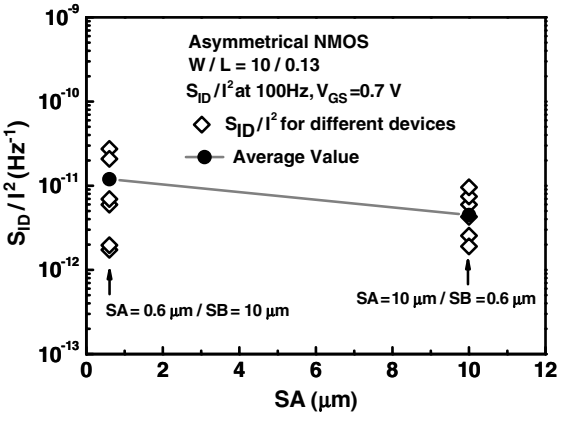

Fig. 13. Normalized noise current spectral density S_{ID}/I^2 at f = 100 Hz for NMOS as a function of the STI-to-gate distances for asymmetrical devices under a V_{DS} of 0.7 V and V_{GS} = 0.7 V. The different traces are for different devices with the same W/L = 10/0.13 (N_{finger} = 1).

in the drain region. This can be further identified by comparing the results for devices with SA = SB = 10 μm as shown in Fig. 9, which shows that the difference in these two cases (SA = 10 μm/SB = 0.6 μm and SA = SB = 10 μm) is not significant. The observed trend can be explained as follows. Between the drain and the pinch-off point in the channel, the carriers travel with the saturation velocity and also the vertical electric field is relatively small. Therefore, the trapping–detrapping process is not as pronounced and the traps around the drain side are not as critical as those located in the source side. A similar explanation has been given, while there were no corresponding experiments to verify this point [18,22]. In this study, the experimental data from the asymmetrical layouts provide a direct proof on this point.

3.2.3. Statistic model for the Flicker noise variation

To quantitatively study the noise level variation in different SA/SB spaces, the following formulas are employed to analyze the measured data. The relative standard deviation σ_{dB} can be calculated by [23–25]

Table 2
Noise variation S_+ as a function of the STI-to-gate distances

	NMOS			PMOS		
$SA(SB)$ (μm)	0.6	1.2	10	0.6	1.2	10
σ_{dB} (dB)	5.95	1.79	1.83	3.93	2.24	2.17
S_+	14.49	1.3	1.39	5.1	2.02	1.75

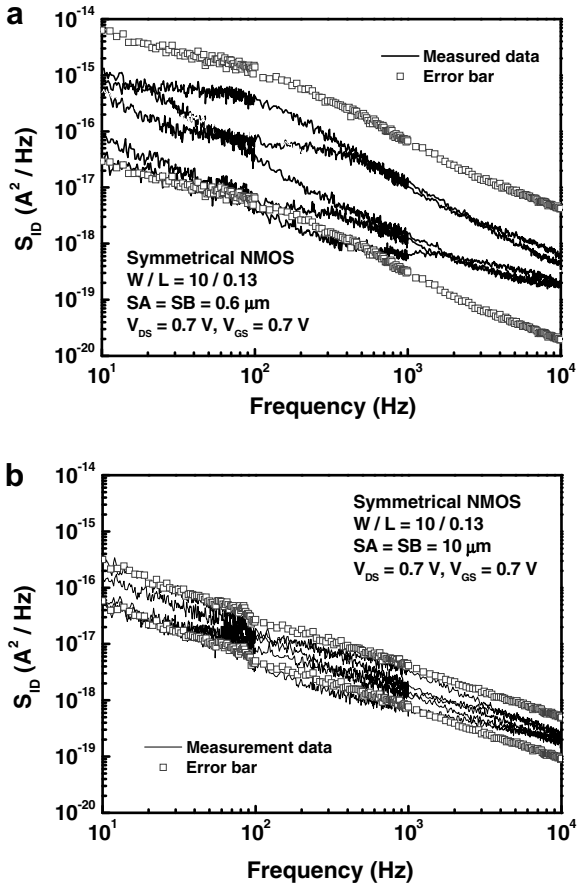

Fig. 14. The noise current spectral densities (solid line) and the error bars (dotted line) for 0.13 μm NMOS with (a) $SA(SB)$ = 0.6 μm, and (b) $SA(SB)$ = 10 μm, using k = 2. The different traces are for different devices with the same W/L = 10/0.13 (N_{finger} = 1).

$$\sigma_{\mathrm{dB}} = \sqrt{\frac{1}{N-1}\sum_{j=1}^{N}\left(S_{\mathrm{ID},j}\Big|_{\mathrm{dB}} - \langle S_{\mathrm{ID}}\rangle\Big|_{\mathrm{dB}}\right)^2} \quad (3)$$

where the $S_{\mathrm{ID},j}|_{\mathrm{dB}} = 10 \times \log(S_{\mathrm{ID},j})$, $S_{\mathrm{ID}j}$ is the jth spectrum and $\langle S_{\mathrm{ID}}\rangle$ is the average noise. The standard deviation is an index of the noise diversion at each frequency point (from 10 Hz to 10 KHz, total 1081 frequency points in this case). For NMOS devices with $SA(SB) = 0.6\ \mu\mathrm{m}$, $1.2\ \mu\mathrm{m}$, and $10\ \mu\mathrm{m}$, the calculated σ_{dB} were 5.95 dB, 1.79 dB, and 1.83 dB, respectively. For PMOS devices with $SA(SB) = 0.6\ \mu\mathrm{m}$, $1.2\ \mu\mathrm{m}$, and $10\ \mu\mathrm{m}$, the calculated σ_{dB} were 3.93 dB, 2.24 dB, and 2.17 dB, respectively. For a simplified analysis, the relative noise level and noise model can be described as follows

$$S_{\mathrm{ID}} = \frac{K_F I_D^{AF}}{f} \times (1 + S_{\pm}) \quad (4)$$

where S_+ and S_- are the relative noise variation above and below the average noise $\langle S_{\mathrm{ID}}\rangle$, and the noise variation can be expressed as [24]

$$S_{\pm} = 10^{\pm k\sigma_{\mathrm{dB}}/10} - 1 \quad (5)$$

where the parameter k is the selected confidence probability. In this work, the relative variation S_+ for different biases were calculated by using $k = 2$. The noise variation S_+ is calculated with different $SA(SB)$ values for NMOS and PMOS as summarized in Table 2. As can be seen, a significant improvement of S_+ can be observed as $SA(SB)$ increased from $0.6\ \mu\mathrm{m}$ to $1.2\ \mu\mathrm{m}$. Fig. 14 shows both the measured results (solid lines) and the error bars (dotted line) for the three types of symmetrical NMOS devices under a V_{GS} of 0.7 V. As the technology keep scaling down, an increased discrepancy due to the impact of STI effect can be expected in both DC and flicker noise characteristics.

4. Conclusion

The geometry effect on DC and flicker noise characteristics have been studied for 0.13 μm CMOS transistors using both symmetrical and asymmetrical layouts with different $SA(SB)$ distances. A more pronounced G–R noise and higher noise level were observed with decreased SA/SB distances, which can be attributed to the STI induced traps and described by the carrier number fluctuation model. The results from the asymmetrical devices proved that the traps around the source side have a more significant impact on flicker noise characteristics compared with those in the drain side. In addition, this study provides a simple approach to improve the device flicker noise. By properly extending the STI-to-gate distance in the source side ($SA > 1.2\ \mu\mathrm{m}$), the noise level and their variation can be reduced, which can be very useful to design noise sensitive circuits and blocks such as oscillators and mixers. Finally, the noise level variation model provided quantitative analysis of these devices, and can be employed in SPICE model for circuit design applications.

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