An Ultra-Low-Power Transformer-Feedback 60 GHz Low-Noise Amplifier in 90 nm CMOS

Po-Yu Chang, Sy-Haur Su, Shawn S. H. Hsu, *Member, IEEE*, Wei-Han Cho, and Jun-De Jin

***Abstract*—An ultra-low-power 60 GHz low-noise amplifier (LNA) with a 12.5 dB peak gain and a 5.4 dB minimum NF is demonstrated in a 90 nm CMOS technology. The LNA is composed of four cascaded common-source stages with the gate-source transformer feedback applied to the input stage for simultaneous noise and input matching. Also, the drain-source transformer feedback is used in the following stages for gain enhancement and interstage/output matching. This LNA consumes only 4.4 mW from a 1 V supply with a compact core area of 0.047 mm^2.**

***Index Terms*—CMOS, low-noise amplifier (LNA), mm-wave, transformer-feedback.**

I. Introduction

FOR short-range and high data rate wireless transmission demands, mm-wave communication has been attracting tremendous interest recently. The frequency range drawing most attention is the unlicensed 60 GHz band that offers several GHz bandwidth for multi-Gb/s data transmission. Owing to the rapid progress in technology, CMOS has become the most promising technology to realize a fully-integrated 60 GHz transceiver. In the receiver end of a 60 GHz system, the low-noise amplifier (LNA) that must provide high enough gain and low enough noise figure (NF) with low DC power is crucial to the overall system performance. The CMOS LNAs designed for 60 GHz operations have been published [1]–[7]. Many of the previous reported LNAs are based on the conventional transmission-line matching networks, which occupy a relatively large chip area even at 60 GHz. In contrast, the design approach with lumped spiral inductors is more area-efficient.

This letter demonstrates a transformer-feedback 60 GHz LNA with ultra-low-power consumption in a compact area by 90 nm CMOS. The transformer feedback technique has been widely used for the LNA design in different applications, but mostly at relatively low frequencies [8]–[10]. Compared with the design using spiral inductors, making good use of this technique can not only enhance the circuit performance due to the feedback of the transformers but also entwine inductors to further reduce the chip area. In this design, both the gate-source and the drain-source transformer-feedback techniques are employed in a four-stage common-source topology to achieve an ultra-low-power and compact LNA with excellent gain and noise characteristics.

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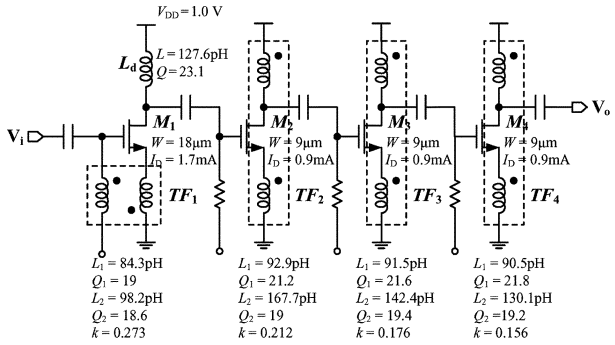

Fig. 1. Circuit schematic of the proposed ultra-low-power 60 GHz LNA with transformer-feedback techniques (TF_1: L_1 is gate inductor and L_2 is source inductor; TF_2, TF_3, and TF_4: L_1 is source inductor and L_2 is drain inductor).

II. Circuit Topology and Analysis

Fig. 1 shows the circuit schematic of the proposed transformer-feedback LNA, which is composed of four cascaded common-source stages with two different transformer-feedback configurations. The gate-source transformer-feedback at the input stage is used for simultaneous noise and input impedance matching, and the following stages are designed using the drain-source transformer-feedback technique to achieve interstage and output matching with improved power gain.

A. Transformer-Feedback Techniques

For the LNA designed in a cascade topology, the first stage dominates the overall noise characteristic of the amplifier. Fig. 2(a) shows the gate-source transformer feedback input stage, and Fig. 3 is the corresponding small-signal and noise model (the induced gate noise is neglected). Using the transformer with the design parameters of self-inductances (L_1 and L_2), the mutual inductance (M), and the coupling coefficient (k), the input stage can achieve a simultaneous impedance and noise matching for high-gain and low-noise characteristics [8], [9]. The following equations, derived based on the small-signal model with the assumption of an ideal transformer (i.e., $L_1L_2 = M^2$, $k = M/\sqrt{-L_1L_2} = 1$), provide a guidance for the transformer design on achieving input impedance matching to the source resistance R_s ($R\mathrm{S} = 50\ \mathrm{ohm}$ in this case)

$$Z_\mathrm{in} = \frac{j\omega L_1}{1-\omega^2 C_\mathrm{gs}(L_1+L_2+2M)+j\omega g_\mathrm{m}(L_2+M)}. \quad (1)$$

From (1), the input matching criteria could be derived as

$$\mathrm{Re}[Z_\mathrm{in}] = \frac{1}{g_\mathrm{m}}\frac{L_1}{L_2+M} = \frac{n^2}{(1+n)g_\mathrm{m}} = R_\mathrm{s} \quad (2)$$

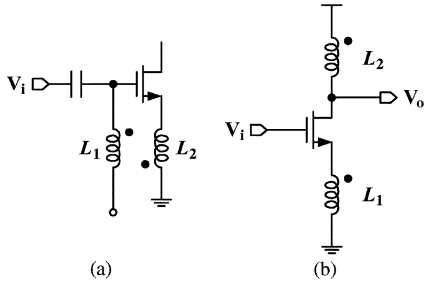

Fig. 2. Topologies of (a) gate-source transformer-feedback technique and (b) drain-source transformer-feedback technique.

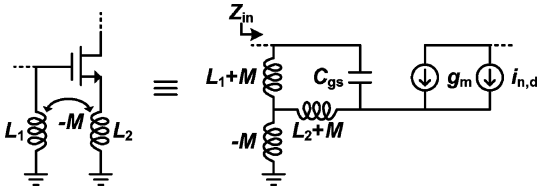

Fig. 3. Small-signal and noise model of a common-source stage with gate-source transformer-feedback. The transformer can be replaced by three inductors to simplify the analysis.

and

$$\mathrm{Im}[Z_{\mathrm{in}}] = 0 \Rightarrow L_1 = \frac{1}{C_{gs}} \left(\frac{n}{\omega(n+1)} \right)^2 \tag{3}$$

where

$$n = \sqrt{L_1/L_2}. \tag{4}$$

Besides, the associated noise factor F can be expressed as

$$F = 1 + \frac{R_{\mathrm{s}}\gamma}{g_{\mathrm{m}}} \left\{ \frac{1 - \omega^2 C_{gs}(L_1 + L_2 + 2M) + j\omega L_1/R_{\mathrm{s}}}{j\omega(L_1 + M)} \right\}^2 \tag{5}$$

where γ is the channel noise parameter [11]. Under input-matching condition [that satisfies both (2) and (3)], the noise factor can be simplified as

$$F = 1 + \frac{\gamma}{1+n}. \tag{6}$$

Equation (6) indicates that F can be lowered by increasing n, and noise matching is wideband as F is independent of frequency (γ is a constant). Note that g_{m} is also a critical design parameter for input matching as can be seen from (1). A large g_{m} is required for input matching if a large n is used, but which could result in increased power consumption P_{DC} or transistor size. In practical design, tradeoffs exist among g_{m}, P_{DC}, and parasitic capacitances of the input transistor. Also, the coupling coefficient k and the quality factor Q of the transformer should be considered. Choosing n around unity and $g_{\mathrm{m}} \sim 10\,\mathrm{mA/V}$ is a good tradeoff for achieving low-noise and low-power design.

The drain-source transformer-feedback topology is shown in Fig. 2(b), which is adopted in the second to the fourth stages. A guidance equation can be derived as (modified from [10])

$$nk \approx \frac{C_{gd}}{C_{gs}} \tag{7}$$

where C_{gd} is the gate-drain capacitance of the MOS transistor. If (7) is satisfied, C_{gd} can be neutralized by the reactive negative feedback and the Miller effect is reduced leading to an enhanced high-frequency gain. In practical design, because $C_{\mathrm{gd}}/C_{\mathrm{gs}}$ can be estimated from the transistor model and k is in a relatively small range ($\sim$ 0.15–0.21, see Fig. 1), n of the transformer can be determined for improved high-frequency gain.

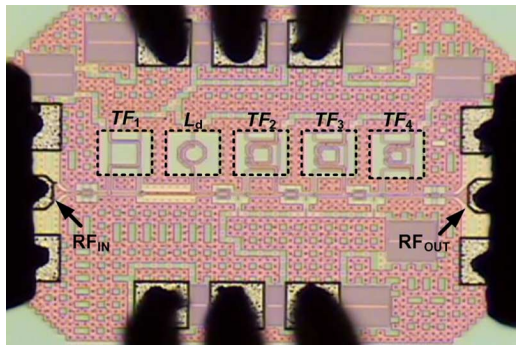

Fig. 4. Chip micrograph of the proposed LNA.

B. Circuit Design

The proposed ultra-low-power 60 GHz LNA is realized in a 1P9M 90 nm CMOS technology. The transistor M_1 of the first stage is designed to obtain a large enough transconductance ($\sim$ 11.7 mA/V in this case). In addition to the gate-source transformer, a drain inductor L_{d} is used in the first stage for gain peaking and interstage matching. For lowering the power consumption and parasitic capacitances, the transistors of the following stages (M_2, M_3, and M_4) are chosen with a smaller size and bias current. The details of transistor sizes and bias conditions of each stage are shown in Fig. 1.

The inductor and the transformers in the circuit are all designed by Metal 9 (thickness of 3.4 μm) and Metal 8 (thickness of 0.85 μm), and simulated rigorously by the EM simulation tool SONNET. The overall circuit is designed by Agilent ADS including the EM simulated passive components. The inductances and the coupling factors are designed according to the tradeoffs among the impedance and noise matching, gain, and bandwidth. The gate-source transformer TF_1 is designed using vertical coupling between Metal 9 and Metal 8, which is more effective than lateral coupling design. A similar structure is also used for TF_2, TF_3, and TF_4. The simulated parameters of the passive devices at 60 GHz are listed in Fig. 1. Note that the grounded-coplanar waveguide (GCPW) configuration is used for all the signal paths to minimize the signal loss and interference from the substrate [12].

III. Measured Results

Fig. 4 shows the chip micrograph of the proposed 60 GHz LNA. The chip size is $0.71 \times 0.51\ \mathrm{mm}^2$ including the probing pads, and the core circuit area is only 0.047 (0.43×0.11) mm^2. Under a 1 V supply voltage and 4.4-mA total current, the measured and the simulated input return loss $|S_{11}|$ and gain $|S_{21}|$ are shown in Fig. 5. A good input matching with return loss better than 10 dB is maintained within the interested frequency range. The measured $|S_{21}|$ has a 12.5 dB peak value at 57.3 GHz and $\sim$ 6 GHz (55.2 $\sim$ 61.2 GHz) of 3 dB bandwidth. The discrepancy between the measured and the simulated results can be attributed to the uncertainty of foundry-provided device RF models (only verified up to 30 GHz). Also, the parasitics between the transistors and the proximate interconnects, and the coupling effects between the passive components and the interconnect traces with a longer distance are not considered in our simulation. Fig. 6 shows the simulated and the measured NF

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR PUBLICATIONS

	[1]	[2]	[3]	[4]	[5]	[6]	This Work
Technology	90-nm CMOS	90-nm CMOS	90-nm CMOS	90-nm CMOS	0.13-μm CMOS	0.13-μm CMOS	90-nm CMOS
Peak Freq. / BW_{3dB} (GHz)	62 / -	58 / -	58 / 5.3	64 / 8.0	58 / 7.0	53 / 4.5	57.3 / 6.0
Supply (V)	1.2	1.5	1.3	1.65	2.4	1.5	1
Power (mW)	10.5	24	3.9	86	65	15.1	4.4
Chip Area (mm^2)	0.48	0.14	0.14/0.04[c]	0.52	0.72	1.06	0.36/0.047[c]
Max. Gain (dB)	12.2	14.6	15	15.5	20.4	21	12.5
P_{1dB} (dBm)	-8.2	-15.1	-18	-11.7	-20	-25	-16
IIP3 (dBm)	-	-6.8	-	-	-12	-16	-7
NF (dB)	6 [b]	< 5.5 [b]	4.4	6.5	8.6	7.19-9.5 [a]	5.4-6.5 [a]
FOM_1 [6] / FOM_2 [13]	-	-	5.99 / 38.7[d]	0.26 / 4.69[d]	0.29 / 0.98	1.01 / 2.62	3.87 / 18.7

[a] Results within 3 dB bandwidth; [b] Only simulated/estimated result; [c] Core area; [d] Estimated by $\mathrm{IIP3} = \mathrm{P1\,dB} + 9.6$.

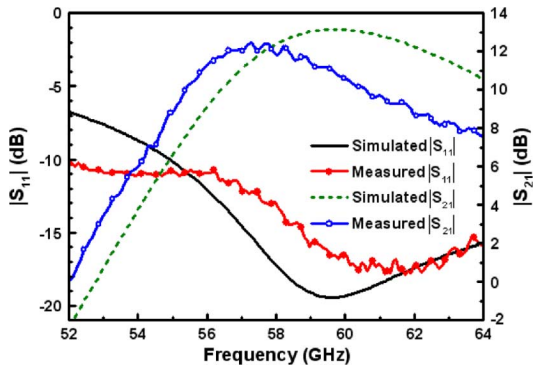

Fig. 5. Simulated and Measured $|S_{11}|$ and $|S_{21}|$.

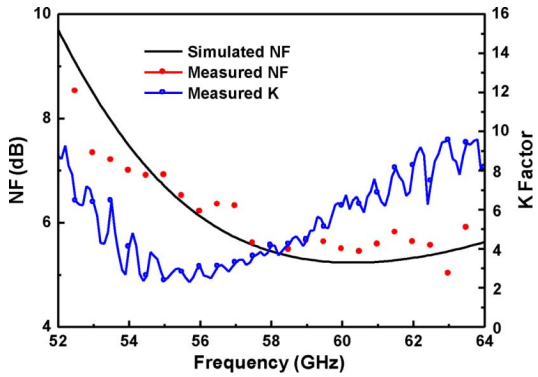

Fig. 6. Simulated and measured noise figure, and the K factor based on measured S-parameters.

with a measured minimum value of 5.4 dB at 60.5 GHz and a maximum value of 6.5 dB at 55.5 GHz within the 3 dB bandwidth. The stability factor K, based on the measured S-parameters, is also included in Fig. 6. The K factor, which is larger than one in a wide frequency, indicates the amplifier's stability. It should be mentioned that the coupling coefficient of each transformer is simulated rigorously by the EM tool to ensure the stability of each stage and the overall circuit. Table I summarizes the performance of the proposed 60 GHz LNA. The comparison with the prior publications based on CMOS technology is also listed with two figure-of-merits (FOMs) [6], [13]. The work published by E. Cohen *et al.* [3] shows superior FOMs mainly due to the relatively low power consumption and low noise figure. At the lowest supply voltage, the proposed LNA presents an excellent NF, comparable gain, while under a very low power consumption within a compact chip area.

IV. CONCLUSION

A compact ultra-low-power 60 GHz low-noise amplifier with a power consumption of 4.4 mW and a core area of 0.047 mm^2 was demonstrated in 90 nm CMOS. Based on the four-stage cascaded common-source topology, the gate-source transformer-feedback technique was employed for the input stage to obtain simultaneous input impedance and noise matching. The following stages were designed with the drain-source transformer-feedback technique for enhanced gain and also interstage/output matching. The amplifier achieved a maximum gain of 12.5 dB with a 6 GHz bandwidth, and a minimum NF of only 5.4 dB.

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