# An Ultra-Low-Power 24 GHz Low-Noise Amplifier Using 0.13 $\mu$m CMOS Technology

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***Abstract*—This study presents an ultra-low-power 24 GHz low-noise amplifier (LNA) using 0.13 $\mu$m CMOS technology. We propose of using the minimum noise measure ($M_{\rm MIN}$) as the guideline to determine the optimal bias and geometry of the transistors in the circuit. The power-constrained simultaneous noise and input matching (PCSNIM) technique is also employed for this design. With the proposed design approach, the LNA achieves a peak gain of 9.2 dB and a minimum *NF* of 3.7 dB under a supply voltage of 1 V. The associated power consumption is only 2.78 mW.**

***Index Terms*—CMOS, k-band, low-noise amplifier (LNA), low power.**

## I. Introduction

CONTINUOUS scaling of CMOS technology keeps driving the innovation of RFICs with higher integration level and lower cost. Significant efforts on the study of both devices and circuits also substantiate the wireless communication systems operating toward higher frequencies. Using the K-band (18 – 26.5 GHz) for short-range and high data-rate wireless communication and anti-collision radars is recently of great interest to both industry and academia [1]–[6]. Similar with other portable wireless applications, low-power design is a critical issue [6]. In this letter, we present an ultra-low-power 24 GHz low-noise amplifier (LNA) in 0.13 $\mu$m CMOS technology. A peak gain of 9.2 dB and a minimum noise figure of 3.7 dB are achieved with a DC power consumption of 2.78 mW only.

## II. Circuit Topology and Analysis

Design of RF LNAs consists of two major parts, namely selection of transistor geometry and bias point, and also determination of circuit topology including the matching networks. The characteristics of transistors play a critical role, since the core circuit is composed of only a few transistors in most cases. In addition, a simple circuit topology is often preferred to prevent the unpredicted parasitic effects from the complicated layout.

Fig. 1 shows the circuit schematic and the chip micrograph of the proposed LNA. The grounded coplanar waveguide (GCPW) is adopted for interconnects to alleviate the signal attenuation and substrate coupling effect [7]. In this design, two common-source (CS) stages connected in cascade are employed. As shown in Fig. 1(a), there are only two transistors in the proposed LNA, and thus determination of transistor geometry and bias is of extreme importance for achieving low-noise and low-power simultaneously.

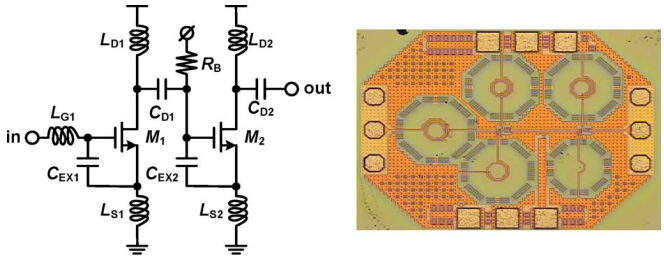


Fig. 1. (a) Circuit schematic and (b) chip microphotograph ($0.76 \times 0.59\ \mathrm{mm}^2$ with core area of $0.59 \times 0.46\ \mathrm{mm}^2$) of the proposed ultra-low-power LNA.

### A. Determination of Transistor Bias and Geometry

Differing from the previous study mainly using the noise figure *NF* to select the transistor size in LNA design [8], the noise measure $M$ is adopted here. $M$ is a calculation for cascaded noisy gain stages to determine which one should be used first for achieving the lowest noise figure [9]. Calculation of $M$ includes the information of both *NF* and gain, the two major concerns in LNA design. Instead of obtaining $M$ by *NF* and power gain ($S_{21}$) under 50 $\Omega$ terminations, we propose of using the minimum noise figure $NF_{\rm MIN}$ and maximum stable gain $G_{\rm MAX}$ to calculate noise measure (denoted as $M_{\rm MIN}$)

$$M_{\rm MIN} = \frac{10^{NF_{\rm MIN}[\rm dB]/10} - 1}{1 - 10^{-G_{\rm MAX}[\rm dB]/10}}. \tag{1}$$

Compared with using *NF* and $S_{21}$, $NF_{\rm MIN}$ and $G_{\rm MAX}$ indicate the best possible performance can be achieved after matching, and hence $M_{\rm MIN}$ provides a pertinent guideline on the transistor bias and geometry determination. Fig. 2 plots $M_{\rm MIN}$ and current density $J_{\rm CH}$ as a function of the gate bias ($V_{\rm DD} = 1$ V) for 0.13 $\mu$m NMOS based on the foundry provided transistor model (BSIM3v3) with three typical channel widths of 10, 20, and 30 $\mu$m. The excellent scalability of MOS transistors results in three almost identical curves of $J_{\rm CH}$. In addition, the optimal $M_{\rm MIN}$ always occurs, independent of the channel width, in a small range of $J_{\rm CH}$. The corresponding $V_{\rm GS}$ is at around 0.55–0.65 V. By also considering power consumption and gain, the finally selected gate bias is 0.6 V, mapping to $J_{\rm CH}$ of about 0.1 mA/$\mu$m. Compared with $M_{\rm MIN}$, the noise measure $M$ is not helpful in this case since matching of the

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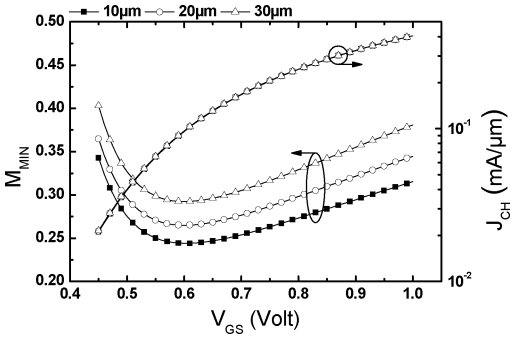


Fig. 2. $M_{\rm MIN}$ and $J_{\rm CH}$ versus gate bias, $V_{\rm GS}$, for transistors of $\rm W/L$ = 2 $\mu$m/0.13 $\mu$m with 5, 10, 15 fingers, respectively, at 24 GHz.

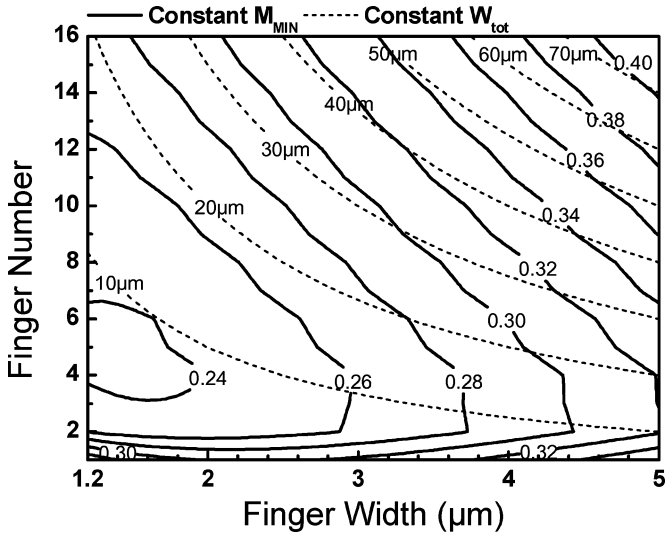


Fig. 3. Contour plot of $M_{\rm MIN}$ and the total finger width for 0.13 $\mu$m NMOS under $V_{\rm GS}$ = 0.6 V and $V_{\rm DD}$ = 1 V at 24 GHz.

transistor is not considered. Without matching, the transistor has an intrinsic gain $S_{21}$ less than 0 dB at 24 GHz and negative $M$.

Fig. 3 shows the contour plot of $M_{\rm MIN}$ and total width $W_{\rm tot}$ under a fixed $V_{\rm GS}$ of 0.6 V ($V_{\rm DD}$ = 1 V) using the finger width and number as the variables for the x-axis and y-axis, respectively. Considering these two parameters separately allows minimizing the undesired parasitics of the gate resistance and capacitance. Compared with the previous study [8] using $W_{\rm tot}$ (x-axis) and the drain current $I_{\rm D}$ (y-axis) as the variables, the proposed approach provides more information about parasitics for high frequency design optimization.

In general, as shown in Fig. 3, $M_{\rm MIN}$ reduces with $W_{\rm tot}$ and the trend is consistent with that observed in Fig. 2. The contour plot indicates that the optimal $M_{\rm MIN}$ ($< 0.24$) occurs when the finger number is about 3 to 7 and with the finger width around 1.2 to 2 $\mu$m. Note the width of 1.2 $\mu$m is the smallest allowed finger width, limited by the technology. The transistor size finally employed in our design is 1.2 $\mu$m$\times$ 0.13 $\mu$m with 10 fingers, which is the optimal geometry that still remains unconditionally stable (verified by the stability factor $K$) and a good power gain of the circuit after matching. If a transistor smaller than this size is used, the input/output impedances become very close to edge of the Smith chart and high Q matching networks are required, which makes the circuit unstable. Since the power consumption is proportional to $W_{\rm tot}$, this is also the smallest size and therefore, the lowest power consumption can be achieved under the criteria of unconditional stability.

### *B. Circuit Topology and Matching Network*

As shown in Fig. 1, the input matching network includes inductors $L_{\rm G1}$ and $L_{\rm S1}$, and capacitor $C_{\rm EX1}$. The extra gate-source capacitance is critical for achieving power-constrained simultaneous noise and input matching (PCSNIM) with both $Z_{\rm in}$ and $Z_{\rm opt}$ at 50 $\Omega$, where $Z_{\rm opt}$ is the source impedance for optimal noise matching. The $Z_{\rm in}$ and $Z_{\rm opt}$ of a CS stage matching by inductor degeneration can be simplified as (modified from [10])

$$Z_{\rm in} = \frac{g_{\rm m}L_{\rm s}}{C_{\rm gs}} + j\left[\omega L_{\rm s} - \frac{1}{\omega C_{\rm gs}}\right] \tag{2}$$

$$Z_{\rm opt} = \frac{\alpha'}{\omega C_{\rm gs}} - j\left[\omega L_{\rm s} - \frac{1-\beta'}{\omega C_{\rm gs}}\right] \tag{3}$$

where $\alpha'$ and $\beta'$ are both technology dependent constants. Note $\beta'$ becomes much smaller than one in advanced technology resulting in a similar imaginary part of $Z_{\rm in}$ and $Z_{\rm opt}$. The real part of $Z_{\rm opt}$ could be optimized approaching 50 $\Omega$ through $C_{\rm gs}$. Estimated by the equations, a large $C_{\rm gs}$ of 42.8 fF ($\sim$ 50 fF from simulation), i.e., a transistor with a larger channel width is required (the intrinsic $C_{\rm gs}$ of the 1.2 $\mu$m$\times$ 0.13 $\mu$m$\times$ 10 device is only $\sim$ 14 fF) making it difficult for low-power design. An external capacitance is used to increase the effective gate-source capacitance while maintaining a small transistor size. Since the transistor bias and geometry are selected, the $g_{\rm m}$ of the transistor is fixed. A gate inductor $L_{\rm g}$, as shown in Fig. 1, is essential to eliminate the imaginary part of both $Z_{\rm opt}$ and $Z_{\rm in}$ for achieving the PCSNIM condition.

The drain inductor $L_{\rm D1}$ functions as the load for the first stage and also serves as the inter-stage matching network together with $L_{\rm S2}$, $C_{\rm D1}$, and $C_{\rm EX2}$. The inductor $L_{\rm D2}$ and capacitor $C_{\rm D2}$ implement the $L$-section matching to a 50 $\Omega$ load for the output stage. With the determined transistor bias and geometry for both $M_1$ and $M_2$, $C_{\rm EX1}$ of 20 fF is employed, and then $L_{\rm G1}$ of 0.8 nH and $L_{\rm S1}$ of 0.5 nH turn both $Z_{\rm in}$ and $Z_{\rm opt}$ into 50 $\Omega$. The inter-stage matching network consists of 0.6 nH $L_{\rm D1}$, 150 fF $C_{\rm D1}$, 20 fF $C_{\rm EX2}$ and 0.3 nH $L_{\rm S2}$. Finally, $L_{\rm D2}$ of 0.7 nH and $C_{\rm D2}$ of 47 fF complete the output matching network. Note the smaller $C_{\rm EX}$ than expected is due to the Miller effect, which adds $\sim$ 15 fF to have a total equivalent $C_{\rm gs}$ of $\sim$ 50 fF.

## III. Measured Results

Fig. 4 shows the measured results together with the simulation. The well agreed $NF_{\rm MIN}$ and *NF* from simulation at around 24 GHz with excellent $S_{11}$ (see Fig. 5) indicate that the PCSNIM condition is obtained. Under a supply voltage of 1 V and bias current of 2.78 mA, a peak gain of 9.2 dB and a minimum noise figure of 3.7 dB were achieved both at 23.6 GHz from measurements. Since the passive components are carefully simulated by the EM simulation tool, the discrepancy between simulated and measured results could be mainly attributed to the modeling of active devices, in which some parasitic effects may

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PUBLISHED WORKS

| Ref. | This work | [2] | [3] | [4] | [5] | [6] |
|---|---|---|---|---|---|---|
| Technology (CMOS) | 0.13 μm | 0.18 μm | 90 nm | 90 nm | 0.18 μm | 0.18 μm |
| Peak gain frequency (GHz) | 23.6 | 24 | 33 | 28.5 | 24 | 22 |
| Power gain (dB) | 9.2 | 13.1 | 18.6 | 20 | 12.8 | 10.1 |
| Bandwidth (GHz) | 22.2-25.9 | 22-26.5 | 31-34 | 27.5-30 | 22.3-26.5 | 19.9-24 |
| Noise figure (dB) | 3.7 | 3.9 | 3 | 2.9 | 3.3 | 4.3 |
| I/O return losses (dB) | 12/16 | 15/20 | 8/18 | 12/17 | 7.5/17 | 12/- |
| $P_{1dB}/IIP_3$ (dBm) | -13/-2.9 | -12.2/+0.54 | -16/- | -17/-7.5 | -/- | -10/-1 |
| $P_{DC}$ (mW) | 2.78 | 14 | 10 | 16.25 | 8 | 7.2 |
| Power supply (Volt) | 1 | 1 | 1.2 | 1 | 1 | 1.8 |
| FoM | 4.53 | 1.45 | 2.79 | 1.62 | 2.92 | 1.74 |

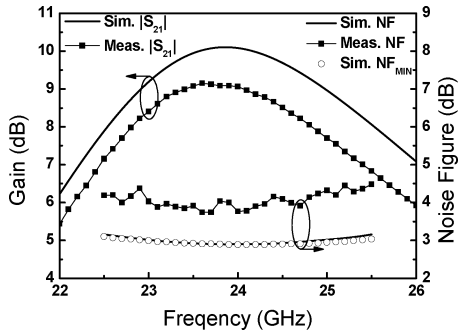


Fig. 4. Simulated and measured gain and noise figure.

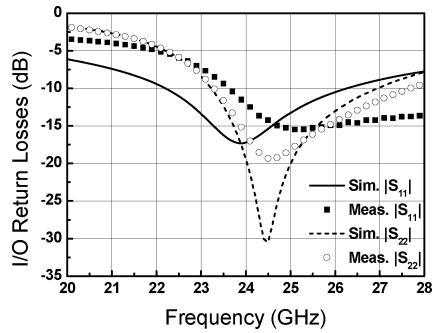


Fig. 5. Simulated and measured input/output return losses.

not be considered at high frequencies. In addition, the BSIM3v3 model does not consider the induced gate noise and use the noise model parameter $\gamma$ of only 2/3 (should be $> 1$ in advanced technology [10]), which result in underestimated circuit noise, as commonly seen in previous publications [2], [6]. The input and output return losses are 12 dB and 16 dB at 24 GHz respectively as shown in Fig. 5.

It should be mentioned that an external gate resistance $r_g$ is used in the model to fit the measured noise characteristics according to the technology notes provided by the foundry. In theory, the effect of the induced gate noise can be incorporated in $r_g$ for a better prediction of noise parameters [11]. Although the induced gate noise is not included in the model, $r_g$ somehow corrects the model for a more accurate $Z_{opt}$ leading to a good agreement between the simulated and measured results for PCSNIM. From the measurements, a good input matching ($|S_{11}| < -10$ dB) is obtained in the frequency range with lowest noise figures ($\sim 24$ GHz), which also suggests that the PCSNIM condition is valid. Performance summary and comparison with prior arts are shown in Table I. The figure of merit (FoM) adopted is defined in [3], [5]. With a low *NF* and a high gain under very low power consumption, the proposed LNA achieves an excellent FoM

$$\mathrm{FoM} = \frac{S_{21}[\mathrm{dB}] \cdot BW[\mathrm{GHz}]}{(NF[\mathrm{dB}] - 1) \cdot P_{\mathrm{DC}}[\mathrm{mW}]}. \tag{4}$$

## IV. CONCLUSION

An ultra-low-power 24 GHz LNA was demonstrated in 0.13 $\mu$m CMOS technology with a peak gain of 9.2 dB and a minimum *NF* of 3.7 dB consuming only 2.78 mW under 1 V power supply. With the proposed design approach using $M_{\mathrm{MIN}}$ and PCSNIM technique, the LNA presents FoM among the best compared with the published results.

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