W-Band Multiple-Ring Resonator by Standard 0.18-μm CMOS Technology

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***Abstract*—A high-Q multiple-ring resonator fabricated by standard 0.18-μm CMOS process is presented. This design achieves a high quality factor at W-band without the need of any post-processing steps. Simulation results indicate that the four open-loop rings enhance the quality factor by 120% compared with the resonator with a single ring. The measured quality factors are 38 and 83 at ~75 GHz under the loaded and unloaded conditions, respectively.**

***Index Terms*—CMOS, microstrip line, resonator, W-band.**

I. Introduction

W-BAND (75–110 GHz) integrated circuits (IC) are widely used for automobile anticollision and space applications [1], [2]. These circuits are mainly fabricated by compound semiconductor technology due to the availability of high-speed devices and the low-loss substrates. With the feature size scaling, the operation frequency of CMOS devices increase rapidly. As a result, CMOS technology becomes a promising candidate for W-band ICs. However, achieving high quality factor passive components is still a problem due to lossy Si substrates. To realize W-band circuits using standard CMOS process for high integration level and low cost, development of low loss and high quality factor passive components is a critical step.

One of the important passive components for microwave circuits is the ring resonator. Ring resonators perform frequency selection functions to achieve high performance oscillators and filters [3]–[7]. A spiral-shaped ring resonator by commercial p-HEMT process showed a quality factor of 6.59 at 60 GHz has been reported [3]. A microstrip square-ring resonator with a Q-factor of 64 at 14.4 GHz was reported in [4]. With MEM's technology, ring resonators on Si-substrates demonstrated high quality factors at microwave frequencies [6], [7]. However, high-Q ring resonators by standard CMOS process for W-band applications have never been reported.

In this study, a high-Q, multiple-ring resonator at W-band by standard 0.18-μm CMOS process is presented. This work attempts to design a high-Q ring resonator, which can be used for microwave oscillators similar with the works shown in [3], [5], and [7]. A resonator including four open-loop $\lambda/2$ resonant rings has been realized to achieve a high quality factor on lossy Si substrate. The bottom metal shielding in modern CMOS technology reduces the substrate loss. Novel multiple-ring design significantly enhances the resonator quality factor. Various multiple ring topologies are designed and the quality factors are calculated. The stress introduced by the oversized metal area and other design rules in CMOS process have been considered. The design optimization such as the spacing between the ring and the signal line, and the quality factor enhancement by different topologies are also studied.

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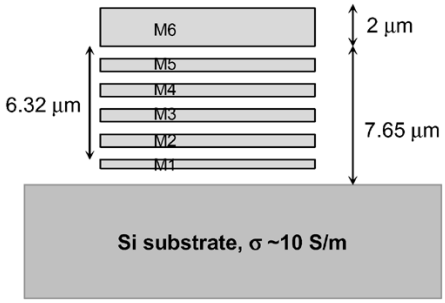

Fig. 1. Cross section of the metal layers in a standard 0.18-μm CMOS process.

II. Resonator Design

Fig. 1 shows the cross section of the metal interconnect layers in 0.18-μm CMOS process. Typical substrate conductivity is ~10 S/m, which can be very lossy at W-band. This technology provides six metal layers (M1-M6) for a flexible design possibility. The distance between each layer is ~ 0.8 μm, and the metal layer thickness is ~0.6 μm except for the top metal layer with a thickness of 2 μm. M1 was chosen as the bottom metal, and M6 was chosen as the top metal for a metal-insulator-metal (MIM) thin-film microstrip structure. Layers from M2 to M5 are not employed in this structure and SiO_2 is used as the dielectric material between M1 and M6. The bottom metal layer provides excellent isolation, and the thickened top metal layer can effectively reduce the conduction loss of the signal line. For a 50 Ω microstrip transmission line designed by this process, the signal line width is 11.6 μm. Simulation results show that the insertion loss is less than 1 dB at 75 GHz for a microstrip line longer than 1000 μm.

To find the optimized structure for high quality factor, various ring resonator structures were designed as shown in Fig. 2. A three-dimensional (3-D)-EM simulator, HFSS, was employed for the simulation. The basic building block uses the open-loop

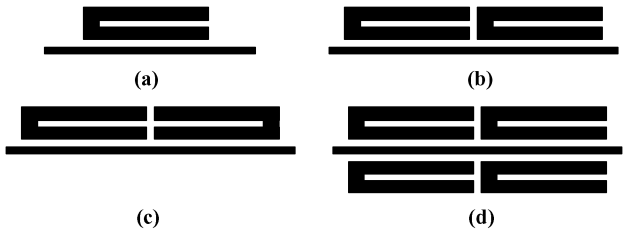

Fig. 2. Different designs of W-band resonators in a standard 0.18–μm CMOS process.

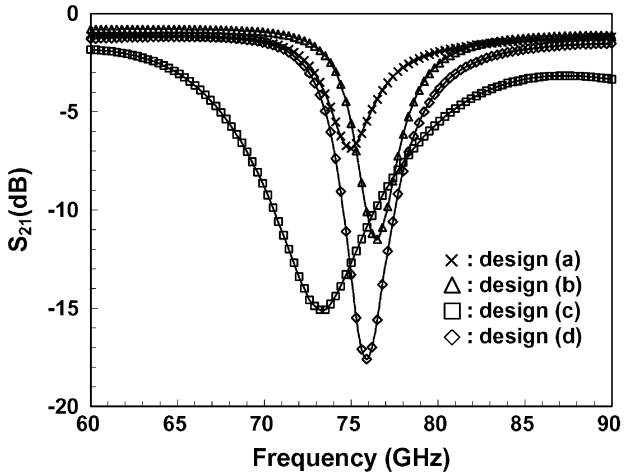

Fig. 3. Simulated transmission characteristics (S_{21}) of the four different ring resonators.

ring topology. The open-loop ring resonator is designed based on the following equations:

$$\lambda_{\text{eff}} = \frac{c}{(\sqrt{\varepsilon_{\text{eff}}}) \cdot f} \tag{1}$$

$$l_{\text{eff}} = \frac{n \cdot \lambda_{\text{eff}}}{2} \tag{2}$$

where f is the central resonant frequency, c is the speed of light in free space, ε_{eff} is the effective dielectric constant, λ_{eff} is the effective wavelength, n is the mode number, and l_{eff} is the effective length of the resonator.

Design (a) is a resonator structure with a single $\lambda/2$ ring and a 50-Ω transmission line. Except the length of the ring, the most critical design parameters are the coupling spacing and the line width of the ring. The spacing used in this design is 1.5-μm limited by the minimum top metal spacing of the technology, which is, however, sufficiently small to achieve good coupling. In addition, the optimized width of the ring was found to be in the range of four to six times of the width of the 50-Ω transmission line. The width adopted in the design is 57 μm.

To enhance the resonant effect for an improved quality factor, various multiple ring structures were designed. The simulated transmission characteristics corresponding to the structures in Fig. 2 are shown in Fig. 3. Design (b) and (c) use dual open-loop ring structures with the open end of the ring in the same and opposite directions, respectively. As can be seen, the design with two rings opened in the same direction results in a significantly improved Q-factor. Design (c) can be approximated as a single close-loop ring with a length of λ. Without the enhancement effect of the dual rings, the quality factor is not as good as design (b). Fig. 2(d) is the finally achieved optimized design structure with four resonant $\lambda/2$ rings. The various designs indicate that the Q-factor can be effectively increased by the multiple ring structures due to enhanced resonance at the desired frequency. The simulated results for the four resonant structures show the loaded quality factors, calculated by the ratio of the resonant frequency and the 3-dB bandwidth, are 20, 36, 19, and 44, respectively. The quality factor improved by 120% in design (d) by multiple rings compared to that in design (a) with a single ring resonator.

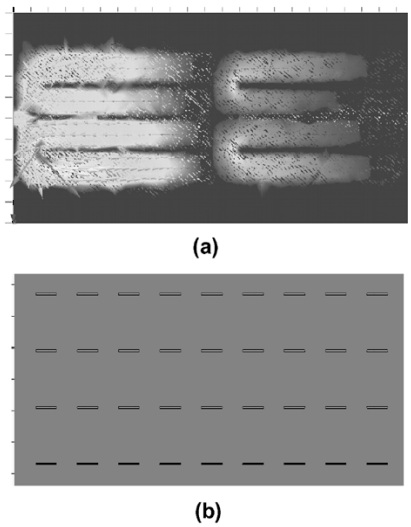

Fig. 4. (a) Simulated current distribution of the ground plane. (b) Locations of the slots on the ground plane.

III. Layout and Measurement Results

To implement the resonator in a standard CMOS process, the oversized metal areas need to be considered. According to the design rule, opening slots to release the stress caused by a large-area metal layer is essential. The suggested minimum size of the slot is 2×10 μm^2. The current density distribution of the resonators was simulated as an indication for the locations of the slots. Fig. 4(a) shows the current distribution on the ground plane. The simulation results indicate that the areas with maximum current densities are underneath the rings, therefore the slots are opened in the positions with relatively small current density, as shown in Fig. 4(b).

The photograph of the fabricated multiple-ring resonator is shown in Fig. 5 with microwave probing pads and ground planes (connected to M1 through via holes) for ground-signal-ground (G-S-G) testing configuration. The overall chip size is 1400 $\times$ 600 μm^2. S-parameter measurements were performed by Agilent 8757 scalar network analyzer. Fig. 6 compares the simulated and the measured results of the resonator from 60 to 90 GHz. The simulated results are in very good agreement with the measured results. The simulated results shown include the probing pads to be completely identical to the fabricated physical structure, and therefore differ from the intrinsic resonator performance as shown in Fig. 3.

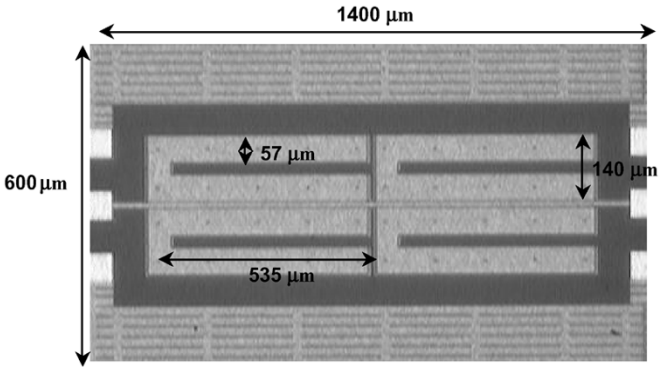

Fig. 5. Photograph of the W-band multiple-ring resonator fabricated by a standard 0.18-μm CMOS process.

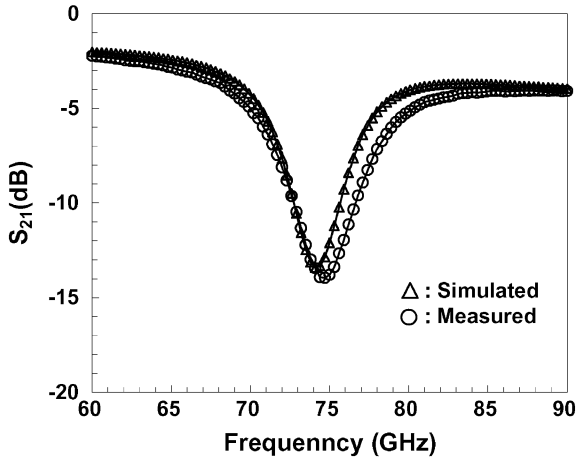

Fig. 6. Simulated and measured transmission characteristics (S_{21}) for the multiple-ring resonator from 60 to 90 GHz.

The calculated loaded Q-factor is 38 after the de-embedding procedure for the probing pads [8]. The unloaded quality factor (Q_u) can be calculated based on the loaded quality factor (Q_L) by the equations described in [9]. The calculated Q_u can achieve 83 after the de-embedding procedure, which is close to the simulated intrinsic resonator performance with Q_u of 104 in case (d) (Fig. 3).

IV. Conclusion

A multiple-ring resonator was designed and fabricated in a standard 0.18-μm CMOS process. A high quality factor was achieved with the multiple-ring topology. Using the bottom interconnect metal layer as the ground plane, the lossy Si substrate is isolated without the need of additional etching process. Based on the design rules, slots were carefully opened to release the stress of the large metal areas. At 75 GHz, the loaded and unloaded quality factors are 38 and 83, respectively. This study demonstrates the possibility of fully integrated high-Q multiple-ring resonator at W-band with a standard CMOS process, and potential applications with active devices for monolithic oscillators.

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