A 76.2–89.1 GHz Phase-Locked Loop With 15.6% Tuning Range in 90 nm CMOS for W-Band Applications

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***Abstract*—In this letter, a wide tuning range W-band phase-locked loop (PLL) in 90 nm CMOS is presented. A novel frequency tripling topology with a single cross-coupled pair and a dual tank is proposed for the voltage-controlled oscillator (VCO) to achieve wide tuning characteristics under low power consumption. The locking range of the PLL at the fundamental tone is 25.4–29.7 GHz, and an excellent tuning range at the third harmonic frequency up to 12.9 GHz (from 76.2 to 89.1 GHz, 15.6%) is obtained. Under a 1.2 V supply voltage ($\mathbf{P_{diss} = 62.4\ mW}$), the measured closed-loop phase noise of the PLL is −83.5 dBc/Hz at 78.34 GHz. To the best of our knowledge, the achieved turning range is the highest currently reported for the PLLs operating in a similar frequency range in CMOS technology.**

***Index Terms*—Phase-locked loop (PLL), tripler, voltage-controlled oscillator (VCO), W-band, wideband.**

I. Introduction

THE W-band (75–110 GHz) found many useful applications such as satellite communications, passive mm-wave cameras, and radar systems. Conventionally, the W-band circuit blocks are mainly realized by III-V or SiGe technologies to take advantage of the superior transistor characteristics [1], [2]. Recently, the rapid progress with impressive device frequency response in CMOS technology has enabled fully integrated solutions with low cost, low power, and high integration level for the emerging applications in W-band [3].

Phase-locked loops (PLLs) are essential in many communication and computing systems [4]. Also, a wide tuning range PLL could be very useful for various applications. However, the requirement of wideband voltage-controlled oscillator (VCO) and frequency divider makes it a real challenge to design a wide tuning range PLL at W-band in CMOS technology. The frequency multiplication technique has been proposed [5]–[7], which exhibits several advantages in the millimeter wave frequency range such as less sensitive to device model inaccuracy and loading effect to the output buffer. Also, the first stage divider can operate at lower frequencies for a PLL, alleviating design difficulties with reduced power consumption. In previously reported works, the injection locking frequency multiplier presented a good phase noise performance with a large output power [5]. In addition, a wideband harmonic current can be generated from the amplifier due to transistor nonlinearity [6], [7]. By using the LC filter, the desired harmonic frequency can be extracted.

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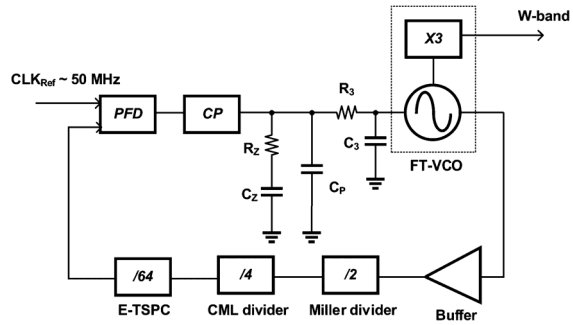


Fig. 1. Block diagram of the proposed wide tuning range W-band PLL.

In this letter, we propose a novel frequency tripling technique to achieve a high performance W-band PLL with a wide tuning range in a standard 90 nm CMOS technology. This letter is organized as follows. Section II presents the circuit architecture of the PLL with details of the frequency tripling technique. The experimental results and discussion are shown in Section III. Finally, Section IV concludes this letter.

II. Circuit Architecture and Analysis

Fig. 1 shows the block diagram of the proposed W-band PLL, which is realized using the integer-N architecture. The proposed frequency tripling (FT) technique is employed in the VCO design to achieve a wide tuning range under low power consumption. The total division number of the divider chain is 512, and the prescaler is designed using the Miller topology. The second frequency divider is realized using the current mode logic (CML), and the low-frequency divider chain is done by the extended True single-phase clock (E-TSPC). The phase frequency detector and charge pump can correct the phase and frequency error in the PLL according to a reference clock at approximately 50 MHz. A third-order loop filter is used to reduce the spurious introduced from the undesired parasitic effects such as bond wires, where C_3 and R_3 are implemented on chip, and other RC components are off chip to reduce the chip size. Also, all the RC components of the loop filter are placed close to the voltage control node to reduce the parasitic effects from the interconnects and bond wires. The loop bandwidth of the PLL is designed as 100 KHz, and the phase margin is about 70°.

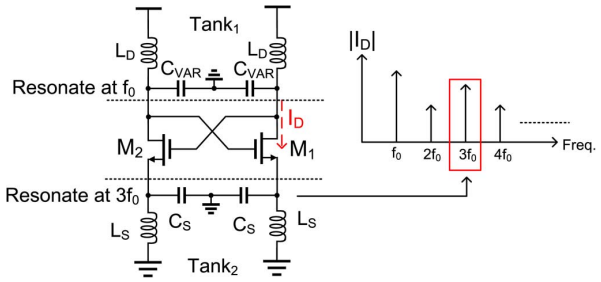
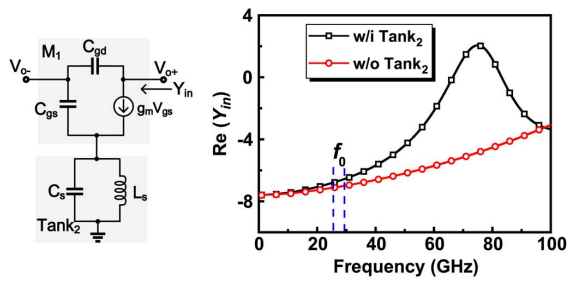


Fig. 2. Circuit schematic and operation principle of the proposed FT-VCO.



(a) (b)

Fig. 3. (a) Simplified half-circuit of the cross-coupled pair with $Tank_2$ to determine $Y_{\rm in}$. (b) Calculated $Y_{\rm in}$ with and without $Tank_2$.

Fig. 2 illustrates the circuit configuration and design principle of the proposed FT-VCO. The NMOS cross-coupled pair provides negative resistance resulting in oscillation, and the harmonic currents $I_{\rm D}$ can be generated when a large voltage swing appears at the gate because of device nonlinearity. In addition to an LC tank placed on top of the cross-coupled pair, a second tank is used at the bottom for frequency tripling. In the proposed topology, the fundamental oscillation at f_0 is supported by $Tank_1$, and $Tank_2$ resonates at approximately $3f_0$ to generate the third-harmonic output. Note that the output power at the fundamental frequency can be effectively suppressed using the proposed configuration, and the tuning range is tripled from that at f_0.

The design of $Tank_2$ plays a critical role for the VCO operation. Composed of $L_{\rm S}$ and $C_{\rm S}$, $Tank_2$ is connected to the source terminals of the cross-coupled pair acting like LC degeneration, which can affect the oscillation frequency of the fundamental tone and the initial condition of negative resistance. The simplified half-circuit in Fig. 3(a) can be used to determine the input admittance $Y_{\rm in}$ which shows how LC degeneration affects $Y_{\rm in}$ of the cross-coupled pair, where $g_{\rm m}$, $C_{\rm gs}$, and $C_{\rm gd}$ are the transconductance, gate-source, and gate-drain parasitic capacitances, respectively, of the MOSFETs. The real part of $Y_{\rm in}$ is

$$\mathrm{Re}\{Y_{IN}\} = \frac{-2g_m\left(1-\left(\frac{\omega}{\omega_1}\right)^2\right)}{\left(1-\left(\frac{\omega}{\omega_1}\right)^2-\left(\frac{\omega}{\omega_2}\right)^2\right)^2+(j\omega L_s g_m)^2} \cdot\left(1-\left(\frac{\omega}{\omega_1}\right)^2-\left(\frac{\omega}{\omega_2}\right)^2\right) \quad (1)$$

where

$$\omega_1=\frac{1}{2\pi\sqrt{L_sC_s}},\quad \omega_2=\frac{1}{2\pi\sqrt{L_sC_{gs}}}.$$

Fig. 3(b) shows the result of calculated $\mathrm{Re}\{Y_{\rm in}\}$ by using $L_{\rm s}=70$ pH, $C_{\rm s}=50$ fF, and $C_{\rm gs}=30$ fF (similar to the values used in the final design). With a proper design by setting the resonant frequency of L_s and C_s close to $3f_0$, $\mathrm{Re}\{Y_{\rm in}\}$ only becomes slightly less negative at the fundamental tone, which indicates the additional tank has a small impact on f_0 oscillation but can provide an excellent frequency selection nearly three times higher than f_0 for the desired W-band output. Note the start-up condition of the VCO is based on (1). When the absolute value of $\mathrm{Re}\{Y_{\rm IN}\}$ is larger than the equivalent admittance (loss) of $Tank_1$ at f_0, the oscillation condition can be satisfied. Fig. 4 shows detailed circuit topology of the proposed FT-VCO, including the output buffers at both f_0 and $3f_0$ frequencies. With a dual-tank topology, $Tank_1$ is composed of two inductors, L_1 and L_2 (combined as a symmetric center-tapped inductor) and two accumulation-mode MOS varactors, $V_{\rm C1}$ and $V_{\rm C2}$, for generating the fundamental oscillation frequency at f_0. Also, $Tank_2$ consists of two transmission line inductors, $TL_{\rm S1}$ and $TL_{\rm S2}$, and two metal-insulator-metal (MIM) capacitors, $C_{\rm S1}$ and $C_{\rm S2}$, for obtaining the tripled frequency at the W-band. To further enhance the tuning range, a 1-bit switch capacitance $C_{\rm SW}$ is added to $Tank_1$, which can also lower $K_{\rm VCO}$ and reduce the reference spurious. Based on the simulated results, the tuning range can cover 25.5–29.7 GHz at the fundamental tone, which corresponds to 76.5–89.1 GHz at the W-band. Also, the simulated phase noise ($V_{tune}=0$ V) of the FT-VCO at f_0 (1 MHz offset) is -99.6 dBc/Hz, which is very similar to that without $Tank_2$ (-98.6 dBc/Hz).

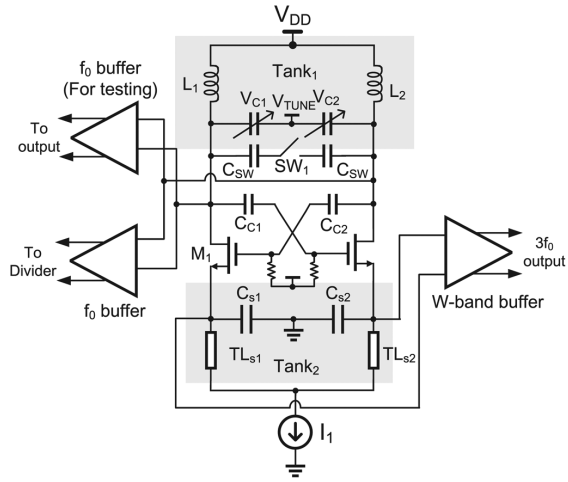


Fig. 4. Detailed circuit topology of the proposed frequency-tripling VCO including the buffer stages.

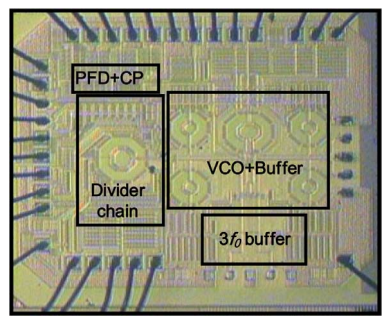
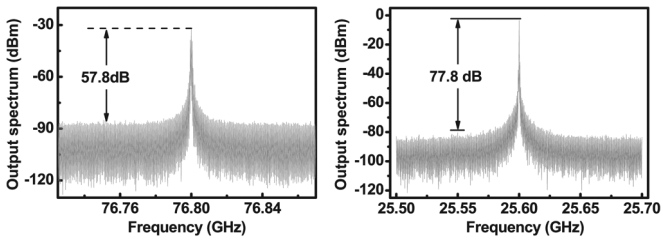


Fig. 5. Chip micrograph of the W-band PLL with the proposed FT-VCO.

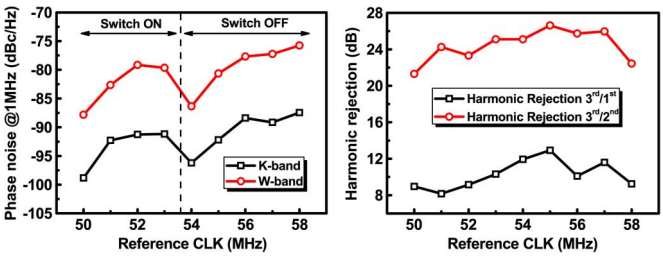
III. Experimental Results and Discussion

The proposed W-band PLL was realized using a 90 nm 1P9M CMOS process. The chip micrograph is shown in Fig. 5. where the chip size including the probing pads is 1.73 mm × 1.51 mm, and the active area is 1.2 mm × 1.1 mm. For the VCO and PLL



(a) (b)

Fig. 6. Output spectrum of the proposed PLL at (a) 3 f_0 and (b) f_0.



(a) (b)

Fig. 7. (a) Phase noises at f_0 and $3f_0$ of the PLL as a function of reference clock. (b) harmonic rejection at the output of W-band.

TABLE I
PERFORMANCE SUMMARY OF PLL AND COMPARISON WITH PRIOR WORKS

	This work	[1]	[8]	[9]
Technology	CMOS 90 nm	SiGe 130 nm	CMOS 65 nm	SiGe 0.18μm
Freq. (GHz)	76.2–89.1	92.7–100.2	70-78	96
TR (%)	15.6	7.8	10.8	10.9
PN (1MHz)	-87.9~-75.8	-102	-83	-92
Spur (dBc)	< -57.8	< -60	-49	-52
P_{diss} (mW)	62.4	469.3	76	140
P_{out} (dBm)	-29 ~-33.9	< 2	--	-11
Area (mm^2)	1.3	0.8	0.16	1.9

measurements, the DUT was mounted on a PCB to provide the DC bias supply, whereas the RF output signals were measured on wafer directly by using the RF probes. With a supply voltage of 1.2 V and loop bandwidth of 100 KHz, the power consumption of the W-band PLL was 62.4 mW. The standalone VCO was tested using an Agilent E4448 spectrum analyzer. The simulated tuning range is 73.89–87.06 GHz, and the corresponding measured result is 75.6–91.26 GHz. The spectrum, phase noise, and harmonic rejection were also measured for the PLL. Note that both W-and V- (only for harmonic rejection) band mixers and a W-band amplifier (only for phase noise) were employed for the measurements. In an input clock range of 49.8–58 MHz, the measured frequency locking range of PLL is 25.4–29.7 GHz at f_0, corresponding to 76.2–89.1 GHz at $3f_0$.

Fig. 6(a) and 6(b) show the output spectrums at 76.8 GHz (RBW = 1 KHz) and 25.6 GHz (RBW = 10 KHz), respectively, with a reference clock of 50 MHz, where the reference spur can only be observed at K-band. The already very low reference spur at K-band also implies that the observation of that at W-band would be even more difficult. Another reason may be the relatively large loss of the W-band mixer used for measurements, which makes the spurs below the noise floor. Fig. 7(a) shows the phase noise (at 1 MHz offset) of PLL as a function of the reference clock. As can be seen, the difference of phase noises between f_0 and $3f_0$ agrees very well with the theoretical value of 9.5 dB (20 log3). Note the 1-bit switch is designed with a relatively large transistor to minimize its impact on the Q of $Tank_1$. This is evident from the similar phase noises in both conditions when the switch is on and off. Fig. 7(b) presents the harmonic rejection measured at the W-band output. With the differential buffer, a relatively higher 2nd harmonic rejection can be observed compared with that of the fundamental rejection.

Table I summarizes the performance of the proposed W-band frequency PLL and comparison with prior works [8], [9]. It should be mentioned that the relatively low $P_{\rm out}$ in this design can be improved by increased stage number and power consumption of the buffer design. Also, we intentionally keep the circuit operating at low power due to the consideration of overall system power budget, which is a trade off with the phase noise.

IV. CONCLUSION

A W-band PLL was realized in a 90-nm CMOS technology. By using the proposed frequency tripling technique in the VCO design, a high performance W-band PLL can be achieved. With a single cross-coupled pair and a dual-tank topology, the W-band PLL demonstrated a wide tuning range up to 15.6% under a low power consumption of 62.4 mW.

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