A 24 GHz Low-Noise Amplifier Using RF Junction Varactors for Noise Optimization and CDM ESD Protection in 90 nm CMOS

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***Abstract*—This letter presents an ESD-protected 24 GHz low-noise amplifier (LNA) in 90 nm CMOS using RF junction varactors for noise optimization and ESD protection simultaneously. One of the junction varactors, inserted as an extra gate-source capacitance, provides an effective CDM ESD protection, and is also used for power-constrained simultaneous noise and input matching. The measured results demonstrate a 2.7 A (corresponding to a 4 kV HBM) and an 11.4 A ESD protection levels using transmission line pulse and very fast transmission line pulse tests, respectively. Under a power consumption of 9.1 mW, the ESD-protected LNA presents a *NF* of 2.9 dB and power gain of 15.2 dB at the center frequency of 24 GHz.**

***Index Terms*—Charge device model (CDM), electrostatic discharge (ESD), low-noise amplifier (LNA), transmission line pulse (TLP), very fast transmission line pulse (VFTLP).**

I. INTRODUCTION

ELECTROSTATIC discharge (ESD) becomes a major reliability concern for IC chip manufacturing, especially when using the modern CMOS technology with reduced gate oxide thickness and lowered breakdown voltage [1]–[3]. Recently, the charge-device-model (CDM) ESD protection has received increasing attention owing to the trend of system-on-chip (SOC) [4], [5]. The SOC chips are typically fabricated in advanced CMOS technology with a thinner gate oxide and a much larger chip size than before. The large substrate could accumulate a considerable amount of charges, resulting in a high ESD discharge peak current during CDM events. Conventionally, the CDM protection device is added to the gate of the input (buffer) stage using gate-grounded NMOS in logic products. However, this approach often introduces significant parasitic capacitance along the signal path that is not suitable for RF applications [4].

In this letter, we propose a new ESD network topology for LNA with an emphasis on CDM protection. The RF junction varactors are utilized as the ESD protection devices and co-designed with the LNA core circuit at 24 GHz in 90 nm CMOS. By co-optimization of ESD protection, noise figure, gain and power consumption, a 24 GHz low-noise amplifier in 90 nm CMOS demonstrates a 2.7 A and an 11.4 A current levels under TLP and VFTLP ESD tests, respectively. Also, the LNA presents a *NF* of 2.9 dB and an associated power gain of 15.2 dB under a power consumption of 9.1 mW.

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II. CIRCUIT TOPOLOGY

A. Co-Design of LNA and ESD Protection Network

By using the ESD/matching co-design approach [6], [7], the proposed ESD-protected LNA is realized in 90 nm CMOS. The schematic and chip micrograph are shown in Fig. 1(a) and (b), respectively. The varactors are co-designed with the input matching network which includes JV_{T} and JV_{B}, gate inductor L_{G}, source inductor L_{S}, and JV_{GS}. The cascode configuration with source inductive degeneration has the advantages of reduced Miller effects, improved input/output isolation, enhanced amplifier stability, and also the possibility of simultaneous noise and input matching. The drain inductor L_{D} functions as the inductive peaking and also the output matching to 50 Ω. The resistor R_{B} is connected between the gate of M_2 and V_{DD} to provide the dc gate potential and the shunt capacitor C_{B} is used for a good ac ground.

The ESD network includes three junction varactors JV_{T}, JV_{B}, and JV_{GS}, and a power clamp connected between V_{DD} and ground. The first two varactors are employed as the primary ESD protection for the direct ESD paths of the PD and NS modes, and also for the PS and ND modes along with the power clamp [6]. The varactor JV_{GS} serves as two purposes; one is to incorporate with the intrinsic C_{GS} of the transistor M_1 to achieve power-constrained simultaneous noise and input matching (PCSNIM) condition [8]. The extra gate-source junction varactor is critical for achieving PCSNIM by increasing the effective gate-source capacitance while maintaining a small transistor size of M_1 for low power operation. Most importantly, this varactor provides efficient CDM ESD protection during ESD zapping.

The CDM event describes the self-discharge procedure of the charges accumulated in the body of ICs through a certain grounded pin. When a CDM ESD event occurs, the circuit may be damaged before the primary ESD protection circuit turns on, since a huge current level up to $\sim$ 10 A could be reached in a short period of time ~ 1 ns [4], [5]. In a practical situation, the most critical CDM current path is from V_{SS} (body) to RF_{in} (NS mode) [9], and it is most likely the discharge current will flow directly through the gate of M_1, owing to the low impedance path provided by the gate capacitance under the high frequency signal of the CDM event. With the ESD device JV_{GS} put close to the gate oxide of M_1, the junction varactor can be quickly

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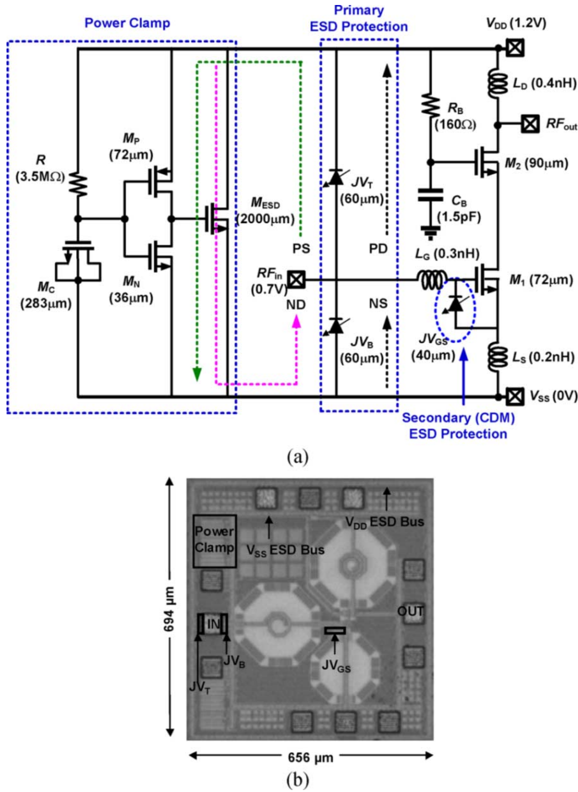

(a)

(b)

Fig. 1. (a) Schematic of the ESD-protected LNA. Different ESD testing modes are also indicated. (b) Chip micrograph of the proposed ESD-protected LNA.

turned on to bypass the large ESD current and protect the vulnerable gate oxide of M_1. As a part of the ESD current path, L_G and L_S are designed by metal lines with a 6-μm width to sustain large ESD current. Also, the RC-inverter-triggered NMOS power clamp with a large total width ($\sim$ 2000 μm) provides a low-impedance path between V_{DD} power-rail to ground. Note all the varactors are reversed biased under normal RF operation.

B. Characterization of Junction Varactors for ESD Protection

In contrast to the typical applications for voltage-controlled oscillators [10] or tunable matching network [11], the RF junction varactors employed for ESD protection must be able to sustain a large ESD current. By adding sufficient vias and large metal widths at both anode and cathode along the ESD paths, the varactors are customized to have small on-resistance and high secondary breakdown current (It_2) for high ESD protection levels.

In this design, the multi-finger topology is used for the varactors, which has the advantages of smooth ESD current flow, large periphery per unit area, reduced on-resistance, and easy for metal routing. Also, a minimum device length of 0.2 μm (limited by the design rule) is selected for the improved ratio of the ESD level to the parasitic capacitance C_{ESD}. For a junction varactor, the parasitic capacitance mostly exists in the bottom area, whereas the ESD current flows mainly through the edges of the junction. With a small device length, the total periphery and hence the ESD current can be maximized while maintaining a small area and parasitic capacitance. Table I summarizes the TLP ESD test results of the junction varactors with different device parameters. As expected, the ESD protection level increases with the finger number N and the width W of each finger. The parasitic capacitance also increases with the device size. These experimental studies indicate that RF junction varactors can be utilized to achieve desired ESD protection level with small parasitic capacitances if the device geometry and size are properly designed and selected.

TABLE I
ESD PERFORMANCE COMPARISON OF DIFFERENT DEVICE PARAMETERS

Parameters	W	L	N	It_2(TLP)	ESD	C_{ESD}	ESD/C_{ESD}
Unit	μm	μm	--	A	kV	fF	V/fF
W1N25	1	0.2	25	0.8	~ 1.2	15.3	~ 78
W2N25	2	0.2	25	1.5	~ 2.3	28.9	~ 79
W5N25	5	0.2	25	1.8	~ 2.7	69.9	~ 39
W1N50	1	0.2	50	1.7	~ 2.5	30.6	~ 82
W2N50	2	0.2	50	3.0	~ 4.5	57.9	~ 78
W5N50	5	0.2	50	4.0	~ 6.0	139.8	~ 43

* ESD levels are estimated from the TLP measurements (~ $It_2 * 1.5$kΩ).

In practical co-design procedure, the sizes of M_1, M_2, and the bias voltages are determined first with the considerations of power dissipation, gain, and noise. The ESD blocks (JV_{GS}, JV_T and JV_B) are then designed with the considerations of estimated protection levels and treated as a part of the input matching network to optimize noise and power gain performance at the center frequency of 24 GHz. It should be pointed out that the ratio of ESD level to C_{ESD} is still important but not that critical in the co-design scheme. As a part of the matching network, the capacitances of the ESD blocks provide more design freedom, and somehow relax the tradeoff between the circuit performance and ESD level.

III. MEASURED RESULTS AND DISCUSSION

The ESD-protected LNA was fabricated using a 90 nm CMOS process with a total chip area of 0.46 mm^2 including the probing pads. The RF and ESD characteristics were both measured on-wafer. The Human-Body Mode (HBM) testing was performed by TLP test (Barth 4002) with a pulse of 10 ns rise time and 100 ns width. The CDM ESD robustness was characterized by VFTLP test (HANWA HED-T5000) with a pulse of 0.2 ns rise time and 1 ns width. The ESD failure level of the circuit was monitored by a dc leakage measurement performed after each pulse.

Fig. 2 shows the measured and simulated S_{11}, S_{21}, and *NF* and NF_{MIN} of the ESD-protected LNA. The LNA presents a peak power gain of 15.2 dB and a minimum *NF* of 2.9 dB at 24 GHz with the input return loss greater than 10 dB, demonstrating the successfully designed input-matching network using the co-design approach with JV_T, JV_B, and JV_{GS}. Also, the well agreed NF_{MIN} and *NF* at 24 GHz indicate that the simultaneous noise and input matching is achieved. The measured $P_{1\ dB}$ and *IIP*3 are -15.1 and -5.3 dBm, respectively. It should be mentioned that if JV_{GS} is replaced by a typically used MIM capacitor, there is no obvious difference in LNA characteristics. Based on simulation, the *IIP*3 changes from -4.7 to -4.1 dBm, the *NF* reduces by 0.25 dB, and the power gain improves by 0.27 dB with the MIM capacitor. Fig. 3 shows the test results of different ESD testing modes (PD, PS, ND, and NS) for the LNA [6]. The PD mode presents a second breakdown current It_2 up to 1.7 A, corresponding to an ESD level of 2.5 kV. In the PS mode, the TLP curve shows a similar on-resistance and ESD level, but with an offset voltage of $\sim$ 1.3 V due to the power clamp, compared to the PD mode. Note that in the NS mode, the TLP I-V curve show smaller

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED 24-GHZ LNAS WITH PRIOR ARTS

Ref.	Tech. (nm)	Freq. (GHz)	Gain (dB)	NF (dB)	S_{11} (dB)	S_{22} (dB)	Power (mW)	P_{1dB} (dBm)	IIP3 (dBm)	ESD (kV)	VFTLP (A)
This work	90 CMOS	24	15.2	2.9	-12	-13	9.1	-15.1	-5.3	4.0/2.5	11.4
[12]	90 CMOS	24	7.5	3.2	-16	-30	10.6	--	--	--	--
[13]	130 CMOS	24	14.0	5.0	-7	-15	18	-14.1	-1.7	3.5/2.5	--
[14]	180 CMOS	24	13.1	3.9	-15	-20	14	-12.2	0.54	--	--

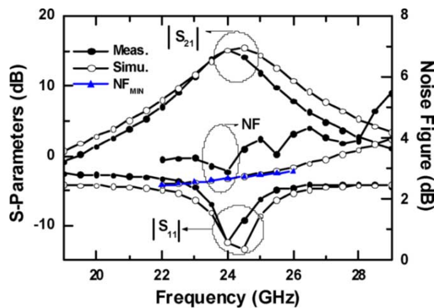

Fig. 2. Measured and simulated S_{11}, S_{21}, and *NF* of the ESD-protected LNA.

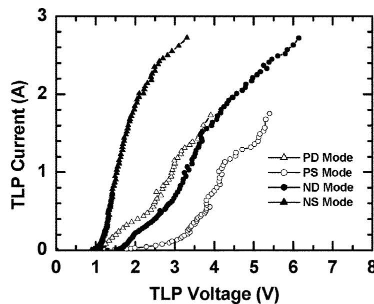

Fig. 3. Measured TLP I-V characteristics of the ESD-protected LNA. The last point indicates the failure current It_2.

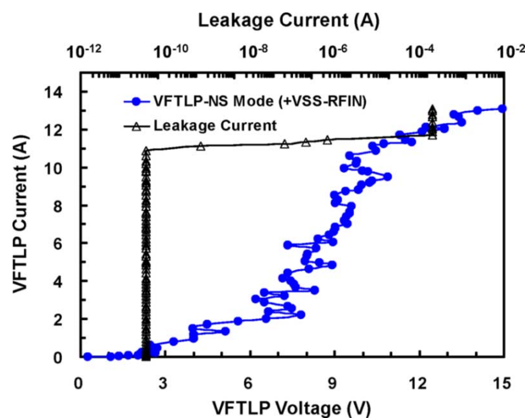

Fig. 4. Measured VFTLP I-V and leakage characteristics of the ESD-protected LNA.

on-resistance compared with the PD mode, indicating an auxiliary ESD path goes through JV_{GS}. Compared to a single ESD path in the PS (PD) mode, the NS (ND) mode with an additional ESD path enhances It_2 up to 2.7 A, corresponding to a 4 kV ESD level.

The VFTLP test was employed to evaluate the ESD protection capability under the CDM events [5], in which the ultra-short pulse describes the first peak of the CDM current waveform [9]. Fig. 4 illustrates the measured VFTLP I-V and leakage characteristics of the LNA, and an 11.4 A current level is reached. Table II compares this work with other published 24 GHz LNAs [12]–[14]. The proposed LNA achieves a lowest *NF* of 2.9 dB and a highest gain under a power consumption of 9.1 mW. Also, the LNA demonstrates a VFTLP ESD protection level up to 11.4 A, which has not been reported before for the CMOS LNA operating in this frequency range to the best of our knowledge.

IV. CONCLUSION

An ESD-protected 24 GHz LNA was realized in 90 nm CMOS technology using the proposed RF junction varactors for noise optimization and CDM ESD protection simultaneously. Under a power consumption of 9.1 mW, the LNA presented a *NF* of 2.9 dB with an associated power gain of 15.2 dB. Also, a 2.7 A TLP current level (corresponding to 4 kV HBM) and an 11.4 A VFTLP ESD protection level have been demonstrated.

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