A Wideband Low Noise Amplifier With 4 kV HBM ESD Protection in 65 nm RF CMOS

Ming-Hsien Tsai, Shawn S. H. Hsu, Fu-Lung Hsueh, Chewn-Pu Jou, Sean Chen, and Ming-Hsiang Song

***Abstract*—This study presents a wideband low noise amplifier (LNA) including electrostatic discharge (ESD) protection circuits using 65 nm CMOS with a gate oxide thickness of only $\sim$2 nm. By co-designing the ESD blocks with the core circuit, the LNA shows almost no performance degradation compared to the reference design without ESD. Under a power consumption of only 6.8 mW, the silicon results show that the LNA can achieve a peak power gain of 13.8 dB. Within the 3 dB bandwidth from 2.6 GHz to 6.6 GHz, the noise figure (NF) is in a range of 4.0 dB to 6.5 dB and the input reflection coefficient S_{11} is below -13.0 dB. Using the miniaturized Shallow-Trench-Isolation (STI) diode of $\sim$40 fF capacitance and a robust gate-driven power clamp configuration, the proposed LNA demonstrates an excellent 4 kV human body mode (HBM) ESD performance, which has the highest voltage/capacitance ratio ($\sim$100 V/fF) among the published results for RF LNA applications.**

***Index Terms*—CMOS, Electrostatic discharge (ESD), low noise amplifier, wideband.**

I. Introduction

RAPID scaling of the feature size has made CMOS technology the most attractive candidate for RF system-on-chip (SOC) applications. The impressive frequency response of the transistors eases the requirement of achieving high speed circuit operation, while the reduced gate oxide thickness and lowered breakdown voltage pose a tremendous challenge for the on-chip electrostatic discharge (ESD) protection design since the sensitive gate oxide of the MOSFET is exposed to the overall ESD voltage drop directly [1], [2]. It is inevitable that the ESD protection devices introduce additional parasitic capacitances and resistances to the circuit especially when a high ESD robustness is required. In general, a tradeoff exists between the parasitic capacitance and ESD level. This effect becomes more critical for RF front-end circuits, which could seriously degrade the input reflection coefficient, gain, bandwidth, and also noise characteristic [3]. For RFIC design, the ESD protection circuit can no longer be treated separately. Instead, it must be considered simultaneously with other blocks for achieving best overall performance [4].

Manuscript received May 15, 2009; revised July 08, 2009. First published October 20, 2009; current version published November 06, 2009. This work was supported by the National Tsing Hua University—Taiwan Semiconductor Manufacturing Company Joint-Development Project.

M. Tsai and S. Hsu are with the Department of Electrical Engineering and Institute of Electronics Engineering, National Tsing Hua University, Hsinchu 300, Taiwan (e-mail: shhsu@ee.nthu.edu.tw).

F. Hsueh, C. Jou, S. Chen, M. Song, and M. Tsai are with the Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu 300, Taiwan.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LMWC.2009.2032019

Different techniques were reported for wideband RF LNA design, while only a few works include the ESD protection [5]–[10]. In this study, we report a wideband LNA with a high level of ESD protection and no NF and gain degradation using 65 nm MOS transistors. Compared with published ESD-protected wideband LNAs, the employed STI-based diode has an extremely small parasitic capacitance $C_{\rm ESD}$ of $\sim$40 fF (other works are in the range of 100–200 fF [1]–[3], [10], and can only pass ESD level below 2.5 kV), while achieving an ESD protection level up to 4 kV with a very thin gate oxide of $\sim$2 nm (other works are in the range of 2.5–5 nm) [1], [3], [7]–[10]. In addition, a robust power clamp is employed to ease the requirement of the diodes for ESD protection. As a result, the miniaturized ESD diode is virtually invisible in the desired frequency band, and thus the ESD-protected LNA has almost no performance degradation compared with the reference design (typical NF degradation is in the range of 0.5–1.5 dB in other works [3], [11]). In this study, a 2.6–6.6 GHz wideband LNA with a 13.8 dB power gain and a 4.0 dB noise figure is demonstrated with an excellent 4 kV Human Body Mode ($V_{\rm HBM}$) ESD performance. This design also achieves the highest figure-of-merit (FOM) of $V_{\rm HBM}/C_{\rm ESD}$ [12] among the published results for ESD-protected RF LNAs.

II. Circuit Topology

A. LNA Configuration

Fig. 1 shows the wideband LNA with the ESD protection scheme consisting of the diodes and power clamp. As shown in Fig. 1, the LNA is designed by a cascode configuration with a RC shunt-shunt feedback. The transistors $\rm M_1$ and $\rm M_2$ have the gate widths of 64 μm and 52 μm, respectively. By proper adjusting of the resistive component $R_{\rm f}$ in combination with the reactive component $C_{\rm f}$, a flat S_{21} can be achieved over a wide bandwidth with low input/output reflection coefficients. The final selected values for $R_{\rm f}$ and $C_{\rm f}$ are 1.2 k Ω and 1.1 pF, respectively. A source degeneration inductor L_S of 0.2 nH and a gate inductor $L_{\rm g}$ of 2.7 nH are also employed in the common-source (CS) stage for a better wideband matching. A small inductor $L_{\rm p}$ of 70 pH is inserted between the CS and common-gate (CG) stages to further extend the bandwidth. Note that a large resistor $R_{\rm b}$ of 5 k Ω is used at the gate of CG stage to protect the gate oxide of $\rm M_2$ during an ESD zap. A capacitor $C_{\rm b}$ of 1 pF is employed to provide an ac ground of the CG stage. The inductor $L_{\rm d}$ of 9.3 nH functions as inductive peaking also for further bandwidth and gain enhancement. The transistors $\rm MB_1$ and $\rm MB_2$ are utilized as the output buffer to the 50 ohm measurement environment.

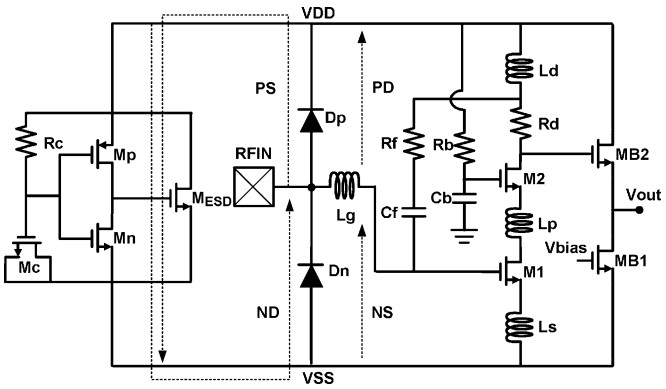

Fig. 1. Circuit topology of the proposed ESD-protected LNA.

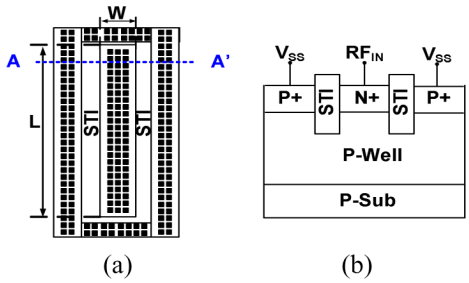

Fig. 2. (a) Layout view of the STI diode (the dots indicate high via and contact density). (b) Cross section view of the N+/PW STI diode.

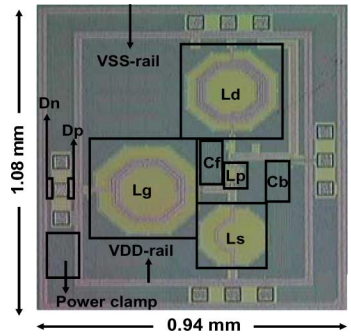

Fig. 3. Micrograph of the proposed ESD-protected LNA.

B. ESD Protection Circuits

The ESD protection blocks are also shown in Fig. 1, which is a double-diode topology ($D_{\rm n}$ and $D_{\rm p}$) together with the power clamp designed by four transistors ($M_{\rm n}, M_{\rm p}, M_{\rm C}$, and $M_{\rm ESD}$) and one resistor ($R_{\rm C}$). The discharge paths for the four different ESD testing modes, i.e., positive (PD mode) and negative (ND mode) to $\rm V_{DD}$, and positive (PS mode) and negative (NS mode) to $\rm V_{SS}$ are also indicated in the figure. In the PD and NS modes, the discharge current only flows through the diode, whereas the discharge paths include both the diode and clamp in the PS and ND modes.

The diodes at the input of the LNA play an important role for the ESD discharge paths, which are also critical for the input matching network. In this design, the two ESD diodes at the input are optimized together with the power clamp to have sufficient ESD performance whereas almost no effect on the input matching network at the desired frequency band. Fig. 2 shows the layout and cross section of the $\rm N+/PW(\mathit{D}_n)$ STI diode. As can be seen, the anode $\rm (N+)$ connected to RF input port $\rm (RF_{IN})$ is surrounded by STI and a single-finger configuration is used. A large length/width ratio ($\rm L = 30\ \mu m$ and $\rm W = 0.8\ \mu m$) is employed to maximize the overall perimeter. With this structure, the ESD parasitic capacitance primarily exists in the bottom area and the current flows mainly through the edges of the diodes. Such a design approach allows a large ESD current bypass capability with minimum area and parasitic capacitances. Note that the diode design utilizes the maximum allowed contact and via density to reduce series resistance. The multi-metal routing is also employed to prevent the electron-migration induced burn out. The overall metal width for anode/cathode interconnection is larger than 40 μm to sustain high ESD current. Compared with other reported works [1]–[3], [7]–[10], the designed STI-based diode consumes the smallest chip area of 24 $\mu\rm m^2$ with an associated parasitic capacitance of only $\sim$40 fF.

In addition, the gate-driven power clamp with a linear characteristic is employed, which has the advantage of a low turn-on voltage over the snapback-mode ESD structure. The MOS capacitor $M_{\rm C}$ and P-type poly resistor $R_{\rm C}$ result in a RC time delay to ensure $M_{\rm ESD}$ functions correctly during an ESD event. Note that $M_{\rm ESD}$ is designed by a multi-finger topology with a total gate width up to $\sim$2000 μm to sustain a high ESD current level. The large size of $M_{\rm ESD}$ with a low on-resistance also allows the power clamp to consume less voltage budget under a certain current level, and thus relaxes the ESD diode design requirement. The power clamp can sustain an ESD level up to 8 kV in our design, as will be shown later.

III. Results and Discussion

Fig. 3 shows the chip micrograph of the fabricated ESD-protected LNA in a 65 nm 1P6M RF CMOS technology. The total chip area is $\sim$1 $\rm mm^2$. As can be seen, the diodes only consume very small chip area and the power clamp is placed close to the amplifier input to minimize the IR voltage drop.

A. RF Characteristics

The RF characteristics of both LNAs (with and without ESD) were measured on-wafer. The circuits were biased under a 1.2 V supply with an associated drain current of 5.7 mA. The measured S_{11} and S_{21} are shown in Fig. 4. Fig. 5 shows the measured noise figure. The two amplifiers have almost identical characteristics, which indicate the impact of the ESD block has been successfully minimized by co-designing with the LNA core circuit. Within the 3 dB bandwidth, the input return loss is greater than 13.0 dB, the peak power gain can achieve 13.8 dB, and the noise figure is in a range of 4.0 dB to 6.5 dB.

B. ESD Testing Results

The HBM test is a commonly used method to evaluate ESD protection. A 2 kV HBM ESD level refers to a current of 1.34 A. Fig. 6 shows the *Transmission line pulse* (TLP) test results of the $V_{\rm DD} - V_{\rm SS}$ path, which can provide the information of ESD capability for the power clamp. The result indicates that the power

TABLE I
PERFORMANCE COMPARISON OF RF WIDEBAND ESD-PROTECTED LNA WITH PRIOR ART

Ref.	Tech. (nm)	BW (GHz)	NF (dB)	P_{DC} (mW)	S_{21} (dB)	S_{11} (dB)	P_{1dB} (dBm)	ESD (kV)	FOM(V/fF)
This work	**65 CMOS**	**2.6-6.6**	**4.0**	**6.8**	**13.8**	**<-13**	**-17.6 @ 4GHz**	**4.0**	**100**
[1]	90 CMOS	0.1-8	3.4	16.0	16.0	<-10	NA	2.25	18
[2]	90 CMOS	0.75-10	7.5	78.0	13.0	<-10	NA	2.0	40
[9]	130 CMOS	3-5	3.6	45.0	25.8	-11	-22.7 @ 4GHz	1.5	–
[3]	180 CMOS	0.5-3	3.8	73.2	16.0	<-10	NA	4.6	20
[10]	180 BiCMOS	DC-10	4.7	3.65	19.1	<-10	-17.1 @ 5.2 GHz	1.5	75

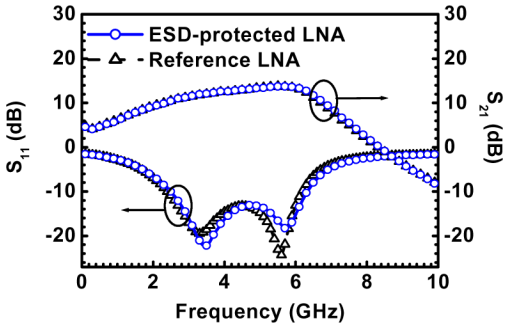

Fig. 4. Measured S_{11} and S_{21} of LNAs with/without ESD protection.

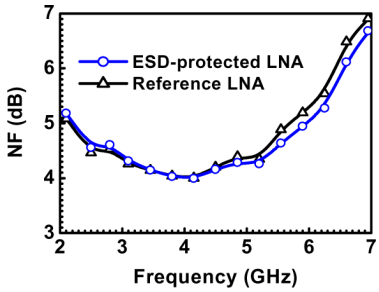

Fig. 5. Measured NF of LNAs with/without ESD protection.

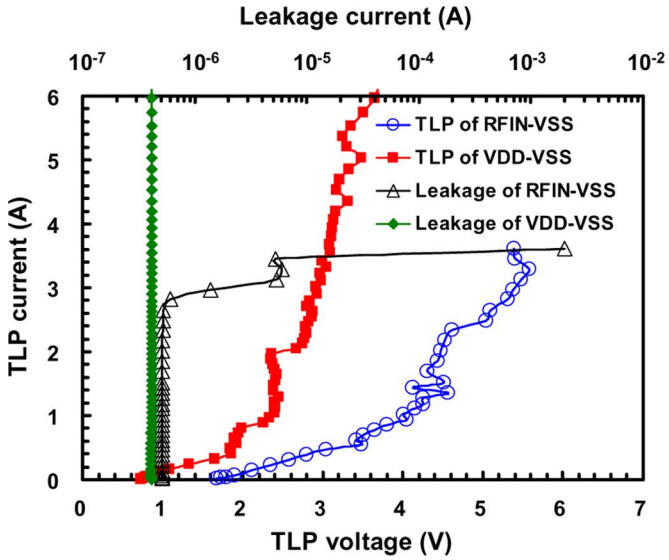

Fig. 6. TLP curves and the corresponding leakage currents.

clamp can sustain a current level above 5.36 A, which is corresponding to an HBM ESD level exceeding 8 kV. Fig. 6 also shows the result of the $\mathrm{RF_{IN}} - V_{\mathrm{SS}}$ path (PS mode), which represents the worst case among the different ESD test combinations. The sudden increase of the leakage current indicates that a second breakdown current up to 2.8 A can be achieved corresponding to an ESD level of 4 kV. Table I compares the published RF wideband LNAs with the considerations of ESD protection. The proposed wideband LNA achieves high gain and low NF under low power consumption with an ESD protection level among the best compared to other works. In addition, the proposed LNA achieves the highest FOM among the published wideband RF LNAs.

IV. CONCLUSION

In this study, we demonstrated a wideband (2.6–6.6 GHz) LNA with an excellent 4 kV HBM ESD performance using 65 nm CMOS. The proposed LNA can achieve a power gain of 13.8 dB and a noise figure of 4.0 dB. With careful consideration of the ESD blocks during the RF design, the RF performance of the LNA was virtually unaffected by the additional ESD protection blocks.

REFERENCES

[1] T. Chang, J. Chen, L. Rigge, and J. Lin, "A packaged and ESD-protected inductorless 0.1–8 GHz wideband CMOS LNA," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 6, pp. 416–418, Jun. 2008.

[2] W. Soldner, M. Kim, M. Streibl, H. Gossner, T. H. Lee, and D. Schmitt-Landsiedel, "A 10 GHz broadband amplifier with bootstrapped 2 kV ESD protection," in *IEEE ISSCC Tech. Dig. Tech.*, 2007, pp. 550–551.

[3] D. Linten, S. Thijs, J. Borremans, M. Dehan, D. Tremouilles, M. Scholz, M. Natarajan, P. Wambacq, and G. Groeseneken, "T-diodes—A novel plug-and-play wideband RF circuit ESD protection methodology," in *Proc. EOS/ESD Symp.*, Sep. 2007, pp. 242–249.

[4] A. Wang, H. Feng, R. Zhan, G. Chen, and Q. Wu, "ESD protection design for RF integrated circuits: New challenges," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2002, pp. 411–418.

[5] Y. Lin, S. Shawn, J. Jin, and C. Chan, "A 3.1–10.6 GHz ultra-wideband CMOS low noise amplifier with current reused technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 3, pp. 232–234, Mar. 2007.

[6] M. T. Reiha and J. R. Long, "A 1.2 V reactive-feedback 3.1–10.6 GHz low-noise amplifier in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1023–1033, May 2007.

[7] M. D. Ker, Y. Hsiao, and B. Kuo, "ESD protection design for 1- to 10-GHz distributed amplifier in CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2672–2681, Sep. 2005.

[8] M. D. Ker and B. Kuo, "ESD protection design for broadband RF circuits with decreasing-size distributed protection scheme," in *Proc. Radio Freq. Integr. Circuits Symp.*, Jun. 2004, pp. 383–386.

[9] R. Salerno and M. Tiebout, "ESD-protected CMOS 3–5 GHz wideband LNA + PGA design for UWB," in *ESSCIRC Tech. Dig.*, 2005, pp. 219–222.

[10] K. Bhatia, S. Hyvonen, and E. Rosenbaum, "A compact, ESD-protected, SiGe BiCMOS LNA for ultra-wideband applications," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1121–1130, May 2007.

[11] D. Linten, L. Aspemyr, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Thijs, R. Garcia, H. Jacobsson, P. Wambacq, S. Donnay, and S. Decoutere, "Low-power 5 GHz LNA and VCO in 90 nm RF CMOS," in *IEEE Symp. VLSI Circuits Tech. Dig.*, Jun. 2004, pp. 372–375.

[12] E. Rosenbaum and S. Hyvonen, "On-chip ESD protection for RF I/Os: Devices, circuits and models," in *Proc. IEEE Symp. Circuits Syst. (ISCAS)*, May 2005, pp. 1202–1205.