A 56.5–72.2 GHz Transformer-Injection Miller Frequency Divider in 0.13 μm CMOS

Wei-Sung Chang, Kai-Wen Tan, and Shawn S. H. Hsu

***Abstract*—A V-band Miller frequency divider with a locking range of 15.7 GHz ($f_0 = 64$ GHz) is realized in 0.13 μm CMOS technology. Using the proposed transformer-injection technique, the signal can be injected into the mixer core directly without the current and impedance limitations of the input stage. The divider also features a fully differential topology. Under the condition of $V_{DD} = 0.9$ V, the divider can even function with a power dissipation of only 0.81 mW.**

***Index Terms*—CMOS, frequency divider, transformer, V-band.**

I. Introduction

CONTINUOUS scaling in CMOS technology is beneficial to circuit design for millimeter-wave wireless communications with increased data rate. Currently, the unlicensed band from 57 to 64 GHz with a 7 GHz bandwidth attracts strong interest in both industry and academia for the applications of wireless home video and data link. It is a challenge to realize a CMOS transceiver operating in this frequency band, and a wideband frequency divider is a key building block of the frequency synthesizer in the transceiver. The flip-flop-based static divider has a wide locking range, but it suffers from high power dissipation and limited operation frequencies. On the contrary, the resonator-based divider has the advantages of high operation frequencies and low power consumption but with a relatively small locking range [1], [2]. In this letter, a resonator-based Miller frequency divider is presented for V-band (40–75 GHz) applications. Using the proposed transformer-injection technique, the divider demonstrates a wide locking range up to 15.7 GHz while maintaining low power consumption. Under the condition of $V_{DD} = 0.9$ V, the divider can even function with a power dissipation of only 0.81 mW.

II. Circuit Topology

The concept of the Miller divider is illustrated in Fig. 1, in which the loop consists of a mixer and a bandpass filter. By retaining the $\omega_{\rm in}/2$ component in the feedback path, this divider functions with a division ratio of two at the output. Compared with the drain-pumped passive mixers [3]–[6], the Gilbert mixer is more desirable for the Miller divider due to its high conversion gain to satisfy the Barkhausen criterion in the feedback loop. A Gilbert mixer with inductive loads is also shown in Fig. 1. A bandpass filter can be formed at the IF output by utilizing the device parasitic capacitances together with the inductors. With the IF port connected back to the RF or LO port, the feedback loop is completed and a Miller divider as illustrated in the block diagram can be realized.

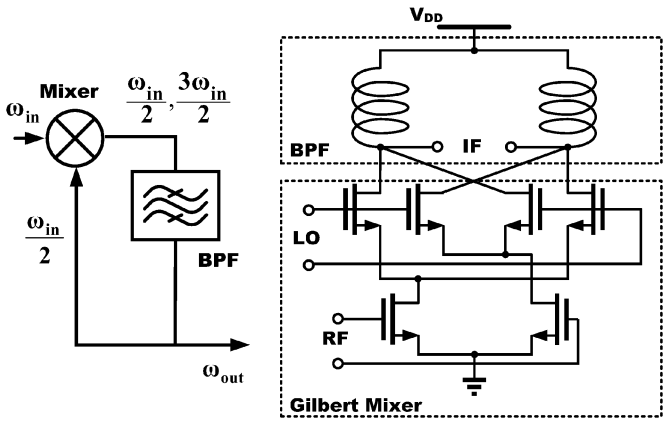

Fig. 1. Block diagram of Miller frequency divider and Gilbert mixer with bandpass load.

In this configuration, small transistors for the input common-source stage are preferred for high frequency and low power operation in practical design. However, the driving current of the mixer core is limited by the bias current and transconductance of the input stage. In addition, the constrained transistor size with undesired impedance may result in signal reflection at the input port and degrade the divider locking range. It was suggested that the internal injection power is important to the locking range of the divider [7]. For the Miller divider as shown in Fig. 1 with the gate injection, the locking range can be enhanced by maximizing the internal injection power if the input signal has an alternative injection path to the mixer core providing an additional current path with wideband and low-impedance characteristics.

To improve the internal injection power for a wide locking range, a transformer-injection Miller frequency divider is proposed as shown in Fig. 2. Using a transformer at the input port, the RF signal is coupled into the mixer core directly, i.e. the sources of the transistors in the switching stage (M_3, M_4, M_5, and M_6) instead of injecting into the gates of the input stage only (M_1 and M_2). The secondary coil of the transformer provides an additional current path for the mixer driving current which is limited by the input-stage transistors in the conventional gate-injection configuration. Through the transformer, the coupled input signal across the secondary coil induces a large current in the mixer core due to the low impedance looking into

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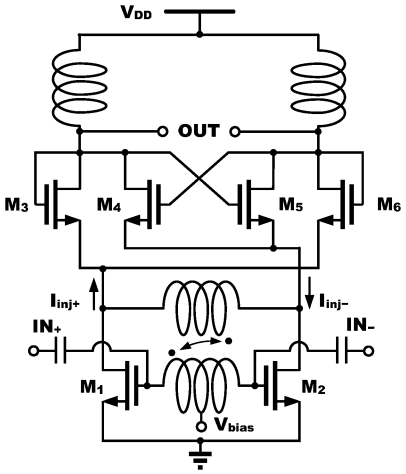

Fig. 2. Proposed transformer-injection Miller frequency divider.

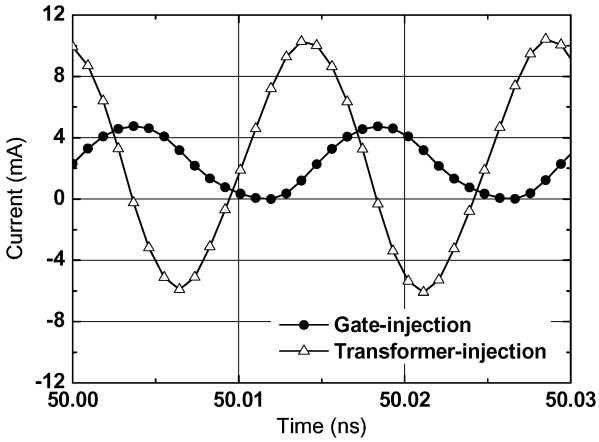

Fig. 3. Simulated current injection levels for the two different designs.

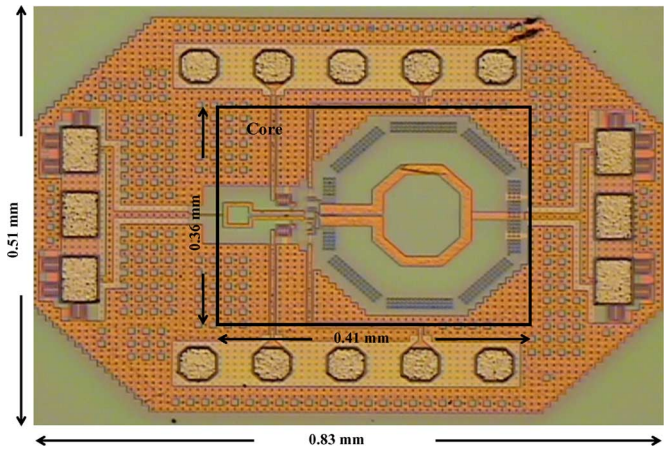

Fig. 4. Chip micrograph of the Miller frequency divider.

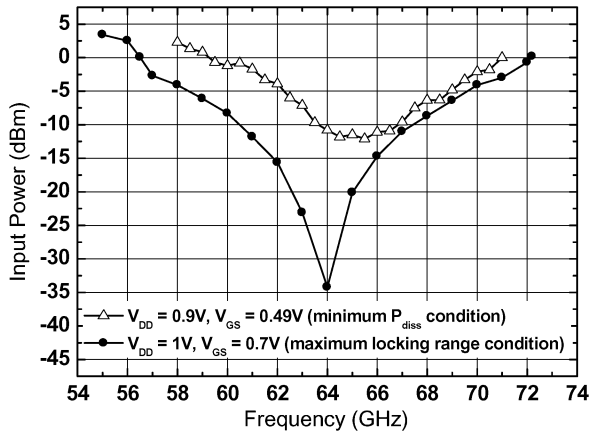

Fig. 5. Measured input sensitivity curves under $V_{DD} = 0.9$ V and 1 V.

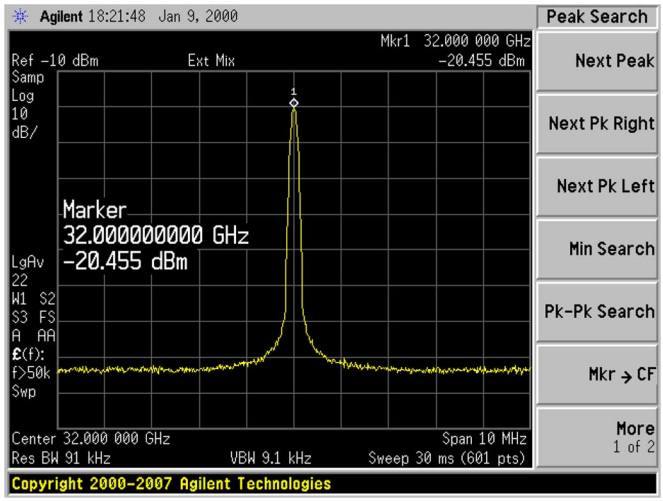

Fig. 6. Output spectrum under a 0 dBm input at 64 GHz.

the switching stage. The transformer input also provides a wideband and low-impedance signal path to ease the external power injection. As a result, the conversion gain of the mixer increases leading to an improved locking range under the same external injection power and a low bias current. In addition, compared to the direct injection-locked design with a single-ended input [1]–[7], the transformer injection allows applying the input differential signal directly without the need of differential-to-single conversion in a fully differential architecture.

Note that the transformer also functions as inductor shunt peaking to increase the locking range and operation frequency. A shunt inductor was used to resonate with the parasitic capacitances at the source nodes of the switching stage for a Miller divider [7]. In this design, the two coils of the transformer with mutual inductance can further enhance the resonance of the parasitics. The primary coil of the transformer connecting the two gate nodes of the input stage also serves as the RF choke to simplify the bias scheme of the divider. It should be notice that the quality factor of the resonator is also critical to the locking range. In this design, the quality factor of the resonator is $\sim$30 to have enough loop gain while also maintaining a wide locking range. The transformer has a relatively lower quality factor of $\sim$14 thus it can function as an additional injection path but not a limiting factor of the locking range. The feedback loop is completed by connecting the mixer IF output back to the LO port rather than the RF port. In this way, there is no need for additional dc block capacitors [8] or level-shift circuits [9], [10].

Fig. 3 compares the simulated results of the dividers with two different input stages, one is the conventional gate-injection design, and the other is the proposed transformer-injection divider.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

Ref. Divider	Tech.	P_{in} (dBm)	Locking Range (GHz)		V_{DD}	P_{diss} (mW)	FOM (GHz/mW)
[1]	0.13 µm CMOS	0	26.3 – 32.5	(6.2GHz, 25%)	1.2	1.86	3.3
[2]	0.13 µm CMOS	0	59.6 – 66.96	(7.4GHz, 11.7%)	0.8	1.6	4.6
[3]	0.18 µm CMOS	0	38.6 – 49.2	(10.6GHz, 24%)	1	6	1.77
[4]	65 nm CMOS	0	128.24 – 137	(8.76GHz, 6.6%)	1.1	5.5	1.59
[5]	0.13 µm CMOS	4	66.4 – 76	(9.6GHz, 13.6%)	1	4.4	2.18
[6]	0.13 µm CMOS	0	49.8 – 62	(12.2GHz, 21.8%)	1	9.72	1.26
[8]	0.18 µm CMOS	4	38.3 – 40.6	(2.3GHz, 6%)	2.5	16.8	0.14
[11]	90 nm CMOS	0	39 – 52	(13GHz, 29%)	0.8	0.8	16.25
This work*	0.13 µm CMOS	0	59.5 – 71	(11.5GHz, 17.6%)	0.9	2.05	5.61
This work**	0.13 µm CMOS	0	56.5 – 72.2	(15.7GHz, 24.4%)	1	4.65	3.38

$\mathrm{FOM} = \mathrm{Locking\ range}/\mathrm{P_{diss}}$ [2]
*Biased for low power operation (minimum $\mathrm{P_{diss}}$ for operation is 0.81 mW)
**Biased for wide locking range operation (maximum locking range up to 15.7 GHz)

It is clear that the proposed transformer injection technique effectively increases the injected current level $(I_{\mathrm{inj}}+)$, resulting in a 3.2× improvement. The simulation results also demonstrate that the locking range (0 dBm input level) is increased by 2.5× from 58.8–65.4 GHz (gate-injection) to 55.4–71.6 GHz with the transformer input stage.

III. RESULTS AND DISCUSSION

The circuit was fabricated using a standard 0.13 μm CMOS technology with a chip area of $0.83 \times 0.51\ \mathrm{mm}^2$ including the RF and dc probing pads (core area: $0.41 \times 0.36\ \mathrm{mm}^2$). The chip micrograph is shown in Fig. 4. The circuit is measured on-wafer in a differential configuration and the results are shown in Fig. 5. The circuit can function under the bias condition of $V_{DD} = 0.9$ V and $V_G = 0.49$ V with a power consumption of 0.81 mW, and the input level is around −12 dBm. It is observed that the circuit has no self oscillation under this bias condition if no input signal is applied due to insufficient loop gain for the Barkhausen criterion. With the additional power from the injected signal, the criterion is fulfilled and the divider can still function properly. The power consumption also increases with the injected signal level since the increased transient gate voltages of M1 and M2 result in higher drain currents of the transistors, and $\mathrm{P_{diss}}$ becomes 2.05 mW at a 0 dBm input power level. The corresponding locking range is 11.5 GHz under this condition. As the bias voltage increases to $V_{DD} = 1$ V and $V_G = 0.7$ V with a power consumption of 3.78 mW, a self oscillation of the divider at 31.84 GHz occurs. A clear notch at 64 GHz with an input power level of −35 dBm is observed from the input sensitivity characteristics. As the input signal level increases to 0 dBm, the power consumption becomes 4.65 mW, and the locking range is enhanced to 15.7 GHz from 56.5 to 72.2 GHz. The measured output spectrum of the divider with the input signal at 64 GHz under a 0 dBm input power is shown in Fig. 6 ($V_{DD} = 1$ V). The measured phase noise of the input signal is −109.2 dBc/Hz at 1 MHz offset and that for the divided output signal is −117.1 dBc/Hz. Table I presents the performance summary and the comparison with the prior arts [11]. As can be seen, the proposed design using the transformer-injection configuration has the FOM among the best compared with the results listed in Table I.

IV. CONCLUSION

In this study, we demonstrated a wide-locking range frequency divider using the proposed transformer-injection technique. Under a Vdd of 0.9 V, the divider can function with a power dissipation of only 0.81 mW. As Vdd increased to 1 V, the divider can achieve a 15.7 GHz locking range with a 4.65 mW power consumption.

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