A 40-Gb/s 4-V_{pp} Differential Modulator Driver in 90-nm CMOS

Yan-Feng Li, Po-Wei Chiu, Ke Li, David J. Thomson, Graham T. Reed, and Shawn S. H. Hsu

***Abstract*— In this letter, a 40-Gb/s optical modulator driver in 90-nm CMOS technology is presented. The design is based on the distributed amplifier (DA) topology with the proposed modified cascode stage to obtain high gain and large bandwidth, while also capable of protecting the MOS transistor under large output voltage swing. The modified cascode stage DA with enhanced high-voltage driving capability can reach an operating data rate up to 40 Gb/s with an differential output voltage swing of 4 V_{pp} (∼3-V eye amplitude), which can be used for driving 50-Ω silicon modulators.**

***Index Terms*— Cascode amplifier, distributed amplifier (DA), modulator driver, silicon photonics.**

I. Introduction

THE exponential growth of data communications over various networks is expected to continue in the near future. The high-speed fiber network plays an essential role in this roadmap. Compared with data transmission via the electrical wires, optical communication features the advantages of an improved bandwidth, smaller power consumption, reduced propagation delay, and immunity from electromagnetic interference [1]–[4].

The optical modulator is essential for high-speed fiber communication systems, because the direct modulation of laser has a limited bandwidth. Fig. 1 illustrates a typical optical communication system, where the modulator driver could be a bottleneck to limit the overall bandwidth for electrical-to-optical signal conversion. One challenge for modulator driver design is the output voltage swing. The $LiNbO_3$ modulator typically requires a driving voltage up to 5–7 V, and the driver is normally based on the III–V technology to take the advantage of the higher breakdown voltage of transistors [4]. The CMOS compatible silicon modulator has attracted a significant attention recently, which can operate at a relatively lower voltage of 4–5 V. Also, the silicon modulator has been reported to achieve a bandwidth up to 50 Gb/s and beyond based on a Mach–Zehnder interferometer [5]. The reduced operating voltage makes it possible to realize the driving circuit in CMOS technology, which is also preferred for the silicon photonics platform. However, the breakdown voltage is still an issue in CMOS devices.

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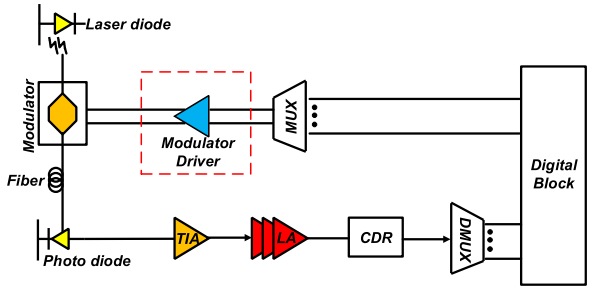


Fig. 1. Block diagram of a typical optical communication system.

In this letter, a 40-Gb/s 4-V_{pp} differential modulator driver fabricated in 90-nm CMOS is demonstrated. The proposed modulator driver employs the distributed amplifier (DA) topology with the modified cascode stages to achieve a large output swing, whilst preventing transistor breakdown. In addition, the characteristics of high gain and large bandwidth can be obtained simultaneously.

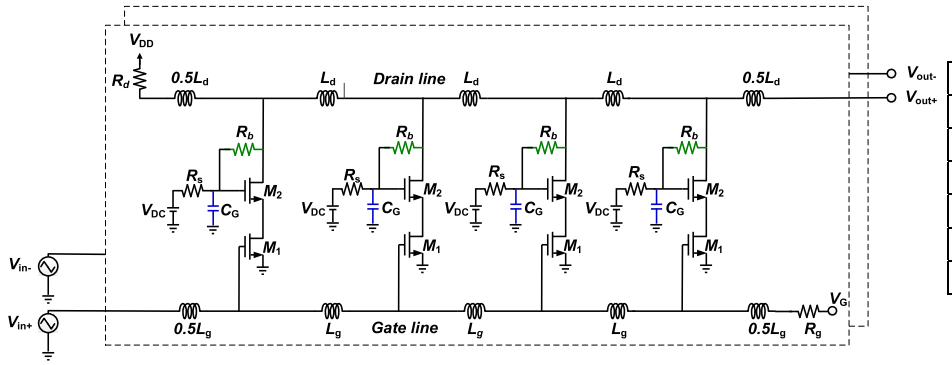
II. Circuit Design and Analysis

A. Distributed Amplifier

The DA is a well-known and widely used topology for various applications. Based on the principle of transmission line (TML), the intrinsic parasitic capacitances of the active devices combine with the external inductive components to form the artificial TMLs, and a wide bandwidth can be obtained [6]–[9]. Fig. 2 shows the proposed DA in a differential configuration. Spiral inductors are used to form the gate and drain lines. The top metal layer with a thickness of 3 μm is employed with the pattern ground for alleviated substrate effects and enhanced quality (Q) factors. The cascode topology is used as the unit stage, which features higher input and output isolation, improved power gain, and increased output swing compared with the common-source (CS) stage. Note that the transistor sizes and stage numbers need to be design properly for wide bandwidth and high gain. A higher power gain can be achieved by selecting larger transistor sizes. However, this also requires the gate and drain lines to have increased inductance for maintaining the characteristic impedance of the line. The increased inductance will have a lower self-resonant frequency, which could ultimately limit the circuit bandwidth. In this design, the sizes of the cascode transistors are designed as 32 (CS) and 55 μm [common-gate (CG)] with the four unit stages to achieve the desired bandwidth and gain. Also, both CS and CG transistors are the standard RF core device.

B. Modified Cascode Stage

As mentioned previously, the relatively low breakdown voltage of CMOS devices is the main limitation for the output



R_g	50 Ω
L_g	0.2 nH
C_G	0.6 pF
R_s	26 Ω
R_b	400 Ω
L_d	0.1 nH
R_d	50 Ω

Fig. 2. Circuit topology of the proposed four MCDA.

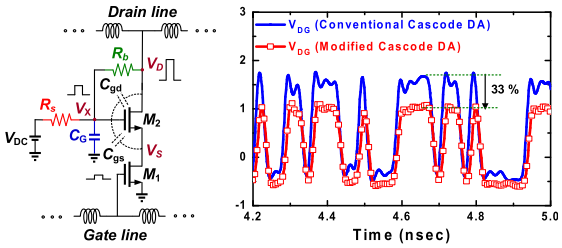


Fig. 3. (a) Modified cascode stage. (b) Comparison of voltage swing of conventional and modified cascode topologies.

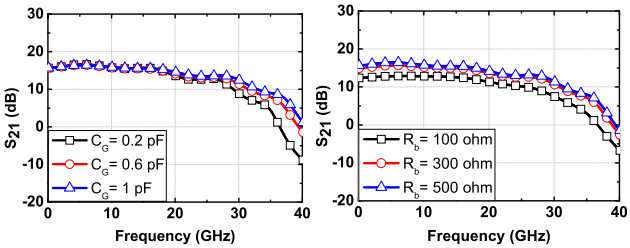


Fig. 4. Simulated S_{21} of the proposed DA as a function of (a) C_G and (b) R_b.

swing of the modulator driver. The supply voltage suggested by the foundry for the adopted 90-nm RF CMOS is 1.2 V (maximum up to ∼1.5 V) to avoid transistor breakdown and ensure long-term reliability. The cascode configuration is often used to enhance the output voltage swing [6], [7]. However, the gate bias of the CG stage is fixed in a typical cascode gain cell, and hence the transistor could encounter the breakdown situation if a large swing appears at the drain node of the cascode cell. We propose the modified cascode configuration to resolve the problem as shown in Fig. 3(a), where a metal–insulator–metal capacitor C_G is added between the gate of M_2 and ground [10], and two resistors R_s and R_b are employed as feedback. As the circuit operates at relatively low frequencies (assuming the capacitances can be neglected), the voltage of V_X can be determined by the voltage divider of R_s and R_b as shown in (1), which allows V_X to swing with the drain voltage V_D of M_2. As a result, the difference of the drain-gate voltage reduces to prevent M_2 breakdown. Similarly, V_X swings simultaneously with the AC signal at high frequencies because the capacitances including C_G, and the parasitic capacitances C_{gs} and C_{gd} start to play important roles. Based on small-signal analysis, V_X can be obtained using (2) at high frequencies

$$V_X = V_D \frac{R_s}{R_b + R_s} \tag{1}$$

$$V_X = V_D \frac{Z_G Z_{gs}}{Z_b Z_{gs} + Z_G Z_{gs} + Z_G Z_b} + V_S \frac{Z_b Z_G}{Z_b Z_{gs} + Z_G Z_{gs} + Z_G Z_b} \tag{2}$$

where $Z_G = R_s // C_G$, $Z_b = R_b // C_{gd}$, and $Z_{gs} = 1/j\omega C_{gs}$, and V_S is the source voltage of M_2. The calculated results of (1) and (2) agree very well with the small-signal model simulation based on the actual circuit parameters.

As shown in Fig. 3(b), the simulated results indicate that the drain–gate voltage V_{DG} of M_2 can be reduced by 33% compared with the conventional cascode stage for the same output swing of 2 V. However, the additional RC components may also degrade the bandwidth, and need to be designed carefully. Fig. 4(a) and (b) shows how the bandwidth and gain vary with C_G and R_b, respectively. Tradeoffs exist between gain bandwidth and transistors protection capability. For example, increasing C_G can enhance the bandwidth. However, the voltage at the gate will not vary with the drain voltage if C_G becomes too large, and the transistor becomes vulnerable. In practical design, C_G is chosen to limit the maximum V_{DG} of M_2 at around 1 V. As mentioned, the suggested V_{DD} is 1.2 V. With a typical gate bias of about 0.5 V, V_{DG} is only 0.7 V. Considering the signal swing of transistor, a 1-V limit should be reasonable for proper operation of the proposed circuit. In contrast, decreasing R_b can reduce the drain–gate voltage of M_2 to prevent transistors from breakdown but at the expense of lowered gain and degraded output matching. The values of circuit parameters in our final design are shown in Fig. 2.

III. Results and Discussion

A. Small-Signal Measurements

The proposed modulator driver using modified cascode stage DA (MCDA) was implemented in a 90-nm CMOS. The micrograph of the chip and the chip connected to the silicon modulator by bond wires are shown in Fig. 5(a) and (b), respectively. The differential S-parameters were measured by the four-port Keysight N5247A network analyzer, as shown in Fig. 5(c) (only two-port results are shown due to symmetry). The circuit was biased at $V_{DD} = 5$ V, $V_{DC} = 1.8$ V, and $V_G = 0.5$ V (see Fig. 2) with a total power consumption of 650 mW. Note that most of the V_{DD} voltage drops on R_d (3.25 V), and the actual dc voltages at the drain nodes of M_2 and M_1 are only 1.75 and 1.46 V, respectively. The driver

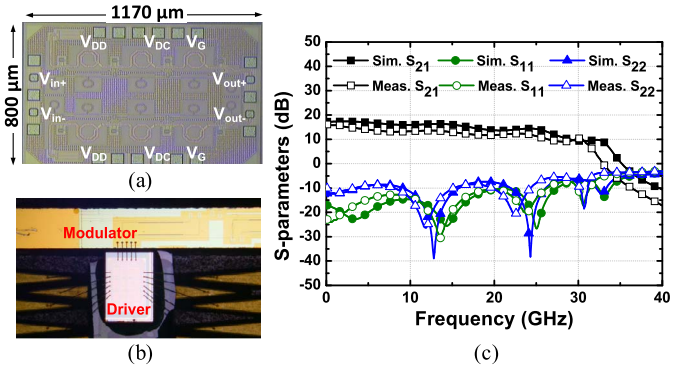


Fig. 5. (a) Chip micrograph of the proposed DA with modified cascode stage. (b) Photograph of DA and silicon modulator connected by bond wires. (c) Comparison of measured and simulated S-parameters of the modulator driver.

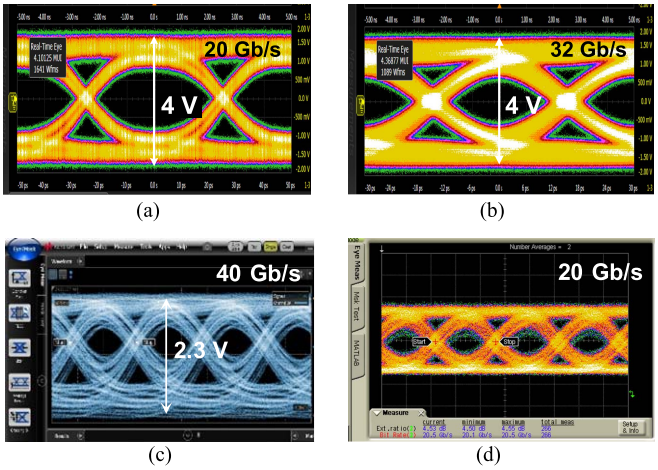


Fig. 6. Measured eye diagrams. (a) 20 and (b) 32 Gb/s of differential output. (c) 40 Gb/s single-ended output. (d) Optical eye diagram at 20 Gb/s.

TABLE I
COMPARISON OF PUBLISHED MODULATOR DRIVERS

Ref.	This work	[1]	[2]	[3]	[4]
Technology	90nm CMOS	45nm CMOS SOI	65nm CMOS	0.13µm CMOS	InP HBT
Data rate (Gb/s)	40	40	25	20	40
Gain (dB)	17	7.6	-	-	> 20
BW (GHz)	28.2	33	-	-	45
Out. swing (V)	4*/3$^+$	4.5*	3.3*	3.5*	2.4$^\#$
Power (mW)	650	437	480	900	1800
Area (mm^2)	0.936	0.38	0.029	0.72	2.81

$^\#$Single-ended signal; *differential signal; +eye amplitude.

achieves a high power gain of 17 dB and a 3-dB bandwidth of 28.2 GHz. The input and output reflection coefficients of the modulator driver remain below −10 dB within the bandwidth.

B. Large-Signal Measurements

The large-signal measurements were performed using the Keysight N4974A pattern generator and the Keysight DSOZ504A Infiniium real time oscilloscope. Note that the differential eye diagram was measured only up to 32 Gb/s limited by the equipment. We also manage to obtain the single-ended eye diagrams up to 40 Gb/s by the Anritsu MP1800A signal quality analyzer and the Keysight 86100D oscilloscope. Fig. 6(a) and (b) shows the measured electrical eye diagrams of the modulator driver with a differential output at 20 and 32 Gb/s, respectively. Fig. 6(c) shows the measured single-ended eye at 40 Gb/s. The measured differential voltage swing can reach up to 4 V_{pp} (about 3-V eye amplitude), whereas that for the single-ended eye can reach 2.3 V_{pp} including the cable loss. Note that the achieved eye amplitude is still sufficient for the recently reported high speed silicon modulators with a reduced operating voltage [11]. Fig. 6(d) shows the measured optical eye diagram up to 20 Gb/s. The reduced speed can be mainly attributed to the loss and impedance mismatch introduced by the bond wires at the OE interface. Table I shows the comparison with previous works. Compared with [1] using 45-nm silicon-on-insulator CMOS, the proposed circuit based on the DA topology has the advantage of a relatively flat gain over a wide bandwidth. Also, a high gain is achieved by a low cost 90-nm CMOS technology. On the other hand, the design in [1] using a single-stage stacked topology demonstrated a large output swing with a much smaller chip area and lower power consumption.

IV. CONCLUSION

The modulator driver proposed in this letter demonstrated high gain, large bandwidth, and excellent driving capability. With the proposed MCDA topology, the CG transistor in the cascode stage can be protected from damage under a large output swing. The operating frequency reached up to 40 Gb/s, and an output differential swing can reach 4 V_{pp} with an about 3-V eye amplitude.

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