An Ultra Compact Millimeter-Wave VCO in 3-D IC Technology

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***Abstract*—In this letter, an ultra compact three-dimensional (3–D) voltage-controlled oscillator (VCO) is presented. By utilizing the through silicon via (TSV) as inductors and variable bridge topology in the LC tank, the core area of VCO is reduced significantly with an improved tuning range. Implemented in a standard 90 nm CMOS process, the VCO consists of the top and bottom layers connected by TSVs using an in-house developed 3-D IC technology. The VCO is capable of operating at 43.3–43.9 GHz with a footprint of 0.0022 mm^3, and a core area of only 0.007 mm^2 which is about one to two orders of magnitude smaller than that in previous works. The measured phase noise is -90.8 dBc/Hz (1 MHz offset) at 43.3 GHz with an output power of -12.6 dBm. Under a supply voltage of 1.2 V, the VCO consumes a dc current of 15.4 mA.**

***Index Terms*—Millimeter wave, three dimensional (3-D), through silicon via (TSV), voltage-controlled oscillator (VCO).**

I. Introduction

SCALING of the device feature size in CMOS technology is approaching its physical limitation, and continuation of Moore's Law becomes even questionable. Also, the chip size keeps increasing to accommodate more circuit functions, which makes long interconnects the bottleneck for high speed operation. A promising solution to address this issue is the three-dimensional integrated circuit (3-D IC) technology, which attracts significant interests recently from both industry and academia. By stacking chips with through silicon vias (TSVs), the significant problem of global interconnect delay in traditional planar design can be resolved, and circuits with high operating speed and small form factors can be expected.

In addition, the 3-D IC/TSV technology can provide more flexibility for the design and integration of RF/microwave circuits. The TSVs exhibit inductive property at high frequencies, which can replace the conventional 2-D planar inductor for the LC tank in voltage-controlled oscillators (VCOs), and matching/ peaking in low-noise amplifiers (LNAs) or power amplifiers (PAs). With a proper arrangement/partition in both transistor and circuit levels at the beginning of design flow, the 3-D RF front-end with a miniature footprint is achievable. It is even possible to further integrate with other mixed-mode/baseband circuits, as long as the "co-design" approach is introduced in the early design stage.

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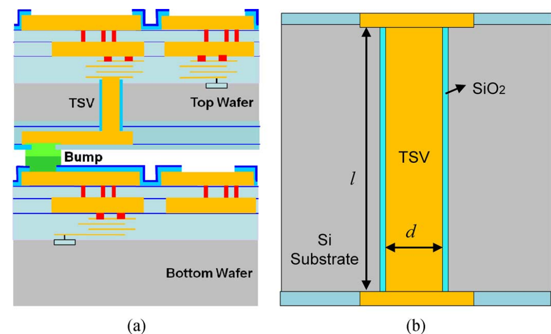

Fig. 1. (a) Cross section of face-to-back chip stacking, and (b) TSV structure and design parameters.

In this letter, we propose using the TSVs as a part of the LC tank to realize an ultra compact VCO in the millimeter-wave frequency range, which is an essential building block of the frequency synthesizer [1], [2]. Using the vertical TSVs to replace the planar spiral inductors, the 3-D VCO achieves a small footprint of only 0.0022 mm^3 (70 μm× 100 μm× 310 μm, not including bonding pads). Also, a TSV array consisting of four TSVs with one switching MOSFET in the LC tank forms variable inductance, which allows dual-band operation to improve the tuning range. By using the 3-D IC technology, the miniaturized VCO can operate at a center frequency of 43.6 GHz.

II. 3-D IC Technology and Design Considerations

Two types of stacking structures are used in typical 3-D IC technology including the face-to-face and face-to-back configurations. The former is a relatively simple solution, where the top die is flipped and mounted onto the bottom die directly. In the face-to-back structure adopted in this work, the upper wafer is thinned down first ($\sim 50\ \mu\mathrm{m}$), etched from the back side to form TSVs, placed on top of the bottom wafer, and then connected by bumps. Fig. 1(a) shows the cross section of face-to-back chip stacking, and Fig. 1(b) illustrates the detailed structure of a TSV, where d and l are the diameter and length of TSV, respectively. The TSV is made of copper and surrounded by a thin $\mathrm{SiO_2}$ layer for isolation. Different geometric parameters can directly contribute to equivalent inductance and quality factor (Q) of TSVs.

Fig. 2 presents the results using 3-D full wave EM simulation with various d and l. In Fig. 2(a), the inductance decreases as d increases, while Q increases with d (l is fixed at 50 μm). Fig. 2(b) shows that the inductance increases with l, but Q changes oppositely (d is fixed at 5 μm). With a narrower diameter and/or longer length, the TSV becomes more inductive but the parasitic resistance is also higher. As a result, the inductance increases but Q decreases. The dimensions of TSVs used in this design are with $l = 50\ \mu\mathrm{m}$ and $d = 5\ \mu\mathrm{m}$ (fixed in the process), which is corresponding to an inductance of $\sim 80-85$ pH with a quality factor

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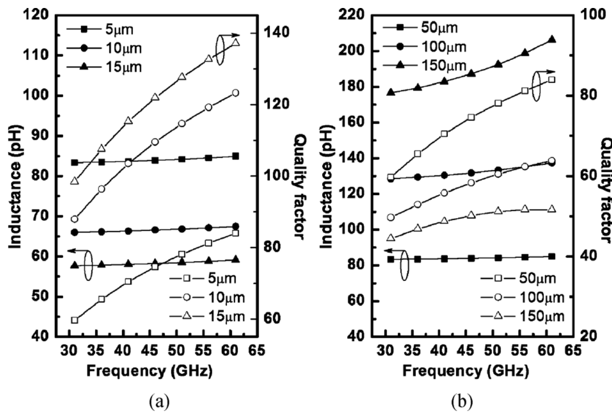

Fig. 2. 3-D full wave EM simulated results of TSVs with (a) different diameters (b) different lengths (solid dot: inductance; hollow dot: quality factor).

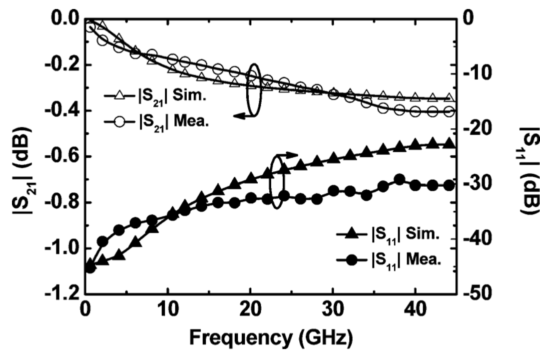

Fig. 3. Measured and EM simulated S-parameters of a single TSV.

of $\sim 70-80$ based on EM simulation. Although the inductance of a single TSV is fixed in this case, different inductances can be obtained by combining 2-D transmission lines with one TSV or multiple TSVs. The overall quality factor is still good enough with a much smaller size.

Different test structures were designed and fabricated to investigate the intrinsic TSV characteristics, and also to verify the EM simulation results. More details can be found in our previous work [3]. The fabricated TSV has $l = 53.8\ \mu\text{m}$ and $d = 4.63\ \mu\text{m}$ (based on SEM images) due to process variation. Fig. 3 shows the measured and simulated (size corrected) S-parameters of a single TSV. A good agreement is obtained between the results.

III. Circuit Topology and Analysis

Fig. 4 shows the circuit topology of the proposed 3-D VCO using TSVs. The circuit was fabricated in a 90 nm CMOS digital/mixed-signal process (without the ultra-thick metal UTM for RF), followed by an in-house developed 3-D IC technology with TSVs to connect the top and bottom wafers. The complementary cross-coupled pairs (M_1, M_2, M_3, and M_4), realized in the upper wafer, are employed to compensate the relatively large interconnect loss due to lack of the UTM and also to enhance the negative resistance for oscillation. The LC tank includes two accumulation-mode MOS varactors $C_{\rm V}$ in the top wafer, and also a TSV array with an NMOS switch M_5 in the bottom wafer.

Fig. 5(a) and (b) illustrate the proposed TSV array for variable inductance and the corresponding circuit model, respectively. The 3-D variable bridge design utilizes four TSVs with the nearby metal feeding lines and a MOS switch to accomplish

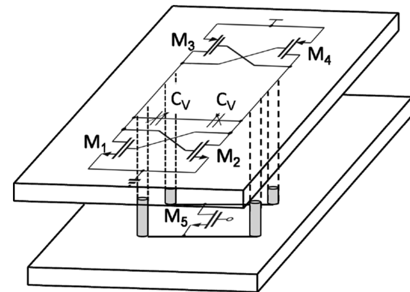

Fig. 4. Proposed circuit topology of the 3-D VCO.

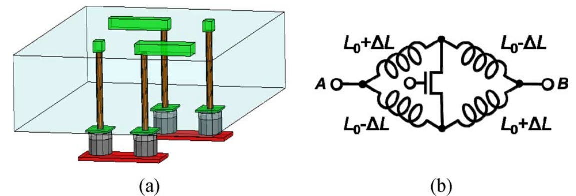

Fig. 5. (a) Proposed TSV array for variable bridge inductance and (b) the corresponding circuit model.

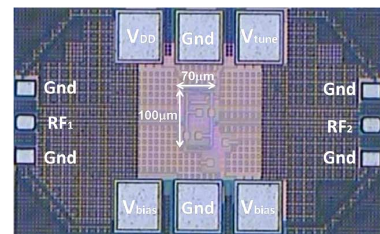

Fig. 6. Chip microphotograph of the proposed 3-D VCO using TSVs.

dual-band operation, as shown in Fig. 5(a). The configuration resembles the Wheatstone bridge, which was proposed in a 2-D VCO design [4]. As shown in Fig. 5(b), an NMOS switch is placed at the middle of the bridge. Also, an inductance offset exists among different signal paths. Compared with the typical variable inductance design using series inductors with a shunt MOS switch [5], the bridge topology can achieve a higher Q with an increased tuning range of the variable inductance. In the conventional design, the shunt MOS transistor must be large enough to reduce the parasitic resistances for maintaining a high Q when the switch is on, but which also introduces considerable parasitic capacitance resulting in decreased tuning range. In the bridge configuration, the MOSFET is not in the main signal path, thereby a smaller transistor size is allowed and a good quality factor can still be expected. Also, the tuning range will not suffer from the transistor parasitic capacitance.

Although with advantages, one obvious issue in practical implementation is a large chip area required if using four inductors in a 2-D design. In the proposed VCO, the four inductors in the bridge are designed by a TSV array, and the offset can be simply realized by the feeding lines. With a proper 3-D layout arrangement, the area of TSV array is as small as only $40 \times 40\ \mu\text{m}^2$, which is also about the total size of LC tank. When the MOS switch is off, the equivalent inductance from A to B is L_0. On the other hand, when the switch is on, the equivalent inductance of the bridge can be determined as [4]

$$L = (L_0 + \Delta L) \parallel (L_0 - \Delta L) + (L_0 + \Delta L) \parallel (L_0 - \Delta L) = \frac{{L_0}^2 - \Delta L^2}{L_0} \quad (1)$$

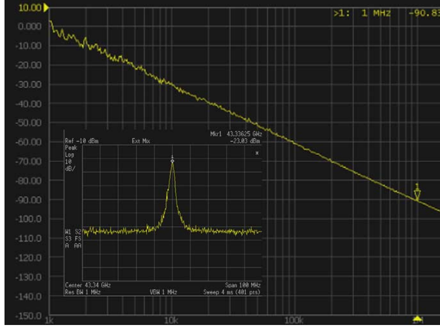

Fig. 7. Measured phase noise (1 MHz offset) and output spectrum ($f_0 = 43.3$ GHz) of the 3-D VCO.

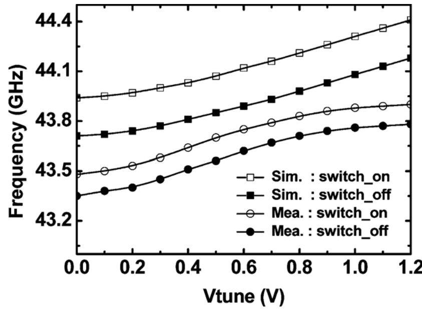

Fig. 8. Measured and simulated frequency tuning range of 3-D VCO.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

Ref.	[6]	[7]	[8]	This
Technology	130 nm CMOS	90 nm CMOS	130 nm CMOS	90 nm CMOS + 3D TSV
V_{DD} (V)	1.2	0.7	1.2	1.2
Frequency (GHz)	47	53.1–61.3	42.2	43.3–43.9
Tuning Range (%)	3.35	14.34	13.2	1.4
Phase Noise (dBc/Hz)	-95.4 (at 1 MHz)	-118.75 (at 10 MHz)	-94.6 (at 1 MHz)	-90.83 (at 1 MHz)
DC power (mW)	3.86	8.7	8	18.5
Chip area (mm^2) /Footprint (mm^3)	0.54^b/–	0.10^a/–	0.54^b/–	0.007^a/0.0022
FoM (dBc/Hz)	-182.9	-184.3	-183.5	-171

a: core area only; b: including pads and buffers.

which is reduced by $\Delta L^2/L_0$, compared to L_0. The simulated bridge inductances (based on corrected TSV geometry) varies from 77.2 to 80.9 pH (Q from 65.2 to 71.2). Note the parasitics introduced by the CMOS switch are considered in simulations, including both the transistors (RF model from the foundry) and the interconnects (EM simulation).

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed VCO was fabricated in a standard 90 nm CMOS 1P9M process, followed by an in-house developed 3-D TSV IC process. Fig. 6 shows the chip microphotograph. The overall chip area (both the top and bottom dies) is $0.61 \times 0.33\ \mathrm{mm}^2$ including the probing pads, and the core area is only 70 μm× 100 μm (0.007 mm^2). Fig. 7 shows the measured output spectrum and phase noise. Under a supply voltage of 1.2 V and bias current of 15.4 mA ($P_{\mathrm{DC}} = 18.5\ \mathrm{mW}$), the VCO is capable of operating at f_0 of 43.6 GHz. The measured phase noise is $-90.8\ \mathrm{dBc/Hz}$ at 43.3 GHz (1 MHz offset, switch off) with an output power of $-12.6\ \mathrm{dBm}$. Note a similar phase noise is observed when switch is on, since the transistor size is small with a negligible current ($\sim$ nA) flowing through in the bridge topology. With the TSV array and MOS switch, the VCO can achieve a dual-band operation and reach a tuning range from 43.3 to 43.9 GHz (1.4%), as shown in Fig. 8. Also, the simulated operating frequencies show a small discrepancy from the measured results.

Table I compares the proposed VCO with previously works [6]–[8]. The 3-D VCO has an figure-of-merit (FOM) of $-171\ \mathrm{dBc/Hz}$ [9]. It should be pointed out that a wider tuning range and lower phase noise can be expected from the 3-D VCO with high Q TSV inductance in the bridge topology. The CMOS digital process without UTM is responsible to the performance degradation of VCO. The parasitic resistance is relatively large resulting lower Q and hence increased phase noise. Also, the transistor sizes in the cross-coupled pairs need to be quite large to compensate the loss from the interconnects, which also introduce a considerable amount of parasitic capacitances and reduce the tuning range. Although interconnects with stacked metal layers can reduce the parasitic resistance, the parasitic capacitance increases accordingly. Based on EM simulation, using the stacked metal layers has a greater impact on limiting the operation frequency of VCO in this design.

V. CONCLUSION

An ultra-compact VCO in 3-D IC technology was demonstrated for millimeter-wave operation with a footprint of only $0.0022\ \mathrm{mm}^3$. Under a power consumption of 18.5 mW, the measured phase noise was $-90.8\ \mathrm{dBc/Hz}$ at 43.3 GHz (1 MHz offset) with a tuning range from 43.3 to 43.9 GHz. Taking advantage of the 3-D IC technology, the proposed VCO using a TSV array for variable inductance demonstrated a smallest core chip area compared with prior works as far as we know.

REFERENCES

[1] A. Scuderi and G. Palmisano, "A low-phase-noise voltage-controlled oscillator for 17 GHz applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 4, pp. 191–193, Apr. 2006.

[2] N. Zhang and K. K. O, "94 GHz voltage controlled oscillator with 5.8% tuning range in bulk CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 8, pp. 548–550, Aug. 2008.

[3] J. Wang *et al.*, "Testkey design of through silicon vias (TSVs) for accurate de-embedding and RF model parameters extraction," in *Proc. Int. Conf. Solid State Devices Mater.*, Sep. 2011, pp. 62–63.

[4] A. Tanabe, K. Hijioka, H. Nagase, and Y. Hayashi, "A novel variable inductor using a bridge circuit and its application to a 5–20 GHz tunable LC-VCO," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 883–893, Apr. 2011.

[5] P. Park, C. S. Kim, M. Y. Park, S. D. Kim, and H. K. Yu, "Variable inductance multilayer inductor with MOSFET switch control," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 144–146, Mar. 2004.

[6] N. Kim, Y. Oh, and J. Rieh, "A 47 GHz LC cross-coupled VCO employing high-Q island-gate varactor for phase noise reduction," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 2, pp. 94–96, Feb. 2010.

[7] C. Yu, W. Chen, C. Yu, and T. Lu, "A 60-GHz, 14% tuning range multiband VCO with a single variable inductor," in *IEEE A-SSCC Dig.*, Nov. 2008, pp. 129–132.

[8] C. Yang *et al.*, "A 20/40-GHz dual-band voltage-controlled frequency source in 0.13 μm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 8, pp. 2008–2016, Oct. 2011.

[9] S. Lee, Y. Chuang, S. Jang, and C. Chen, "Low-phase noise Hartley differential CMOS voltage controlled oscillator," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 2, pp. 145–147, Feb. 2007.