A Low-Power Miniature 20 Gb/s Passive/Active Hybrid Equalizer in 90 nm CMOS

Chi-Chou Lee, Ho-Chieh Hsieh, and Shawn S. H. Hsu, *Member, IEEE*

***Abstract*—In this letter, a compact and very low power passive/active hybrid equalizer is presented. By sharing the loading of high frequency peaking with the active equalizing stage, the passive filtering stage at the input can reduce the power consumption significantly. To achieve a small area while maintaining high performance, the 3-D inductor and active inductor techniques are also incorporated. Implemented in a standard 90 nm CMOS process, the proposed equalizer only consumes 10.8 mW and occupies a core chip area of 0.017 mm^2. The equalization function up to 22 Gb/s was successfully demonstrated with a gain of 10 dB at around 11 GHz for the data transmitted through a 180 cm coaxial cable line.**

***Index Terms*—3-D inductor, active inductor, CMOS, equalizer, low power, miniature.**

I. Introduction

As the data transmission speed keeps increasing up to the microwave frequency range, inter-symbol interference (ISI) becomes more severe. To overcome the impairment of data when transmitting through various channel conditions, different equalization methods have been proposed [1]–[4]. The passive equalizer composed of RLC components is widely used [5], [6] due to the nearly zero power consumption. However, it usually has small output swing and limited high frequency boost capability. Also, if the passive equalizer is to be implemented on chip, the area-consuming inductive components are a major issue. Another is the active type equalizer, which is capable of wideband operation with signal boosting at high frequencies [7]–[11]. This kind of equalizer often incorporates broadband design techniques such as inductive peaking and Cherry–Hooper topology. In addition, the resistive degeneration with variable capacitance is employed to provide tunable loss compensation. Compared with the passive filter design, the power consumption of active equalizer is the main consideration. However, the obvious advantage is the gain provided to the attenuated input signal and a relatively small chip area.

In this letter, we propose a hybrid type CMOS equalizer to exploit the advantages of both passive and active equalizers with the focus of low power and small area, while achieving high frequency operation. Fig. 1 shows the design concept of the proposed equalizer. The input signal is first enhanced by a passive equalizer with high-frequency boost capability, and followed by an active RC-degenerated equalizer to provide the tunable gain and further compensate the loss at high frequencies. A similar concept has been proposed [6] for a 10 Gb/s equalizer, but with a relatively large chip area and high power consumption. In this study, we introduce the 3-D inductors in the passive stage, and also the active inductors in the active stage to achieve a 20 Gb/s equalization capability. To the best of our knowledge, the high speed CMOS equalizer using 3-D inductors has not been reported. Also, our design demonstrates a significantly smaller chip area under very low power consumption compared with previous works. In addition to the adopted passive/active stage topology, the well-designed inductive components which allow a relatively simple active stage are of critical importance to circuit performance.

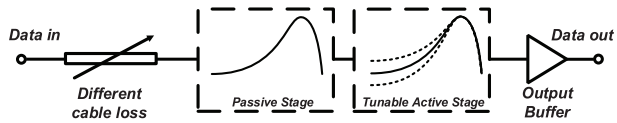


Fig. 1. Conceptual plot of the configuration of the proposed equalizer.

This letter is organized as follows. Section II presents the design and analysis of the proposed hybrid equalizer. Section III shows the measured results and comparison with prior works, and Section IV concludes this work.

II. Circuit Topology and Analysis

The proposed circuit topology is shown in Fig. 2. First, a passive filter is designed to equalize most of the attenuated signal from the cable line, and then the active equalizer can enhance the signal to the desired level. At last, an output buffer is essential for the 50 Ω measurement environment.

A. Passive Filtering Stage

Most high speed equalizers use on-chip passive inductors for effective gain boost at high frequencies [7], [8]. However, the conventional 2-D implementation in the CMOS process with only two metal layers occupies a large chip area. The 3-D inductor has been proposed [12], which utilizes all the metal layers available in the back-end process. Fig. 3(a) and (b) compare the chip layouts and frequency response of 3-D (with 9 metal layers) and 2-D (provided by foundry) inductors respectively realized in a standard 90 nm CMOS process. With a similar inductance at the desired frequency at around 11 GHz, the area of 3-D inductor is only 0.07 × of that compared with the 2-D counterpart. The quality factor of 3-D inductor is relatively small as expected due to the increased capacitive and resistive parasitics in the multi-layer structure. However, the low-Q nature is actually favorable for the wideband design such as the equalizer in this study.

The 3-D inductors L_{p} are used in the passive filtering stage of the equalizer, as emphasized in Fig. 2. Note L_{P} is connected to the gate of M_1 (M_2) of next stage, which makes the impact of

Manuscript received April 14, 2015; revised May 30, 2015; accepted June 11, 2015. Date of publication August 17, 2015; date of current version October 05, 2015. This work was supported by the National Science Council under Contract NSC 100-2628-E-007-030-MY3.

The authors are with the Department of Electrical Engineering, National Tsing Hua University, Hsinchu 300, Taiwan (e-mail: shhsu@ee.nthu.edu.tw).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LMWC.2015.2463224

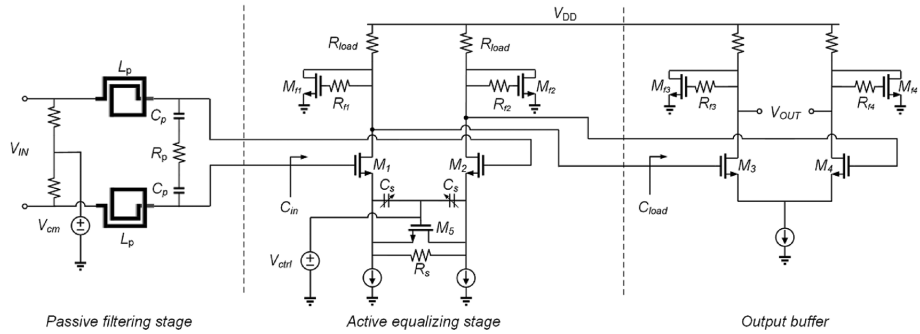


Fig. 2. Proposed hybrid equalizer with the passive filtering stage at the input, followed by an active equalizing stage, and an output buffer, where L_{P} are 3-D inductors.

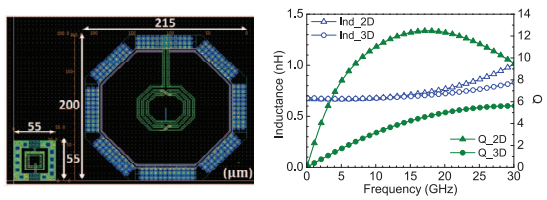


Fig. 3. Comparison of 3-D and 2-D inductors in terms of (a) area and (b) frequency response.

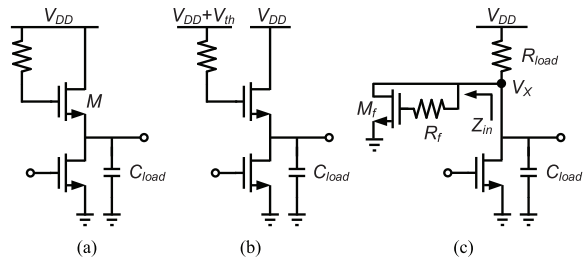


Fig. 4. Comparison of different active inductors (a) conventional (b) boosted voltage bias (c) folded topology.

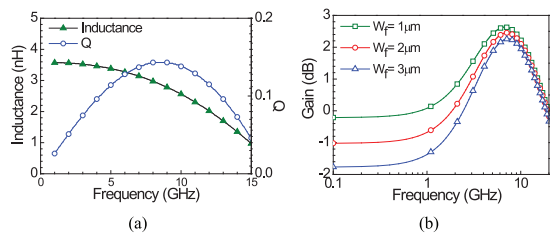


Fig. 5. (a)Inductance and Q of the active inductor (b) Gain of the active equalizing stage as a function of the transistor width W (M_{f1} and M_{f2}).

parasitic resistance of the 3-D inductor on the dc gain relatively small. The inductor L_{p} and capacitor C_{p} are chosen based on the desired peaking frequency ($\sim$ 10 GHz). With a fixed resonant frequency, L_{p} is designed as 0.67 nH (optimized based on the area of 3-D structure), and C_{p} is determined as 0.2 pF. It should be mentioned that the solenoid-type 3-D design was adopted instead of the stacked 3-D inductor. The parasitic capacitances of each layer are connected in series, resulting in a smaller equivalent capacitance [12]. The simulated result shows a self-resonant frequency of $\sim$ 53 GHz for L_{p}, which is much higher than the desired operation frequency range. The resistor R_{p} of 22 Ω is designed to obtain a sufficient peaking gain, and also for controlling the ascent of peaking profile (optimized together with the active stage). With proper design of the reactance and resistance components, the voltage across the equivalent output reactance can be much larger than V_{in} at around the resonant frequency. In other words, this circuit has a voltage gain. In addition to provide signal peaking at high frequencies, the increased voltage swing is also beneficial for converting the signal to current type in the following transconductance stage (M_1 and M_2) at the input of active equalizing stage.

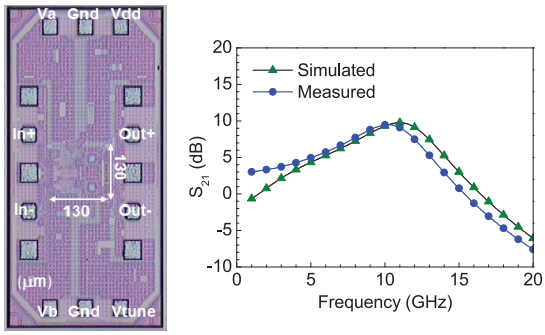
B. Active Equalizing Stage

To further enhance the signal quality after the passive filter stage, an active equalizer is used at the second stage. It should be emphasized that the passive filter effectively relieves the loading of the active stage regarding both the peaking gain and operating bandwidth. Compared with previously reported works using either multi-gain stages [7], [8] or other more complicated/power-consuming broadband techniques [9], we achieve a total 10 dB peaking gain with only a single active gain stage. Note that the buffer stage was designed to have negligible gain but with a bandwidth up to 11 GHz.

As shown in Fig. 2, the active equalizing stage uses the source resistive degeneration, where R_{s} and C_{s} can produce a zero for gain peaking, and the folded active inductor provides further boosting. Compared with the passive 3-D inductor, the active inductor occupies an even smaller chip area. Fig. 4 compares three different configurations of active inductors [13], [14]. The conventional active inductor as shown in Fig. 4(a) suffers from a large voltage drop, and a relative large V_{DD} is needed. One improved version is shown in Fig. 4(b). The separated supply voltage for the gate of active inductor can relax the required V_{DD} for the main current path. Fig. 4(c) shows the folded active inductor adopted in this design. The parallelly connected active inductor with R_{load} can effectively reduce V_{DD} for a low power design. Fig. 5(a) shows the inductance and quality factor of Z_{in} as a function of frequency. Fig. 5(b) illustrates how the frequency response varies with W_{f} (total width of M_{f}) in the active equalizing stage, which mainly determines the low frequency gain. Although not shown here, the resistance of R_{f} dominates the high frequency gain peaking. In the final design, W_{f} (M_{f1} and M_{f2}) and R_{f} (R_{f1} and R_{f2}) are 1 μm and 3 kΩ, respectively. It should be mentioned that Z_{in} remains inductive in the desired output swing range for the equalizer. The simulated results show a small variation of inductance when V_{x} changes from 0.7 to 0.9 V.

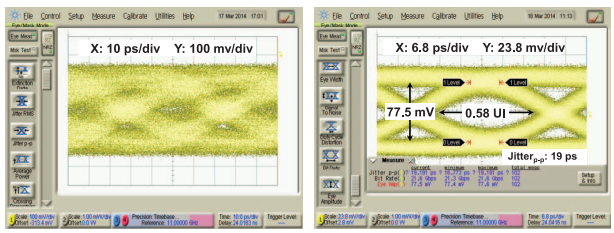
III. Experimental Results and Discussion

Fig. 6(a) shows the chip micrograph of the proposed hybrid equalizer fabricated in 90 nm CMOS technology with a core area of only 0.017 mm^2 (total area is 0.36 mm^2). Fig. 6(b) compares the simulated and measured S_{21} of the equalizer.



(a) (b)

Fig. 6. (a) Chip micrograph of the proposed equalizer. (b) S_{21} of the equalizer.



(a) (b)

Fig. 7. Measured eye diagrams via a 180 cm coaxial cable (a) before (b) after equalization.

TABLE I
PERFORMANCE AND COMPARISON WITH PRIOR WORKS.

Ref.	This work	2007 [6]	2005 [9]	2010 [10]	2014 [15]
Tech. CMOS	90 nm	180 nm	110 nm	90 nm	45 nm
Data rate (Gb/s)	22	10	10	20	32
Peaking gain (dB)	9.4@11	16.7@5	20@5	24@10	18@16
Jitter_{p-p} (ps)	19	< 50	27.8	32	17.5
Eye opening (UI)	0.58	> 0.5	0.72	0.36	0.44
Core area (mm^2)	0.017	1.1	0.004*	0.09	0.068
V_{DD} (V)	1.2	1.8	1.2	1	0.73
Power (mW)	10.8	34.2	13.2	40	9.3
FoM (Gb·dB/mW)	19.1	4.9	15.2	12	61.9

*Without using inductors

The measurement setup for eye diagram includes an Agilent N4974A pattern generator and a high speed Agilent 86100C sampling scope. Since the measurement setup is limited from 22 to 40 Gb/s, the lowest data rate 22 Gb/s was used to verify the proposed equalizer for the design target at 20 Gb/s. The measured eye diagrams before and after equalization at 22 Gb/s when signal (PRBS of $2^{31} - 1$) passed through a 180 cm coaxial cable (loss of $\sim$ 11.5 dB at 11 GHz) are shown in Fig. 7. The signal is successfully reconstructed and the maximum peak-to-peak jitter is about 19 ps. The circuit performance is summarized in Table I with the comparison of previously published equalizers. Note that a 32 Gb/s equalizer was demonstrated in 45 nm CMOS with a power consumption of only 9.3 mW and a core area of 0.068 mm^2 [15]. In contrast, our work also achieves a very low power of 10.8 mW with a miniature chip area of only 0.017 mm^2 simultaneously.

In this design, we targeted at an operation speed of 20 Gb/s and tried to reduce the chip area and power consumption by the 3-D and active inductors. On the other hand, one can also focus on achieving a high operation speed without considering the tradeoff of the power and chip area. Compared with [6], this design demonstrated a higher operation speed with much lower power consumption and much smaller chip area. The main contributor should be the well-designed inductive components, including the passive and active ones. The other reason should be the relatively simple design of the active stage. With the help of the active inductor for gain peaking, a wider bandwidth can be achieved with very low power consumption. If taking into consideration the advantage of technology for FoM calculation (assuming f_T is doubled), the proposed equalizer still shows much improved performance compared with [6].

IV. CONCLUSION

A low-power and high speed hybrid equalizer with a very small chip area was demonstrated in a 90 nm CMOS technology. Using a passive filtering stage at the input, the loading for the desired overall equalization was much relieved for the succeeding active stage. Also, the 3-D inductors employed in the passive stage significantly reduced the chip area, and the parallel active inductor in the active stage successfully enhanced the signal quality with small power consumption and area. Under a power dissipation of 10.8 mW, this miniature hybrid equalizer with a core area of only 0.017 mm^2 is capable of transmitting 22 Gb/s data through 180 cm coaxial cable line.

REFERENCES

[1] Y. Shim, W. Lee, E. Song, J. Cho, and J. Kim, "A compact and wide-band passive equalizer design using a stub with defected ground structure for high speed data transmission," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 5, pp. 256–258, May 2010.

[2] C. Y. Hsiao and T. L. Wu, "A novel dual-function circuit combining high-speed differential equalizer and common-mode filter with an additional zero," *IEEE Microw. Wireless Compon. Lett.*, no. 99, pp. 1–3, Jun. 2014.

[3] E. Song, J. Cho, W. Lee, M. Shin, and J. Kim, "A wide-band passive equalizer design on PCB based on near-end crosstalk and reflections for 12.5 Gbps serial data transmission," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 12, pp. 794–796, Dec. 2008.

[4] S. C. Bera, "Amplitude tilt active equalizer for frequency and temperature compensation," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 7, pp. 344–346, Jul. 2011.

[5] R. Sun *et al.*, "A tunable passive filter for low-power high-speed equalizers," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2006, p. 198.

[6] J. H. Lu, C. L. Luo, and S. I. Liu, "A passive filter for 10 Gb/s analog equalizer in 0.18-μm CMOS technology," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2007, pp. 404–407.

[7] S. Gondi and B. Razavi, "Equalization and clock and data recovery techniques for 10 Gb/s CMOS serial-link receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1999–2011, Sep. 2007.

[8] J. Lee, "A 20 Gb/s adaptive equalizer in 0.13-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2058–2066, Sep. 2006.

[9] Y. Tomita *et al.*, "A 10 Gb/s receiver with series equalizer and on-chip ISI monitor in 0.11-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 986–993, Apr. 2005.

[10] S. A. Ibrahim and B. Razavi, "A 20 Gb/s 40 mW equalizer in 90 nm CMOS technology," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 170–171.

[11] M. S. Kao *et al.*, "A 10 Gb/s CML I/O circuit for backplane interconnection in 0.18 μm CMOS technology," *IEEE Trans. VLSI*, vol. 17, no. 5, pp. 688–696, May 2009.

[12] C. C. Tang *et al.*, "Miniature 3-D inductors in standard CMOS process," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 471–480, Apr. 2002.

[13] S. Hara *et al.*, "Broad-band monolithic microwave active inductor and its application to miniaturized wide-band amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 36, no. 12, pp. 1920–1924, Dec. 1988.

[14] J. Chen, F. Saibi, J. Lin, and K. Azadet, "Electrical backplane equalization using programmable analog zeros and folded active inductors," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 7, pp. 1459–1466, Jul. 2007.

[15] A. Manian and B. Razavi, "A 32 Gb/s 9.3-mW CMOS equalizer with 0.73-V supply," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2014, pp. 1–4.