A 17.5–26 GHz Low-Noise Amplifier With Over 8 kV ESD Protection in 65 nm CMOS

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***Abstract*—By the electrostatic discharge (ESD)/matching co-design methodology, a wideband low-noise amplifier (LNA) using a grounded spiral inductor in conjunction with a MOM capacitor for ESD protection and wideband matching is demonstrated in a 65 nm CMOS. The shunt inductor provides an effective bidirectional ESD protection to the ground and the series capacitor greatly enhances the breakdown level in the current discharge path. The measurement results demonstrate an over 8 kV human-body-model ESD protection level with almost no RF characteristic degradation after ESD zapping. Under a power consumption of 5.6 mW, the ESD-protected LNA presents a flat NF and power gain of 3.3–3.9 dB and 16.6–17.9 dB, respectively, in the frequency range of 18.5–24.5 GHz, and a 3 dB bandwidth of 17.5–26 GHz is achieved.**

***Index Terms*—CMOS, electrostatic discharge, human-body-model (HBM), low-noise amplifier (LNA), radio frequency (RF).**

I. Introduction

With rapid feature size scaling in CMOS technology, the improved device performance is beneficial to RF integrated circuits for portable and wireless applications. However, the reduced gate oxide thickness and hence lowered breakdown voltage also increase the difficulties of on-wafer electrostatic discharge (ESD) protection design. The ESD protection blocks are often incorporated with the RF low-noise amplifier (LNA), since the LNA is usually connected to the external components directly. The diode-based or SCR-based ESD protection techniques are limited by the capacitive parasitics for high frequency applications, and also limited by the on resistance for achieving a high ESD protection level [1], [2].

The ESD design using inductive cancellation was first proposed in 2001 [3]. Recently, the ESD protection techniques involving inductive components have received increasing attention [4]–[6]. An ESD protection scheme with plug-and-play inductor was proposed to tune out the parasitic capacitance at 5 GHz [4]. Using the similar concept of [3] and [4], a multilayer coplanar waveguide (MCPW) inductor $L_{\rm ESD}$ for grounding the ESD current was designed to tune out the pad capacitance at f_0 [5]. A series $L_{\rm ESD}$ connected to the ESD diode provided high impedance, functioning as an RF choke to minimize impact of diode parasitic capacitances on the core circuit [6].

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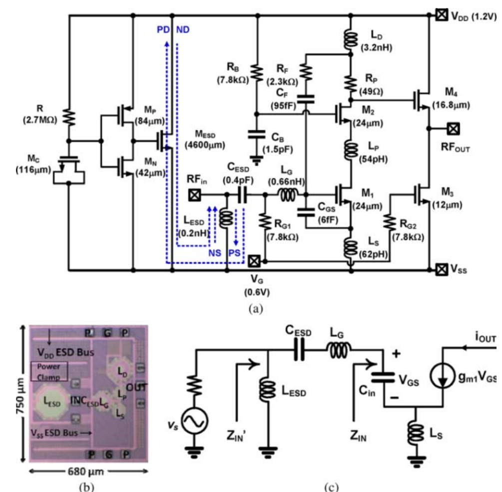

Fig. 1. (a) Schematic of the ESD-protected LNA, also indicating discharge paths of different ESD test modes, (b) chip micrograph, and (c) small-signal equivalent circuit model of the input stage.

In this study, we propose a rather simple design approach utilizing a grounded spiral inductor and a metal-oxide-metal (MOM) capacitor in conjunction with the power clamp to achieve a robust ESD network for wideband LNA design. The shunt inductor connected to the ground is used to bypass the ESD current directly [3]–[5], and also for tuning out the parasitic input capacitances. However, a relatively large $L_{\rm ESD}$ is required without combining $L_{\rm ESD}$ with other matching components. In contrast, $L_{\rm ESD}$ in this study functions together with $C_{\rm ESD}, L_{\rm S}, L_{\rm G}, C_{\rm GS}$ (see Fig. 1), and the transistor parasitic capacitances to form a multi-stage matching network, which relaxes the limitation of the parasitics on bandwidth in typical RF ESD design using the plug-and-play approach. Only a small inductance of $\sim$0.2 nH is needed. Although the ESD protection scheme looks similar to those in [3]–[5], the co-design concept with the entire input matching for achieving wide bandwidth and low noise was not mentioned before. Also, the importance of $C_{\rm ESD}$ to the ESD protection level was not pointed out, as will be discussed later. This design focuses on achieving a wideband LNA to cover the full K-band with a robust ESD protection using advanced 65 nm CMOS technology with a very thin oxide layer ($\sim$ 20 Å). This work reports the highest ESD protection level in 65 nm CMOS LNA and achieves figure-of-merits among the best compared with prior arts.

II. Circuit Design

Fig. 1(a) and (b) show the LNA topology and the corresponding chip micrograph, respectively. The design parameters are also shown in Fig. 1(a). Fig. 1(c) is the corresponding small-signal equivalent circuit model of the input stage. The

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LNA employs a cascode topology (M_1 and M_2) with a source degeneration inductor $L_{\rm S}$, which has the advantages of high gain, reduced Miller effects, and improved input/output isolation. For wideband design, the RC feedback consisted of $R_{\rm F}$ and $C_{\rm F}$ and a peaking inductor $L_{\rm P}$ are used. Also, a small resistance $R_{\rm P}$ is utilized for low-Q resonant network to extend the bandwidth [7]. The inductor $L_{\rm D}$ works as the inductive peaking and also matching to the source follower buffer stage M_4 (biased by M_3) for 50 Ω testing environment. The input matching network includes the shunt inductor $L_{\rm ESD}$ (also for ESD device), metal-oxide-metal (MOM) capacitor $C_{\rm ESD}$ (also for ESD device), gate inductor $L_{\rm G}$, source inductor $L_{\rm S}$, and a MOM capacitor $C_{\rm GS}$. A flat S_{21} can be achieved over a wide bandwidth with low input/output reflection coefficients, which almost covers the full K-band (18–26.5 GHz) in this design. The capacitor $C_{\rm GS}$ is used for achieving power-constrained simultaneous noise and input matching (PCSNIM) [8], which allows a small transistor size but with a 50 Ω real part of the input impedance and hence reduced power consumption [9]. Impedance of the input stage

$$Z_{IN} = \frac{g_{m1}L_S}{C_{in}} + j\left[\omega L_S - \frac{1}{\omega C_{in}}\right] \quad (1)$$

$$Z'_{IN} = (j\omega L_{ESD})//\left(\frac{1}{j\omega C_{ESD}} + j\omega L_G + Z_{IN}\right). \quad (2)$$

Using the "co-design" approach, the $L_{\rm ESD}$ and $C_{\rm ESD}$ are combined with $L_{\rm G}, C_{\rm in}$ (the equivalent input capacitance at the gate of $\rm M_1$), and $L_{\rm S}$ to have $\mathrm{Re}(Z'_{\rm IN})$ as 50 Ω, and $\mathrm{Im}(Z'_{\rm IN})$ to be zero. The feedback resistor R_F (2.3 kΩ), much larger than 50 Ω, can be neglected for simplicity. In practical design, the sizes of M_1 and M_2, and the value of g_{m1} (transconductance of M_1) are determined first with the considerations of power dissipation, gain, and noise characteristics. The inductor $L_{\rm ESD}$ is the most critical component for ESD protection level, which is then determined in the design flow. Finally, $C_{\rm ESD}$ are co-designed with $L_{\rm G}$, $L_{\rm S}$, and $C_{\rm GS}$ to achieve noise and power matching.

The ESD network in this design is rather straightforward, including a grounded shunt inductor $L_{\rm ESD}$ with a high current capability and a series capacitor $C_{\rm ESD}$ with a high breakdown voltage, and a $V_{\rm DD}$-to-$V_{\rm SS}$ power clamp. The shunt $L_{\rm ESD}$ provides a low-impedance bi-directional path to the ground for ESD discharge current. The capacitor $C_{\rm ESD}$ can be viewed as a substitute of the gate capacitance of M_1, which raises the upper bound of ESD design window significantly since the breakdown voltage of the MOM capacitor is up to ∼75 V. As the ESD zapping occurs, the relatively low frequency ESD current will be blocked by the high impedance $C_{\rm ESD}$ and be conducted to the ground through $L_{\rm ESD}$. Note that the $L_{\rm ESD}$ and $C_{\rm ESD}$, as a part of the input matching network, function as typical passive elements for RF signal under normal operation. Compared with adding a relatively large inductor by the plug-and-play method [4], the $L_{\rm ESD}$ here is co-designed with the input matching network, which takes the ESD design into consideration in the early RF design stage. This approach allows the optimization of RF performance and ESD protection simultaneously and the value of $L_{\rm ESD}$ is reduced substantially. As for the concern of ESD time constants, since both $L_{\rm ESD}$ (0.2 nH) and $C_{\rm ESD}$ (0.4 pF) are very small by using the co-design approach, $L_{\rm ESD}$ and $C_{\rm ESD}$ act like short and open circuits respectively to the ESD zap (the upper frequency ranges of human-body-model (HBM) and Machine Model (MM) are ∼10 and 16 MHz, respectively).

The power clamp provides a low-impedance path from $V_{\rm DD}$ to ground, which also completes the ESD paths for the PD and ND modes. The multi-metal routing (from $\rm M_1$ to $\rm M_6$) is employed to reduce IR drop and prevent the electron-migration induced burn out. The overall metal width for anode/cathode interconnection is larger than 30 μm to sustain the high ESD current. To prevent a large ESD discharge current through the vias causing electro-migration (EM), a half-turn spiral inductor using only the thick top metal layer (M6) with a width of 10 μm is adopted. With a large enough width of $L_{\rm ESD}$ and relatively short length using the co-design approach, the voltage drop on the current path via $L_{\rm ESD}$ becomes very small and an excellent ESD protection level can be achieved. Note that the selection of $L_{\rm ESD}$ $(\mathrm{Radius} = 75\,\mu\mathrm{m}, \mathrm{Q_{peak}} = 22.5, \text{and area} \sim 0.04\,\mathrm{mm}^2)$ is based on the design environment provided by the foundry, including PDK and RLC extraction flow, to speed up the design process. The chip area could be further reduced if a customized inductor layout is employed.

III. Measured Results and Discussion

The ESD-protected LNA was fabricated using a 65 nm CMOS process with a total chip area of 0.51 mm^2 including the probing pads. The RF and ESD characteristics were both measured on-wafer. The ESD tests were performed by both HANWA HED-W5100D ESD tester and Barth 4002 TLP test system, both with a pulse of a 10 ns rise time and 100 ns width to simulate HBM. The MM ESD test has also been performed by HANWA HED-W5100D. In typical ESD test, the leakage current is monitored as the failure criteria. Compared with the conventional design using ESD devices such as diode, GGNMOS, or SCR, the leakage current of $L_{\rm ESD}$ and $C_{\rm ESD}$ in this study is difficult to be monitored directly. Alternatively, the leakage check can be performed at the $V_{\rm DD}$ node [4] and also confirmed with the RF characteristic degradation such as gain and noise figure after ESD stress.

Fig. 2 shows the measured small-signal power gain, input/output return losses, and NF of the ESD-protected LNA under a 1.2 V supply with an associated drain current of 4.7 mA. The LNA achieves a 3 dB bandwidth from 17.5 to 26 GHz (the bandwidth specified under a 10 dB return loss is from 18.5 to 24 GHz) and a peak gain of 17.9 dB, and the input and output return losses are greater than 6 and 13 dB, respectively, within the 3 dB bandwidth. The gain variation is only 1.3 dB (16.6 to 17.9 dB) from 18.5 to 24.5 GHz. The LNA presents a flat NF of 3.3 to 3.9 dB in the frequency range from 18.5 to 24.5 GHz. Also, the measured S-parameters and NF before and after ±8 kV (measurement limitation) HBM ESD zap are almost identical ($|\mathrm{S}_{21}|$ degradation $<$0.8 dB and NF degradation $<$0.3 dB within $f_{3\ \mathrm{dB}}$), indicating the ESD current has been successfully bypassed via $L_{\rm ESD}$ to the ground or $V_{\rm DD}$ without damaging the core circuit. It should be mentioned that the simulated results indicate that $L_{\rm ESD}$ and $C_{\rm ESD}$ can effectively increase the bandwidth of LNA, while maintaining a similar peak gain, compared to the optimized design without $L_{\rm ESD}$ and $C_{\rm ESD}$. The main penalty comes from a slightly increased noise figure (∼0.1–0.2 dB) due to the additional LC components.

Fig. 3 shows the TLP characteristics of the four HBM testing modes of the LNA. All the cases present a second breakdown

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED K-BAND LNAS WITH PRIOR ARTS

Ref.	Tech. (nm)	Freq. (GHz)	S_{21} (dB)	NF (dB)	S_{11} (dB)	S_{22} (dB)	Power (mW)	P_{1dB} (dBm)	IIP3 (dBm)	ESD (kV)	FOM[1]	FOM[2]
This work	65 CMOS	17.5 – 26	17.9	3.3 – 5.9	< -6	< -13	5.6	-15	-5	> 8	3.3	26.5
[10]	90 CMOS	1.6 – 28	10.7	2.92 – 4.4	< -10	--	21.6	-9	4	--	10.9	--
[11]	90 CMOS	18 – 26	16.2	2.5 – 4	< -4	< -3	26.4	--	-	--	--	--
[12]	180 CMOS	21 – 27	10.6	4.9 – 6.1	< -13	< -8.2	27	-14	-4	--	0.1	--
[13]	350 SiGe	22.2 – 26	13.1	3.1 – 3.3	< -5.4	< -10.6	41	-8.7	-1.8	1.5	0.2	0.24

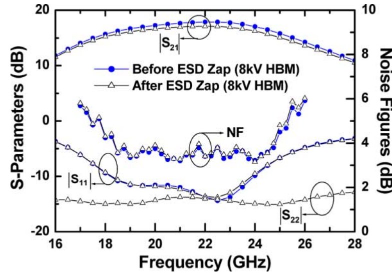

Fig. 2. Measured S_{11}, S_{21}, S_{22}, and NF of the ESD-protected wideband LNA before and after 8 kV HBM ESD zapping.

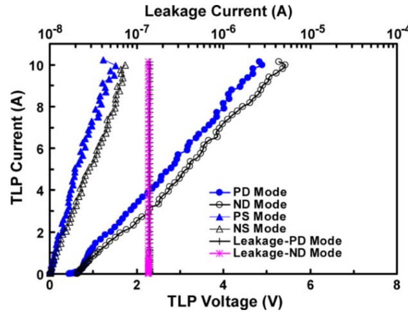

Fig. 3. Measured TLP $I-V$ characteristics of ESD-protected wideband LNA.

current It_2 over 10 A, corresponding to an ESD level over 15 kV $(V_{\rm ESD} \sim It_2 \cdot 1.5{\rm k}\Omega)$ [2]. Note that in the PS and NS modes, the ESD network behaves like a short circuit due to $L_{\rm ESD}$ and the TLP current is conducted to the ground directly. Since the leakage current cannot be monitored across $L_{\rm ESD}$, the ESD protection level is verified by the HANWA ESD tester together with the RF characteristics before and after 8 kV HBM ESD zapping, as shown in Fig. 2. For the PD and ND modes, the measured leakage currents are also shown in Fig. 3 (mainly from the power clamp). The extremely small and unchanged leakage current $(\sim 0.14\ \mu{\rm A})$ up to 10 A indicates that the proposed ESD protection design is very effective. The MM tests by HANWA HED-W5100D also demonstrate the LNA can pass over ± 700 V for the PD and ND modes and ± 1000 V for the PS and NS modes. It should be pointed out that $L_{\rm ESD}$ plays a major role in the ESD protection by short circuiting the ESD discharge current to the ground, as can be seen from the relatively small TLP voltage (<6 V) in different stress modes. However, $C_{\rm ESD}$ is still very important to the overall ESD protection robustness, especially when the chip size increases with long metal routing and in more advanced technology node with even smaller breakdown voltage. Without measurements, it is difficult to predict the actual ESD protection level. Therefore, it is preferred to push the upper limit of the ESD level in practical design to prevent device latent damages during ESD events.

Table I [10]–[13] compares this work with published wideband LNAs operating at K-band, where ${\rm FOM}^1$ and ${\rm FOM}^2$ (modified from [4]) are as follows:

$$FOM^1 = \frac{Gain[abs] \times IIP3[mW] \times BW_{3\ {\rm dB}}[GHz]}{(NF-1)[abs] \times P_{DC}[mW]} \quad (3)$$

$$FOM^2 = \frac{Gain[abs] \times IIP3[mW] \times BW_{3\ {\rm dB}}[GHz] \times ESD[kV]}{(NF-1)[abs] \times P_{DC}[mW]}. \quad (4)$$

With low noise, high gain, low power consumption, and high ESD protection level, the proposed LNA achieves FOMs among the best compared with prior works.

IV. CONCLUSION

An ESD-protected LNA was realized in 65 nm CMOS technology using grounded shunt inductor with high current capability and a series MOM capacitor with high breakdown voltage for ESD protection and input matching simultaneously. Under power consumption of 5.6 mW, the LNA presented excellent wideband and low noise characteristics. The minimum NF was only 3.3 dB and below 3.9 dB from 18.5 to 24.5 GHz. The peak power gain was 17.9 dB and the 3 dB bandwidth was from 17.5 to 26 GHz. LNA can pass 8 kV ESD stress, verified by RF performance measurements before and after 8 kV HBM ESD zap.

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