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A V-BAND LOW-NOISE AMPLIFIER CO-DESIGNED WITH ESD NETWORK IN 65-nm RF CMOS

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ABSTRACT: *A V-band low-noise amplifier (LNA) with electrostatic discharge (ESD) protection using RF junction varactors is demonstrated in a 65-nm CMOS technology. The gate-source junction varactor is used to achieve a power-constrained simultaneous noise and input matching, and also as an auxiliary ESD protection for the NS and ND modes. The measured results shows an over 2.0-kV ESD protection in the PD and PS modes, whereas the ESD level is enhanced up to 4.0 kV in the NS and ND modes. Under a power consumption of only 14.1 mW, the LNA demonstrates a noise figure (NF) of 5.2 dB and a peak power gain of 10.9 dB at 51 GHz, only a 0.8-dB degradation for both NF and power gain compared with the reference design (LNA without ESD protection).*
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Key words: *CMOS; electrostatic discharge; low-noise amplifier; V-band*

1. INTRODUCTION

The CMOS technology with rapid feature size scaling demonstrates integrated circuits capable of high speed and low power applications. Studies have been reported recently by using advanced CMOS technology to realize receiver circuits for high data rate wireless communications [1–3]. As the first stage of an RF receiver, the low-noise amplifier (LNA) is exposed directly under the risk of electrostatic discharge (ESD), and hence it is essential to provide ESD protection at the RF input pin of the LNA. Design of ESD network becomes a more challenging task in advanced CMOS technology with the reduced gate oxide thickness and lowered breakdown voltage. The increased operation frequency also makes the noise figure (NF) and gain of the LNA more sensitive to the parasitics introduced by the ESD protection devices [3–6].

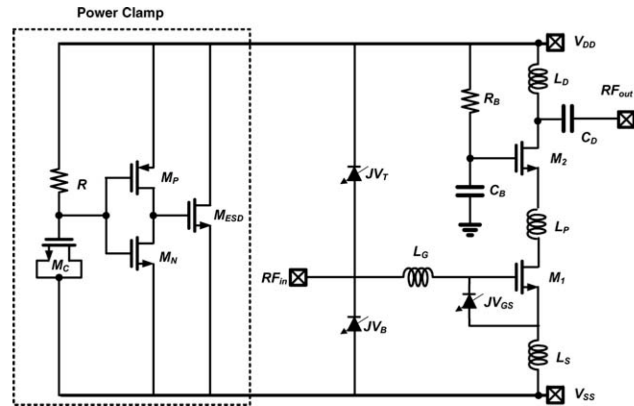

Figure 1 Circuit schematic of the proposed V-band LNA with ESD protection network

In this study, an ESD-protected LNA is proposed using RF junction varactors for noise optimization and ESD robustness enhancement simultaneously. By codesigning the ESD/input matching network, a V-band ESD-protected LNA with a one-stage cascode configuration is demonstrated in 65-nm CMOS. Under a power consumption of only 14.1 mW, the proposed ESD-protected LNA achieves an over 2-kV Human-body-mode ESD protection (over 4-kV for NS and ND modes), a peak power gain of 10.9 dB, and a NF of 5.2 dB at 51 GHz. The NF and power gain are both degraded by only 0.8 dB compared with the reference design.

2. LNA DESIGN

Figure 1 shows the circuit schematic of the core LNA together with the ESD network. The LNA is basically a cascode configuration with inductive source degeneration, which has the advantage of good isolation and the capability of simultaneous noise and impedance matching. The input matching network includes

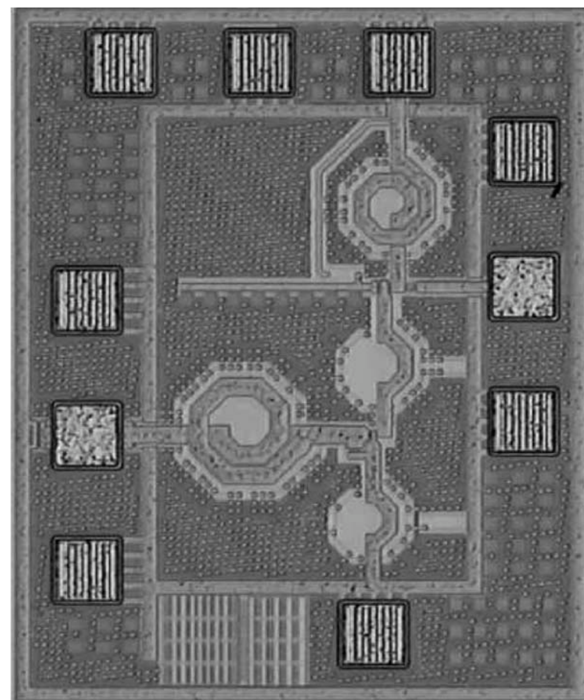

Figure 2 Chip microphotograph (Chip area: 0.51 × 0.41 mm^2)

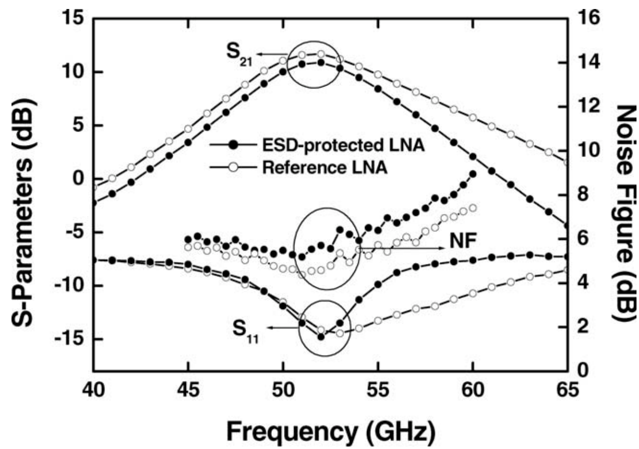

Figure 3 Measured S-parameters and NFs of the LNAs with/without ESD protection

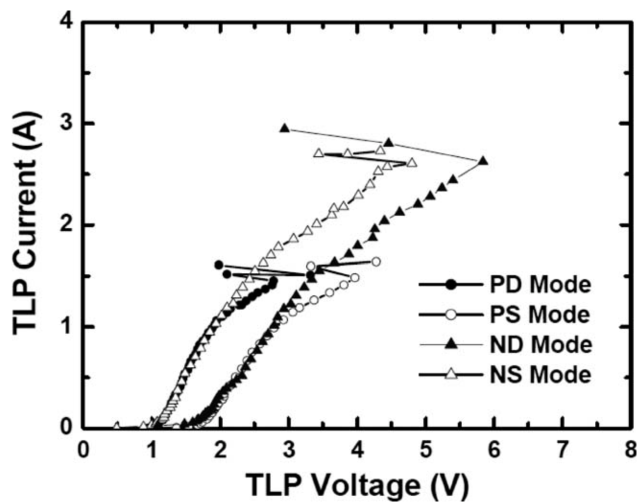

Figure 4 Measured TLP I–V curves of the proposed ESD-protected LNA

two junction varactors JVT and JVB (also used as ESD devices), gate inductor LG, source inductor LS, and the gate-source junction varactor JVGS (also used for power-constrained simultaneous noise and input matching (PCSNIM) and ESD enhancement simultaneously). All the elements for input matching are co-optimized in the beginning of LNA design, and hence the performance degradation due to the extra ESD network can be minimized. The inductor LP inserted between the common-source and common-gate stage of the cascode configuration is used for gain peaking, and also resonating with the parasitic capacitances to improve output matching [7]. The drain inductor LD and capacitor CD are used for the output-matching network in the 50-Ω measurement environment. The dual-diode topology (JVT and JVB) is used for the ESD devices at the RF input to provide the direct ESD current paths for the PD and NS modes. The power clamp consists of RC (resistor R and MOS capacitor MC) and inverter (MP and MN) to trigger the large NMOS (MESD), which provides a low-impedance path from VDD to ground and completes the ESD paths for PS and ND modes. An extra gate-source MIM capacitor is widely used for the input stage of LNA design to achieve PCSNIM [8]. In this study, instead of using the conventional MIM capacitor, the junction varactor JVGS is adopted, serving as the extra gate-source capacitance for low power design. Simultaneously, JVGS will turn on under forward bias during ESD zapping, providing an additional ESD current path to enhance the ESD level for both the NS and ND modes.

3. RESULTS AND DISCUSSION

Figure 2 shows the chip micrograph of the proposed ESD-protected LNA fabricated in a 65-nm CMOS technology, in which the chip area is 0.41×0.51 mm^2 including the probing pads for on-wafer testing both RF and ESD characteristics. The reference design (LNA without ESD protection) with the same chip size was also realized. Figure 3 shows the measured S_{11}, S_{21}, and NFs of the LNA with and without the ESD protection, respectively. The ESD-protected LNA presents a peak power gain of 10.9 dB, an input return loss of greater than 10 dB, and a NF of 5.2 dB at 51 GHz. Compared with the reference design, both the peak gain and NF only degrade by 0.8 dB. The measured third-order-intercept point IIP3 of both LNAs are about -10 dBm at 51 GHz, which indicates that using the RF junction varactors as the ESD devices does not have significant impacts on LNA linearity. The ESD testing was performed using the Barth 4002 transmission line pulse (TLP) test system. Figure 4 shows the TLP I–V characteristics of four different testing modes (PD, PS, ND, and NS) for the ESD-protected LNA [6]. A second breakdown current It_2 up to ~1.4 A can be achieved, corresponding to an ESD level of 2.0 kV in the PD and PS modes. In both ND and NS modes, It_2 is up to ~2.6 A, corresponding to an ESD level of 4.0 kV. By taking the ESD level and chip size into consideration, a figure-of-merit (FOM, modified from Ref. 4), consisting of gain, input third-order intercept point (IIP3), operating frequency (fC), dc power consumption, NF, chip area, and ESD level, is used to quantify both ESD and RF performance for RF LNAs. Table 1 summarize the circuit performance and compares the proposed ESD-protected LNA with

TABLE 1 Performance Comparison of the Proposed ESD-Protected LNAs with Prior Art

Ref.	[3]		[4]		[5]		[6]		This Work	
Tech. (nm)	130		90		90		65		65	
Freq. (GHz)	60		5.5		2.4		5.8		51	
NF (dB)	7.2	8.6	2.7	2.9	2.56	3.2	1.85	2.57	4.4	5.2
Power (mW)	65	65	9.72	9.72	12.9	12.9	7.8	7.8	14.1	14.1
S_{21} (dB)	20.2	20.4	13.3	12.3	22.1	21.9	18.1	16.7	11.7	10.9
S_{11} (dB)	−15	−15	−10.3	−14.4	−12.66	−10.99	−18.7	−15.9	−12.8	−14.2
IIP3 (dBm)	−12	−12	−3	−3	−10.83	−11.01	−10	−11	−10	−10
HBM (kV)	–	6.5/1.5	–	2.0	–	4	–	6.5	–	4.0/2.0
Area (mm2)	0.48	0.715	0.72	0.94	1.44	1.44	0.55	0.55	0.2	0.2
FOM	**	0.9/0.2	**	2.9	**	0.5	**	5.9	**	11.0/5.5

prior arts. The proposed LNA shows an FOM among the best compared with the published results in the table.

$$\text{FOM} = \frac{\text{Gain[abs]} \times \text{IIP3[abs]} \times f_C[\text{GHz}] \times \text{ESD[kV]}}{(\text{NF} - 1)[\text{abs}] \times P_{DC}[\text{mW}] \times \text{Area}[\text{mm}^2]}$$

4. CONCLUSIONS

A V-band LNA with ESD protection network was realized in 65-nm CMOS technology using the proposed RF junction varactors as the ESD devices. Under a power consumption of only 14.1 mW, the LNA demonstrated a NF of 5.2 dB with an associated power gain of 10.9 dB, only a 0.8-dB degradation of both power gain and NF compared with the reference LNA. The proposed gate-source junction varactor design technique successfully enhanced the ESD protection level from 2.0 to 4 kV for the ND and NS modes.

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FIBER BRAGG GRATING CURRENT SENSOR BASED ON BIREFRINGENCE EFFECT

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ABSTRACT: *A novel DC current sensor configuration by combining the sensing theory of fiber Bragg grating (FBG) with the birefringence effect is proposed. Electromagnet force will occur when the measured current is applied due to the sensor configuration of a magnetic coil and a permanent magnet. A sensing FBG and a supporting fiber with the same diameter and material are inserted between two glass sheets. The electromagnet force will act on the glass sheets, resulting in a radial load on the sensing FBG. This transverse load will lead to the birefringence effect because of the different strain or refractive index variation of the two orthogonal axes of the sensing fiber. Thus, two orthogonal polarization modes will be reflected by the sensing FBG with different wavelengths. The theoretical model between Bragg wavelength shifts versus the applied current is derived. Preliminary experiments and simulation results show that current measurement sensitivity can reach 2 nm/A, and measurement resolution is about 0.5 mA. Cross-sensitivity of temperature can be compensated by the differential method.* © 2012 Wiley Periodicals, Inc. Microwave Opt Technol Lett 54:822–826, 2012; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.26609

Key words: *fiber Bragg grating sensor; current sensor; birefringence effect; transverse load; wavelength shift*

1. INTRODUCTION

Several physical principles and effects can be used as the basis of the fiber optic current sensors, such as the electromagnetic induction effect, the Faraday rotation effect, the magnetostrictive effect, the heat effect, the converse piezoelectric effect, the electromagnetic force effect, and so on [1–4]. A traditional Rogowski coil is often used to sample the transmission-line current in those fiber optic current sensors based on the electromagnetic induction effect. So, it is not an all-optical fiber current sensor.

The current sensors based on the principles of magnetostrictive effect, the heat effect, the converse piezoelectric effect, and the electromagnetic force effect could be classified as one sort because the measured current will lead to a force or a displacement, acting on the sensing fibers or fiber Bragg gratings (FBGs). For example, the expansion of the magnetostrictive material under an electromagnetic condition will lead to a length variation of the sensing fiber, which is fixed on the surface of the magnetostrictive material. The length variation will cause the optical phase variation of the fiber optic interferometer. For those FBG current sensors using magnetostrictive effect, the FBG is fixed on the surface of the magnetostrictive material, and the expansion will cause the reflected wavelength shift of the Bragg grating [2]. In these kinds of sensors, the fibers are all glue-bonded on the magnetostrictive material; load effect will occur at the bonding point, leading to the hysteresis effect with increase in the measured current. There are two kinds of electromagnetic force-based fiber current sensors. One is to change the cavity length of the F-P interferometer due to the electromagnetic force-generated displacement [3], and the other is to change reflected wavelength of the FBG sensor due to the electromagnetic force-generated deformation [4].

In this article, a FBG current sensor based on the birefringence effect is proposed. The electromagnetic force generated by the measured current transversely acts on the sensing FBG in the radial direction, resulting in the birefringence effect, which leads to the reflected spectrum separation of the two polarization states. By measuring the wavelength difference between the two polarization states, the relationship between the wavelength difference and the measured current will be established.

2. SENSING STRUCTURE AND MEASUREMENT PRINCIPLE

2.1. Sensing Structure

The schematic diagram of the proposed FBG current sensor system is shown as in Figure 1. In the sensor probe, a sensing FBG