dc and rf characteristics of self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors using molecular beam epitaxy-$Al_2O_3/Ga_2O_3(Gd_2O_3)$ as gate dielectrics

T. D. Lin, P. Chang, H. C. Chiu, and M. Hong[a),b)]
Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan

J. Kwo[a),c)]
Department of Physics, National Tsing Hua University, Hsinchu 30013, Taiwan

Y. S. Lin and Shawn S. H. Hsu
Institute of Electronics Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan

(Received 22 September 2009; accepted 30 November 2009; published 6 April 2010)

dc and rf characteristics of self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors (MOSFETs) using molecular beam epitaxy (MBE) deposited $Al_2O_3/Ga_2O_3(Gd_2O_3)$ (GGO) high κ dielectrics and TiN metal gates are reported. MOSFETs with various oxide thicknesses were fabricated. The $In_{0.53}Ga_{0.47}As$ MOSFETs using Al_2O_3(2 nm)/GGO (5 nm) gate dielectric demonstrated a maximum drain current of 1.05 mA/μm and a peak transconductance of 714 μS/μm, both are the highest values ever reported for enhancement-mode InGaAs MOSFETs with 1 μm gate length. In addition, the same transistors exhibited excellent embedded rf properties and achieved a f_T of 17.9 GHz and a f_{max} of 12.1 GHz. The high-quality *in situ* MBE growth of high κ dielectrics/InGaAs has attributed to the high device performance.
© *2010 American Vacuum Society.* [DOI: 10.1116/1.3276442]

I. INTRODUCTION

Solutions for complementary metal-oxide-semiconductor (CMOS) devices beyond the 16 nm node have been strongly demanded, as the silicon-based technology approaches its physical and technical limits. Research activities have been intensified on combining high κ gate dielectrics with channel materials of high carrier mobility, among which III-V InGaAs compound semiconductors are of great interest due to their high-electron mobilities.

In the 1990s, high-quality molecular beam epitaxy (MBE) deposited Ga_2O_3 (Gd_2O_3) (GGO) (Ref. 1) and Gd_2O_3 (Ref. 2) have unpinned GaAs and InGaAs surface Fermi levels, and further, have enabled the demonstration of the first inversion-channel GaAs and $In_{0.53}Ga_{0.47}As$ MOS field-effect transistors (MOSFETs) in a non-self-aligned approach.[3,4] Recently, atomic layer deposited (ALD) oxides[5–9] and sputtered high κ dielectrics with Si or Ge interfacial layers[10] have been used to passivate InGaAs as well; these have led to the fabrication of inversion-channel InGaAs MOSFETs.[11–15] Non-inversion-channel enhancement-mode (e-mode) InGaAs MOSFETs have also been demonstrated in the configurations of flatband[16] or buried channel[17] type devices. Excellent direct current (dc) performances, including very high drain currents of ~1 mA/μm (Refs. 11, 12, 18, and 19) and a high transconductance of over 700 μS/μm,[18,19] have been achieved in inversion-channel InGaAs (with In content $\geq$53%) MOSFETs. The employment of InAs in pseudomorphic high-electron mobility transistors also led to very high cutoff frequencies (f_T).[20,21]

Nonetheless, reports on the radio frequency (rf) performance of enhancement-mode III-V MOSFET are relatively scant: inversion-channel GaAs MOSFET with 1 μm gate length showed an f_T of 1.2 GHz and a maximum frequency of oscillation (f_{max}) of 2.6 GHz;[22] inversion-channel $In_{0.53}Ga_{0.47}As$ MOSFET with 0.75 μm gate length exhibited an f_T of 7 GHz and an f_{max} of 10 GHz;[4] flatband type $In_{0.3}Ga_{0.7}As$-channel MOSFET demonstrated f_T and f_{max} of 13 and 37 GHz (1 μm gate length), and of 14 and 40 GHz (0.8 μm gate length), respectively.[23] In this article, excellent drive current, transconductance, and high frequency responses of 1 μm gate length $In_{0.53}Ga_{0.47}As$ MOSFETs using Al_2O_3/GGO as gate dielectrics are reported, showing the capability of GGO/$In_{0.53}Ga_{0.47}As$ MOSFETs for future dc and rf applications.

II. DEVICE STRUCTURE AND FABRICATION

A schematic cross section of the self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ MOSFETs is shown in Fig. 1. Undoped buffer layers and Be doped $In_{0.53}Ga_{0.47}As$ layer with doping concentrations of 5×10^{16} cm^{-3} were grown on semi-insulating InP substrates using MBE. Al_2O_3/GGO gate dielectrics were e-beam evaporated onto $In_{0.53}Ga_{0.47}As$ surface, with a procedure reported previously.[24] Sputtered TiN served as the gate metal. Samples with the same Al_2O_3 thickness (2 nm) and different GGO thicknesses (5 and 10 nm) were studied in this work to investigate the device performance with GGO thickness scaling; the corresponding de-

a)Authors to whom correspondence should be addressed.
b)Electronic mail: mhong@mx.nthu.edu.tw
c)Electronic mail: raynien@phys.nthu.edu.tw

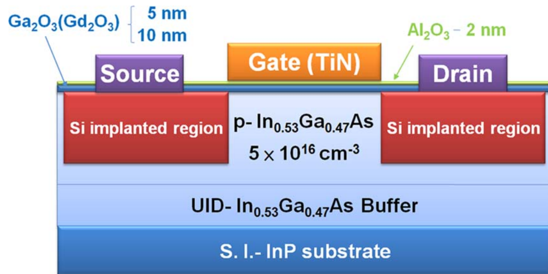

FIG. 1. (Color online) Schematic cross section of $In_{0.53}Ga_{0.47}As$ *n*MOSFETs with MBE-deposited Al_2O_3/GGO dielectrics and sputtered TiN metal gates. The devices were not isolated.

vices will be referred as the transistors with 7- and 12-nm-thick oxides, respectively, in the following discussion.

In situ Al_2O_3 cap, effective in preventing GGO from absorbing moisture, thus passivating the GGO/InGaAs interfaces,[25] has been deposited on GGO/$In_{0.2}Ga_{0.8}As$ to achieve very thin thickness in high κ dielectrics, along with a low leakage current density, a high dielectric constant, a low interfacial density of states, and excellent thermodynamic stability at temperatures above 800 °C. These properties are essential for the self-aligned processed inversion-channel Al_2O_3/GGO/InGaAs MOSFETs.

The inversion-channel devices were fabricated with a previously published self-aligned process.[18,26] MOSFETs with ground-signal-ground rf pads were fabricated for characterizing rf properties. dc and rf performances of the fabricated devices were characterized by Agilent 4156 C semiconductor parameter analyzer and HP 8510 C network analyzer, respectively.

III. RESULTS AND DISCUSSION

The dc *I*-*V* characteristics, measured with a gate bias varying from 0 to 2 V in steps of 0.5 V, of the self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ MOSFETs with 1 μm gate length (L_g) and 10 μm gate width (W_g) are shown in Fig. 2(a). Maximum drain currents (I_{DS}) of 602 μA/μm and 1.05 mA/μm were obtained under a gate bias of 2 V and a drain bias of 2 V for the transistors with 12- and 7-nm-thick oxides, respectively. The corresponding transconductance (g_m) curves are shown in Fig. 2(b). A maximum g_m of 342 μS/μm was demonstrated for the transistor with 12-nm-thick oxide at V_{DS}=2 V and V_{GS}=1.2 V, while g_m of 714 μS/μm was demonstrated for the transistor with 7-nm-thick oxide at V_{DS}=2 V and V_{GS}=0.7 V. The I_{DS} of 1.05 mA/μm (Refs. 18 and 19) achieved by self-aligned 1 μm gate length device with thin oxide is as high as that of the non-self-aligned ALD-Al_2O_3 MOSFETs with shorter gate lengths of 0.4 (Ref. 11) and 0.75 μm (Ref. 12) and higher In-content channels of $In_{0.65}Ga_{0.35}As$ (Ref. 11) and $In_{0.75}Ga_{0.25}As$,[12] respectively, and is the highest ever reported for enhancement-mode InGaAs MOSFETs. The g_m of 714 μS/μm exhibited by the same device (with 7-nm-thick oxide) is among the highest extrinsic g_m values ever demonstrated for InGaAs MOSFETs. The excellent dc characteristics reported in this work show the high-quality TiN/Al_2O_3/GGO/$In_{0.53}Ga_{0.47}As$ heterostructure, particularly the *in situ* MBE growth of the high κ dielectrics and compound semiconductors.

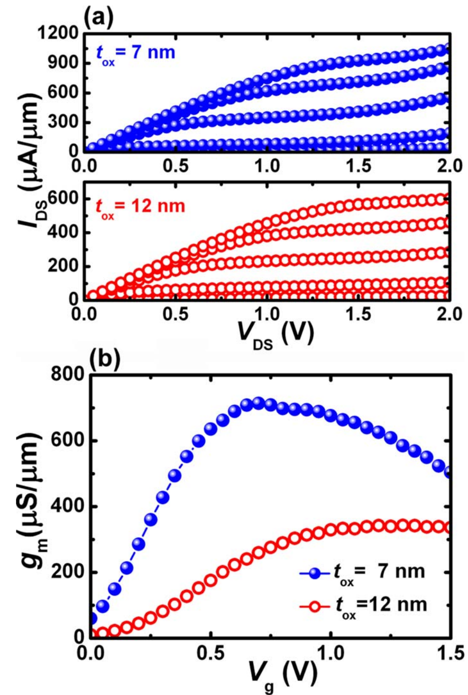

FIG. 2. (Color online) (a) Output characteristics I_{DS} vs V_{DS} of 1 μm(L_g) ×10 μm(W_g) self-aligned inversion-channel Al_2O_3/GGO/$In_{0.53}Ga_{0.47}As$ MOSFETs. (Top: output characteristics of the transistor with 7-nm-thick oxide, showing a maximum I_{DS} of 1.05 mA/μm; bottom: that of the transistor with 12-nm-thick oxide, exhibiting a maximum I_{DS} of 602 μA/μm.) (b) Transconductance g_m curves of the inversion-channel $In_{0.53}Ga_{0.47}As$ MOSFETs with 7- and 12-nm-thick oxides, showing peak g_m's of 714 and 342 μS/μm, respectively. Both curves were measured at V_{DS}=2 V.

rf characteristics extracted from the MOSFETs with ground-signal-ground rf pads are shown in Fig. 3(a). The gate length and the finger width of the devices are 1 and 10 μm, respectively. The f_T and f_{max} of rf devices can be estimated by the small-signal equivalent circuit model parameters with the following equations:[27]

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs}+C_{gd}}, \quad (1)$$

$$f_{max} = \frac{f_T}{2\sqrt{(R_g)(g_{ds}+2\pi f_T C_{gd})}}, \quad (2)$$

where g_m is the transconductance, C_{gs} and C_{gd} are the gate-to-source and gate-to-drain capacitances, respectively, and R_g is the gate resistance. As biased at V_{GS}=1.1 V and V_{DS} =2 V, the transistor with 12-nm-thick oxide exhibited a f_T of 6.9 GHz and a f_{max} of 4.7 GHz. Figure 3(a) also shows the rf performance of device with 7-nm-thick gate oxide biased at V_{GS}=0.6 V and V_{DS}=2 V. Compared to that of the device with 12-nm-thick gate oxide, the device with 7-nm-thick gate oxide exhibited a better rf performance due to a higher g_m value (714 μS/μm). The f_T and f_{max} are 17.9 and 12.1

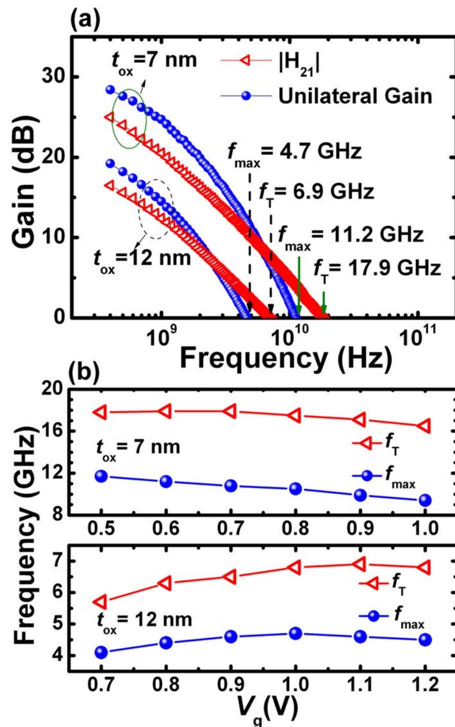

FIG. 3. (Color online) (a) Embedded rf performances of the devices (biased at $V_{DS}=2$ V) mentioned in Fig. 2. The transistors with thin gate oxides exhibited f_T and f_{max} of 17.9 and 12.1 GHz, respectively; those with thick oxides exhibited f_T and f_{max} of 6.9 and 4.7 GHz, respectively. (b) Frequency responses of the two devices as a function of gate voltage. Both the f_T and f_{max} show very minor change with varying gate bias, typical characteristics of MOSFETs.

GHz, respectively, which are roughly 2.5 times higher than those of the device with 12-nm-thick gate oxide and are proportional to the g_m values. Notice that the parasitic capacitances resulted from the lack of isolation seriously affect the f_{max} of the devices. In addition, there also exists a parasitic conduction path passing through the low electrical-resist InGaAs epilayers, which acts like resistive parasitics. Since f_{max} is more sensitive to the parasitics, it is reasonable to have f_{max} smaller than f_T.

Figure 3(b) shows the frequency response of each device as a function of the gate voltage. Both the f_T and f_{max} show very minor change with varying gate bias, a typical characteristic of MOSFET, since the g_m value is almost constant while approaching the maximum value and the input junction capacitance remains constant as operated in a strong inversion region. Notice that the rf performances reported here were not de-embedded, which certainly lead to lower rf performances. No isolation between devices had been introduced in this work and an additional conduction path was formed between the input pad and device substrate, resulting in additional parasitic components and power loss. As a consequence, the power gain was also degraded, again resulted in underestimated f_T and f_{max}. Nevertheless, compared to the previously reported (In)GaAs MOSFETs, the rf performance exhibited by the present self-aligned inversion-channel $Al_2O_3/GGO/In_{0.53}Ga_{0.47}As$ MOSFET with 7-nm-thick gate oxide is still very good; the non-de-embedded f_T of 17.9 GHz and f_{max} of 12.1 GHz are much higher than those of non-self-aligned inversion-channel GGO/GaAs (Ref. 22) and $GGO/In_{0.53}Ga_{0.47}As$ (Ref. 4) MOSFETs, and are comparable with those of the non-inversion-channel flatband-type $In_{0.3}Ga_{0.7}As$-channel MOSFET,[23] in which the devices are isolated using oxygen implantation. Taking the de-embedding and isolation processes into consideration, much higher intrinsic rf performance is expected for the self-aligned inversion-channel $Al_2O_3/GGO/In_{0.53}Ga_{0.47}As$ MOSFET.

Both the dc and rf performances were improved by decreasing oxide thickness, indicating that the inversion-channel $In_{0.53}Ga_{0.47}As$ MOSFET with Al_2O_3/GGO gate dielectric is highly scalable. The performances will be further enhanced by optimizing implantation/activation, employing a channel of higher indium content, shortening the gate length, replacing the Al_2O_3-cap layer with *in situ* metal gates, and introducing the de-embedding and isolation processes.

IV. CONCLUSION

Self-aligned inversion-channel $Al_2O_3/GGO/In_{0.53}Ga_{0.47}As$ MOSFETs have given excellent dc and rf characteristics, with the maximum drain current being the highest ever reported and the peak transconductance being the highest extrinsic values ever demonstrated for the InGaAs MOSFETs with 1 μm gate length.; the non-de-embedded rf performances exhibited by the $Al_2O_3/GGO/In_{0.53}Ga_{0.47}As$ MOSFETs are also outstanding. These device performances have revealed the MBE grown high-quality MOS structures as being one of the most promising candidates for CMOS devices beyond the 16 nm node.

ACKNOWLEDGMENTS

The authors wish to thank the Ministry of Education and National Science Council, Taiwan for supporting this work (Grant Nos. NSC-98-2120-M-007-002 and NSC-97-3114-M-007-001). They would also like to acknowledge the support from the Intel and the Asian Office of Aerospace Research and Development of the U.S. Air Force.

[1]M. Hong, J. P. Mannaerts, J. E. Bower, J. Kwo, M. Passlack, W. Y. Hwang, and L. W. Tu, J. Cryst. Growth **175–176**, 422 (1997).
[2]M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, and A. M. Sergent, Science **283**, 1897 (1999).
[3]F. Ren *et al.*, Solid-State Electron. **41**, 1751 (1997).
[4]F. Ren *et al.*, IEEE Electron Device Lett. **19**, 309 (1998).
[5]P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, H. J. L. Gossmann, M. Hong, K. K. Ng, and J. Bude, Appl. Phys. Lett. **84**, 434 (2004).
[6]M. L. Huang, Y. C. Chang, C. H. Chang, Y. J. Lee, P. Chang, J. Kwo, T. B. Wu, and M. Hong, Appl. Phys. Lett. **87**, 252104 (2005).
[7]M. L. Huang, Y. C. Chang, C. H. Chang, T. D. Lin, J. Kwo, T. B. Wu, and M. Hong, Appl. Phys. Lett. **89**, 012903 (2006).
[8]Y. C. Chang *et al.*, Appl. Phys. Lett. **92**, 072901 (2008).
[9]S. Koveshnikov *et al.*, Device Research Conference Digest, 2008 (unpublished), p. 43.
[10]H. S. Kim *et al.*, Appl. Phys. Lett. **93**, 062111 (2008).
[11]Y. Xuan, Y. Q. Wu, and P. D. Ye, IEEE Electron Device Lett. **29**, 294 (2008).
[12]Y. Xuan, T. Shen, M. Xu, Y. Q. Wu, and P. D. Ye, Tech. Dig. - Int.

Electron Devices Meet. **2008**, 371.
[13]H. C. Chiu *et al.*, Device Research Conference Digest, 2009 (unpublished), p. 83.
[14]J. P. de Souza *et al.*, Appl. Phys. Lett. **92**, 153508 (2008).
[15]H.-S. Kim *et al.*, Appl. Phys. Lett. **93**, 132902 (2008).
[16]R. J. W. Hill *et al.*, IEEE Electron Device Lett. **28**, 1080 (2007).
[17]Y. Sun *et al.*, IEEE Electron Device Lett. **28**, 473 (2007).
[18]T. D. Lin, H. C. Chiu, P. Chang, L. T. Tung, C. P. Chen, M. Hong, J. Kwo, W. Tsai, and Y. C. Wang, Appl. Phys. Lett. **93**, 033516 (2008).
[19]M. Hong, J. Kwo, T. D. Lin, and M. L. Huang, MRS Bull. **34**, 514 (2009).
[20]D.-H. Kim and J. A. del Alamo, IEEE Electron Device Lett. **29**, 830 (2008).
[21]D.-H. Kim and J. A. del Alamo, Tech. Dig. - Int. Electron Devices Meet **2008**, 719.
[22]Y. C. Wang *et al.*, Mater. Res. Soc. Symp. Proc. **573**, 219 (1999).
[23]M. Passlack *et al.*, Tech. Dig. - Int. Electron Devices Meet. **2007**, 621.
[24]M. Hong, M. Passlack, J. P. Mannaerts, J. Kwo, S. N. G. Chu, N. Moriya, S. Y. Hou, and V. J. Fratello, J. Vac. Sci. Technol. B **14**, 2297 (1996).
[25]K. H. Shiu, T. H. Chiang, P. Chang, L. T. Tung, M. Hong, J. Kwo, and W. Tsai, Appl. Phys. Lett. **92**, 172904 (2008).
[26]C. P. Chen, T. D. Lin, Y. J. Lee, Y. C. Chang, M. Hong, and J. Kwo, Solid-State Electron. **52**, 1615 (2008).
[27]C. Y. Chan, S. C. Chen, M. H. Tsai, and S. Hsu, IEEE Electron Device Lett. **29**, 1245 (2008).