A 0.18-μm CMOS Balanced Amplifier for 24-GHz Applications

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***Abstract*—A 24-GHz balanced amplifier (BA) with a 45-dB gain is realized in 0.18-μm CMOS technology. An effective technique, π-type parallel resonance, is proposed to boost the high-frequency gain of a MOSFET by resonating out the inherent capacitances. The miniaturized lumped-element coupler in the circuit occupies a chip area of only $\sim$2% compared to that of the conventional transmission-line coupler. The BA consumes 123 mW from a supply voltage of 1 V. To the best of the authors' knowledge, the proposed CMOS BA presents the highest gain of 45.0 dB with a chip area of 0.97 $\times$ 0.63 mm^2 (core area: 0.78 $\times$ 0.43 mm^2) among the published narrowband amplifiers with similar technologies and operation frequencies.**

***Index Terms*—Balanced amplifier, CMOS, lumped-element coupler, narrowband amplifier, parallel resonance.**

I. Introduction

THE balanced amplifier (BA) configuration was reported first in 1965 as a way of providing a good input/output matching, high degree of stability, and a 3-dB higher linearity compared to a single amplifier [1], [2]. Composed of two identical amplifiers and two 90° couplers, this design concept was employed widely for millimeter-wave applications by III–V [3]–[7] and SiGe [8], [9] technologies. The CMOS technology with high integration level, low power consumption, and low cost should also be an excellent candidate for this circuit configuration. However, a fully integrated BA in a standard CMOS process has not been reported to date. In this paper, a 24-GHz amplifier with a 45-dB gain is achieved in a standard 0.18-μm CMOS technology by the newly proposed gain-boosting technique and the balanced circuit configuration. The 24-GHz band is allocated for the industrial, scientific, and medical (ISM) applications, and several CMOS amplifiers operated in this frequency range have been reported [10]–[12]. Among these, the proposed BA shows the highest gain under only a 1-V power supply.

The proposed high-gain BA can be employed in a gain block as the post-stage amplifier to further increase the signal level. In this case, its contribution to the total noise figure (NF) is not significant if a low-noise amplifier (LNA) is used as the previous stage. Linearity is also an important consideration, and there is typically a tradeoff between linearity and gain. For the high-gain design here, a relatively lower input 1-dB gain compression point ($P_{1\ \mathrm{dB,in}}$) is expected. This amplifier may find suitable applications in a communication system where the received signal level is low at the front-end, thus the low $P_{1\ \mathrm{dB},in}$ is not a major concern. With the high-gain amplifier used, the overall signal level can be boosted substantially to relax the requirement for other stages in the system. For example, a mixer with a small conversion gain or even a passive type can be used to maintain an overall signal linearity.

Design of millimeter-wave CMOS BA encounters two main challenges. First, the high-frequency performance of the active device is generally not as good as the transistors in the SiGe and III–V technologies. Second, the couplers can be very lossy on the Si substrate and occupy a large chip area. To achieve high gain and high operation frequency simultaneously, a new technique of using π-type parallel resonance (PPR) is proposed. By incorporating three inductors, the inherent gate–source capacitances C_{gs}, gate–drain capacitances C_{gd}, and drain–source capacitances C_{ds} of a MOSFET can be effectively resonated out with the parallel LC networks. In addition, the lumped-element coupler is adopted here instead of using the area-consuming transmission-line coupler [13], [14]. Compared with the branch-line coupler using quarter-wave transmission lines, the proposed lumped-element coupler can reduce the chip area to only $\sim$2% without sacrificing the coupler performance at 24 GHz.

This paper is organized as follows. Section II describes details for the CMOS BA design including the PPR technique, the circuit topology of the amplifier, and the lumped-element coupler. The measured results are presented in Section III, and Section IV concludes this study.

II. BA Design

A standard BA is composed of two 90° couplers and two identical amplifiers (Amp1 and Amp2), as illustrated in Fig. 1, where the input signal is divided into two parts by the input coupler with an equal power splitting, but a 90° phase difference. Both signals are amplified separately in each path and then combined by the output coupler with a reversed 90° phase shift to obtain the overall output. In principle, the gain of a BA is the same as a single amplifier. However, the stability and input/output impedance matching can be improved by the balanced design even if the single amplifier of each branch is highly mismatched and with a very high gain. Therefore, the single amplifier of each branch can be intentionally mismatched to achieve a better circuit performance. In addition, the 90° couplers ensure excellent isolation from the previous and/or the following stages for easy system integration. As shown in Fig. 1, the input power from

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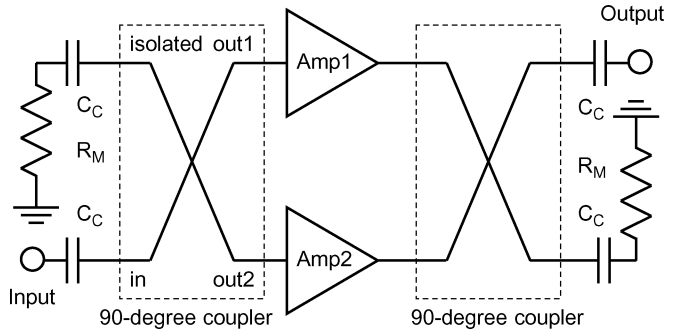

Fig. 1. Circuit topology of a BA.

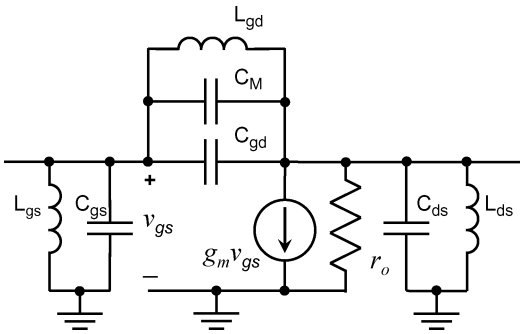

Fig. 2. Small-signal equivalent circuit model of a MOSFET with PPR inductors and the intentional Miller capacitor (C_M).

port *in* is divided to be half with a 90° phase difference and delivered to ports *out1* and *out2*. Part of the signal can be reflected back due to impedance mismatch. After passing through the 90° coupler again, the reflected signals from both paths appearing at port *in* have a 180° phase difference, which can cancel each other resulting in an unconditionally matched condition at the input. On the other hand, the reflected signals with a 0° phase difference are superimposed at port *isolated* and terminated by a 50-Ω resistor (R_M). Similarly, the output port also has a minimum reflection to guarantee the matching and stability. Compared with a single amplifier, the BA configuration needs two couplers and two amplifiers, resulting in larger power consumption and chip area. However, the output 1-dB gain compression point $(P_{1\ \mathrm{dB,out}})$ is 3 dB higher than that obtained from a single amplifier. In addition, even when one of the amplifiers fails, the circuit can still operate with reduced gain (−6 dB). The design details of the high-performance amplifier and the small-size coupler are described in Sections II-A–C.

A. PPR Technique

For a MOSFET, the RF performance is ultimately limited by the inherent capacitances of the transistor including C_{gs}, C_{gd}, and C_{ds}, as shown in Fig. 2. A simple, yet effective approach, i.e., PPR, is proposed here to improve the device frequency response. By adopting inductors in parallel with the intrinsic capacitances, the parallelly resonated LC networks become an open circuit at the desired operation frequency f_o. As a consequence, the capacitance limited high-frequency response of the MOSFET can be improved significantly.

As shown in Fig. 2, the PPR inductors are the gate–source inductor L_{gs}, gate–drain inductor L_{gd}, and drain–source inductor

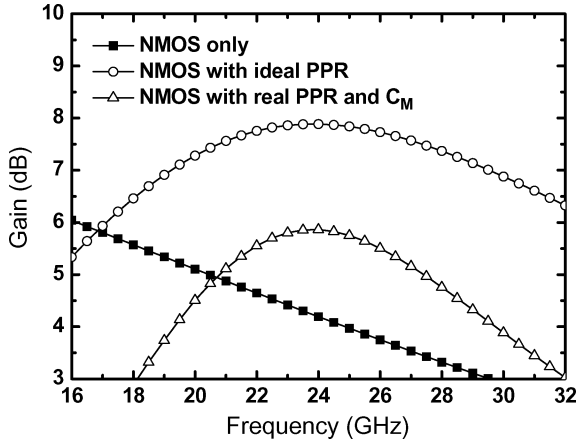

Fig. 3. Simulated power gain of a CS stage without and with ideal/real PPR inductors.

L_{ds}, and C_M is an intentional Miller capacitor. Using the simple resonant equation for a parallel LC network, the inductances can be determined. With the inductors properly designed, the devices can achieve a maximum voltage gain (A_0) of $g_m r_o$ at f_o, where g_m and r_o are the transconductance and the output resistance of the MOSFET, respectively. It has been reported that using L_{gd} as the neutralization technique is impractical because a large inductance is required [15]. In this design, an additional capacitor C_M is inserted between the gate and the drain to lower the required L_{gd}. At the resonant frequency f_o, the L and C cancel each other, thus only a parallel resistor R_p exists between the two terminals, where R_p is mainly originated from the parasitic series resistance of an on-chip spiral inductor. These parasitic resistances, especially the one resulting from L_{gd}, can severely degrade the gain A_0. A simple method to reduce the undesired resistance in the LC resonant circuit is to use a smaller inductor by increasing the capacitance. With a capacitor C_M connected between the gate and the drain intentionally, the required L_{gd} to resonate at f_o can be effectively reduced.

Fig. 3 compares different cases to illustrate the merit of using the proposed PPR technique. For a common-source (CS) stage biased at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 1$ V, the simulated power gain S_{21} is 4.2 dB at 24 GHz. By employing three ideal PPR inductors, the gain can be improved up to 7.9 dB. With the real inductors and C_M in the CMOS process, the gain is enhanced to 5.9 dB.

B. Circuit Topology

The amplifier of each branch consists of eight CS stages in cascade, as shown in Fig. 4. The PPR technique is incorporated into each stage to boost the amplifier gain up to A_0^8. In this cascade configuration, L_{ds} and L_{gs} from the next stage can be combined to be one inductor L_{DD}, as shown in this figure. To simplify the circuit design and layout complexities, each CS stage is designed to be identical. Note that the required PPR inductor L_{gs} at the gate terminal of M_1 is removed, while one additional L_{gs} is inserted at the drain terminal of M_8. In this manner, the overall gain is comparable, and the layout of each CS stage is exactly the same. By connecting L_{DD} to the power supply voltage V_{DD}, each transistor is biased at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = V_{DD}$. For the operation frequency f_o designed at 24 GHz, the component

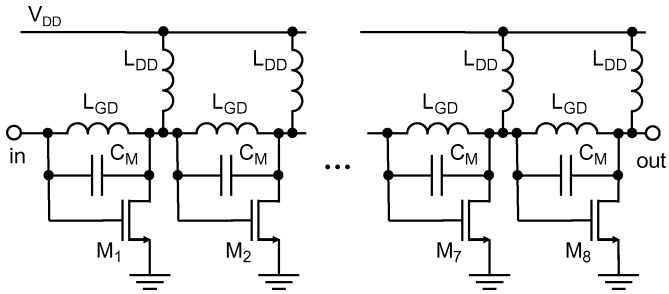

Fig. 4. Circuit topology of the single amplifier of each branch in the BA configuration.

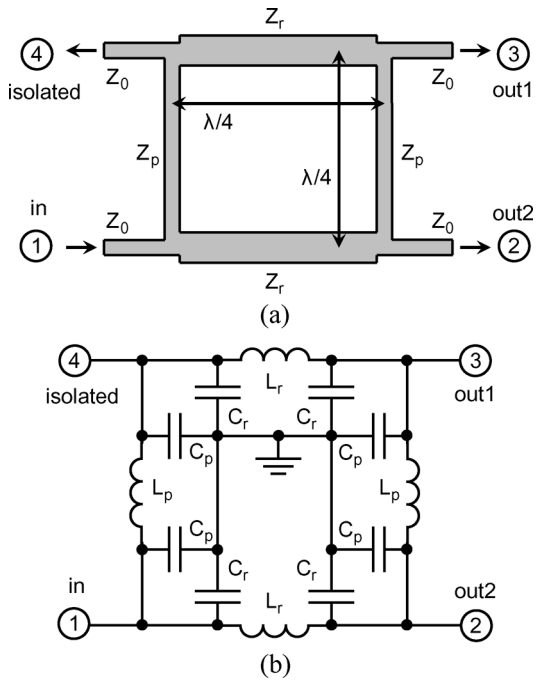

Fig. 5. 90° couplers in: (a) branch-line and (b) lumped-element topologies.

values are listed as follows: $L_{DD} = 1.08$ nH, $L_{\rm GD} = 0.54$ nH, $C_M = 52$ fF, and the gatewidth $W_g = 64$ μm, where C_M is implemented by a metal–insulator–metal (MIM) capacitor with a chip area of 6 μm $\times$ 6 μm.

C. Design of Lumped-Element Coupler

The 90° couplers used for BA applications are usually realized by transmission lines, such as the branch-line coupler, as depicted in Fig. 5(a). The quarter-wavelength $(\lambda/4)$ transmission lines provide a 90° phase delay from port 1 to port 2, and a 180° delay from port 1 to port 3. The characteristic impedances of the series (Z_r) and the shunt (Z_p) transmission lines can determine the delivered power ratio of the two output ports. For an equal power splitting, Z_r and Z_p should be designed as $Z_0/\sqrt{2}$ and Z_0, respectively, where Z_0 is the characteristic impedance of the system, and is typically 50 Ω. For a design at 24 GHz, the calculated physical length of a quarter-wave microstrip line is about 1560 μm in the CMOS technology used here, which makes the balanced design with two couplers consume a large chip area.

In this study, the lumped-element coupler constructed from spiral inductors and MIM capacitors, as shown in Fig. 5(b), is adopted. Compared to the transmission-line coupler, this design is more area efficient, but has a smaller bandwidth [13]. With the same function of the branch-line coupler, each $\lambda/4$ transmission line section can be replaced by an LC π-network including one inductor L and two capacitors C in the miniaturized lumped-element coupler. Using $ABCD$-parameters, the required L and C can be determined by the following equations for both series and shunt lines, where the matrix on the left side is for a lossless $\lambda/4$ transmission line, and the matrix on the right side is for the equivalent LC π-network. For the series line,

$$\begin{bmatrix} \cos\theta & jZ_r\sin\theta \\ j\dfrac{1}{Z_r}\sin\theta & \cos\theta \end{bmatrix} = \begin{bmatrix} 1-\omega_o^2 L_r C_r & j\omega_o L_r \\ j\omega_o C_r\left(2-\omega_o^2 L_r C_r\right) & 1-\omega_o^2 L_r C_r \end{bmatrix} \quad (1)$$

where θ is 90°, and for the shunt branch line, a similar equation can be constructed as follows:

$$\begin{bmatrix} \cos\theta & jZ_p\sin\theta \\ j\dfrac{1}{Z_p}\sin\theta & \cos\theta \end{bmatrix} = \begin{bmatrix} 1-\omega_o^2 L_p C_p & j\omega_o L_p \\ j\omega_o C_p\left(2-\omega_o^2 L_p C_p\right) & 1-\omega_o^2 L_p C_p \end{bmatrix}. \quad (2)$$

By solving the above two equations, the values of the lumped elements can be obtained as follows:

$$L_r = Z_r/\omega_o \quad (3)$$

$$L_p = Z_p/\omega_o \quad (4)$$

$$C_r + C_p = \frac{1}{\omega_o}\left(\frac{1}{Z_r}+\frac{1}{Z_p}\right). \quad (5)$$

Note that C_r and C_p can be combined as one capacitor in circuit implementation since these two capacitors are connected in parallel.

By considering the parasitic effects of both L and C, the finally optimized component values of the 24-GHz lump-element coupler are listed as follows: $L_r = 0.23$ nH, $L_p = 0.33$ nH, and $C_r + C_p = 110$ fF, where C_r and C_p are implemented by a MIM capacitor with a chip area of 9.5 μm $\times$ 9.5 μm. The total chip area is $\sim$ 200 μm $\times$ 200 μm, which occupies an area of only $\sim$2% compared to that of the conventional branch-line coupler using the same technology.

From the EM simulation [16], the S-parameters based on the actual layout of the lumped-element coupler are shown in Fig. 6. At 24 GHz, the insertion losses from port 1 to ports 2 and 3 are 6.4 and 6.2 dB, respectively. The loss is higher than the desired value of 3 dB due to the resistive loss introduced from the spiral inductors. The reflection coefficients of port *in* and the isolation from port *in* to port *isolated* are both below -15 dB. The phase difference between the two output ports is 89.6°.

For such a high gain amplifier, stability is a critical design consideration. To achieve unconditional stability, the stability factor K and the stability measure B_1 should be larger than 1 and 0, respectively [17]. The simulation results indicate that

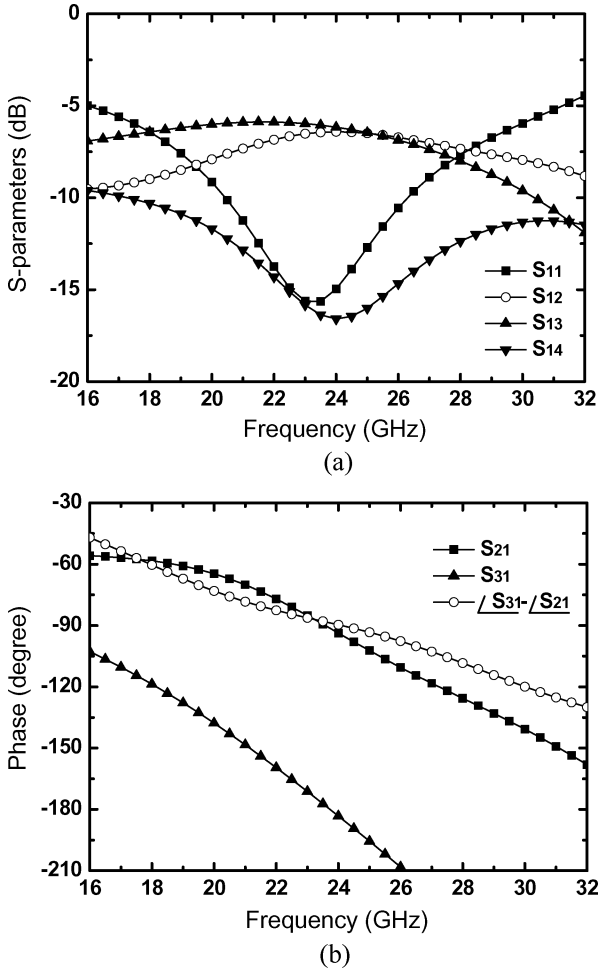

Fig. 6. Simulated S-parameters of the 24-GHz lumped-element coupler for: (a) magnitude and (b) phase.

each inter-stage and the entire circuit are unconditionally stable over a wide frequency range. The amplifier also shows unconditional stability under the V_{DD} varying in a range from 0.6 to 1.8 V.

III. Experimental Results

The fully integrated BA was fabricated in the 0.18-μm CMOS technology with a chip area of 0.97 $\times$ 0.63 mm^2 including the probing pads (core area: 0.78 $\times$ 0.43 mm^2), as shown in Fig. 7. To reduce the interconnect loss, the semicoaxial (SC) line structure was employed in the design [18], [19]. The chip was measured on-wafer by using coplanar ground–signal–ground (GSG) probes (Picoprobe 67A-GSG-125-C-W). Fig. 8 shows the measured S-parameters, where the gain S_{21} at 24 GHz is 41.6 dB, and the peak gain G_p is 45.0 dB at the frequency f_p of 23.7 GHz. S_{11} and S_{22} at f_p are -10.8 and -9.1 dB, respectively, which indicate a good input/output matching. From the measured S-parameters, the amplifier is unconditionally stable over the measured frequency range from 16 to 32 GHz, as shown in Fig. 9. The NF was measured from 16 to 26.5 GHz, as shown in Fig. 10, and an NF of 10.8 dB was obtained at f_p. The output power level as a function of the input power was measured at f_p, which indicated a $P_{1\ \mathrm{dB,out}}$ of -2.3 dBm, as shown in Fig. 11. Under a supply voltage of 1 V, the power

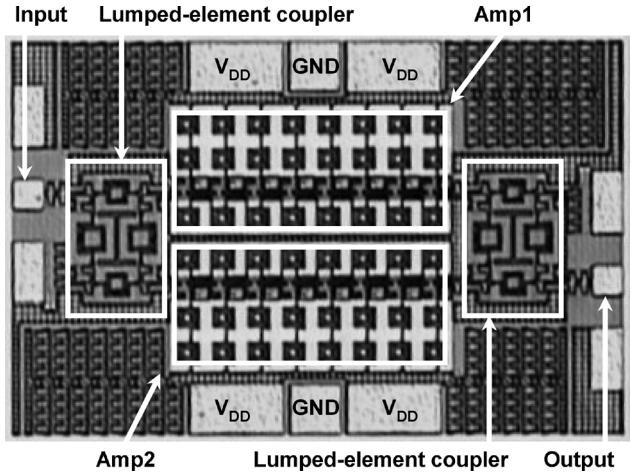

Fig. 7. Chip micrograph for the 24-GHz BA. The chip size including the probing pads is 0.97 $\times$ 0.63 mm^2 (core area: 0.78 $\times$ 0.43 mm^2).

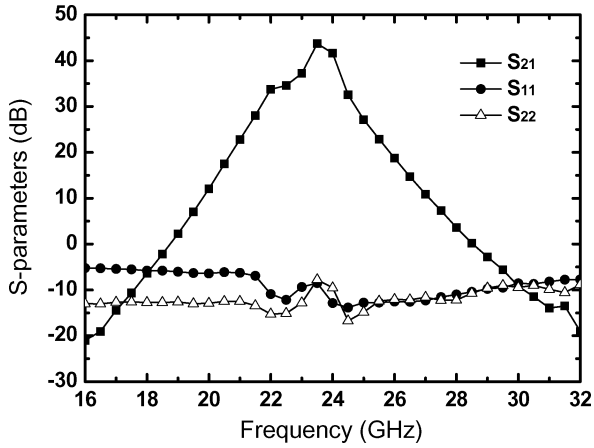

Fig. 8. Measured S-parameters as a function of frequency.

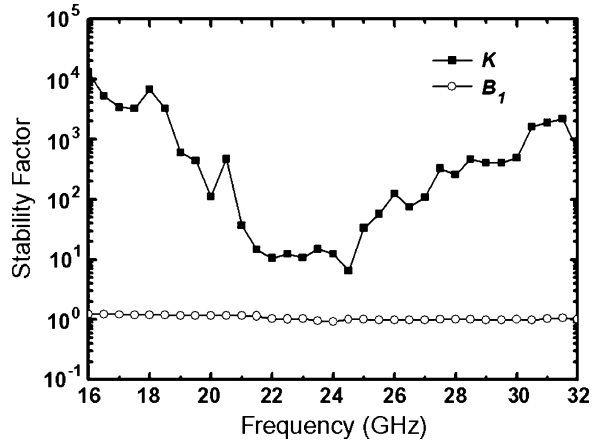

Fig. 9. Measured stability factors as a function of frequency.

consumption (P_{DC}) is 123 mW. By employing the proposed PPR technique, a high peak gain-frequency product per dc power ($G_p f_p / P_{\mathrm{DC}}$) figure-of-merit of 34.3 GHz/mW can be achieved. The circuit performances of the proposed BA are summarized in Table I together with other studies at similar operation frequencies [10]–[12]. Although the balanced-type

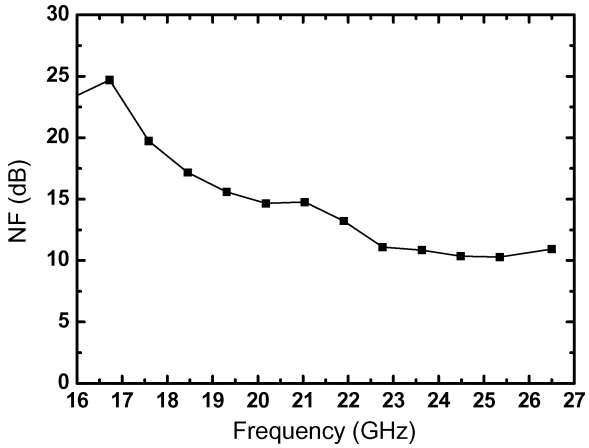

Fig. 10. Measured NF as a function of frequency.

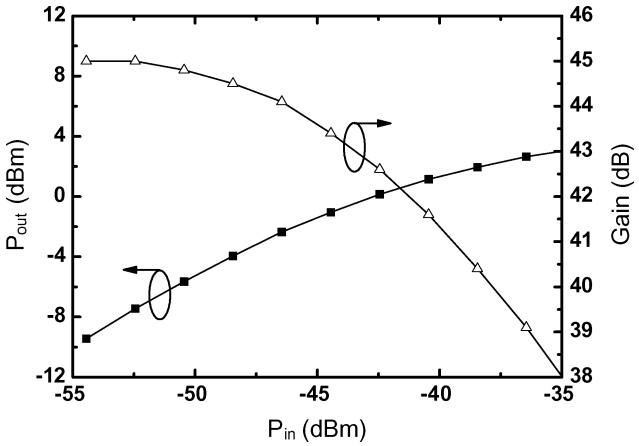

Fig. 11. Measured output power and gain versus input power at the peak gain frequency (f_p).

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER STUDIES

Ref.	This work	[10]	[11]	[12]
G_p (dB)	45.0	15.0	10.0	8.9
f_p (GHz)	23.7	21.8	24.0	25.7
S_{11} (dB)	-10.8	-21.0	-14.0	-14.0
S_{22} (dB)	-9.1	—	—	-12.0
NF (dB)	10.8	6.0	6.0*	6.9
$P_{1dB,out}$ (dBm)	-2.3	-9.0	—	-2.3
V_{DD} (V)	1	1.5	—	1.8
P_{DC} (mW)	123	24	47	54
Chip area (mm^2)	0.97x0.63	—	—	1.05x0.7
Core area (mm^2)	0.78x0.43	0.2x0.25	—	—
$G_p f_p/P_{DC}$ (GHz/mW)	34.3	5.1	1.6	1.3
Process	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS

* Extrapolated from measured results up to 20 GHz.

design requires two amplifiers and couplers, the core area in this design is still very small ($\sim$ 0.34 mm^2) owning to the miniaturized lumped-element coupler. To the best of the authors' knowledge, the proposed BA presented the highest gain and $G_p f_p/P_{\rm DC}$ among the published results with similar technologies and operation frequencies.

IV. CONCLUSION

In this paper, a fully integrated CMOS BA was presented, and demonstrated a gain of 45.0 dB at around 24 GHz with unconditional stability. The input and output ports were both matched well. Under a supply voltage of 1 V, NF and $P_{1\ \rm dB,out}$ were 10.8 dB and -2.3 dBm, respectively. With the proposed PPR design technique and the employment of the lumped-element couplers, the proposed BA showed the highest $G_p f_p/P_{\rm DC}$ figure-of-merit of 34.3 GHz/mW among published results.

ACKNOWLEDGMENT

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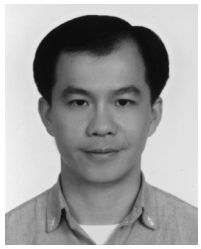

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