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High-frequency AlGaN/GaN T-gate HEMTs on extreme low resistivity silicon substrates

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The T-gate high frequency AlGaN/GaN high electron mobility transistors (HEMTs) are demonstrated on an 8 inch extremely-low resistivity (ELR) silicon substrate with a resistivity of ~2.5 mΩ cm to investigate the potential of using the ELR Si substrate for RF applications. The devices are also fabricated on the 60 Ω cm substrate for comparison. The 0.1 μm T-gate is realized by e-beam lithography to improve the high frequency characteristics of the devices. The short-circuit current gain cutoff frequency (f_T), the maximum oscillation frequency (f_{max}), and maximum transconductance ($g_{m,max}$) of 27 GHz, 71 GHz and 247 mS mm^{-1} can be achieved, respectively. The obtained high frequency performance is among the best reported to date for the GaN HEMTs on such low resistivity silicon substrates.

1. Introduction

With the continuous advancement of the IMT-2020 standard, the fifth-generation (5 G) wireless communication systems are ready for the market. Power amplifiers designed with the conventional CMOS processes are not suitable for many emerging 5 G applications. For the sub-6GHz band of 5 G wireless communication, the GaN-based high electron mobility transistors (HEMTs) on silicon substrates have attracted much attention recently.[1–4] Compared with other conventional semiconductor materials, the GaN-on-Si HEMTs can offer remarkable higher power performance with a much lower cost owing to the large dimension silicon wafers with the advanced GaN epitaxial technology.[5–7]

The low cost and high performance of GaN-on-Si devices have been a strong motivation for related research over the past few years. Most of the early researches are based on the silicon substrate with high resistivity such as 6 kΩ cm for RF applications.[8,9] The primary consideration is that the high resistivity silicon substrate has smaller substrate parasitic effects, which could significantly degrade the device performance for high frequency operation. However, the high resistivity silicon substrate is relatively expensive due to the complicated process. Also, the weak mechanical strength compared with the low resistivity substrate could cause wafer bowing and cracking during the epitaxial process.[10–12]

To take advantage of large wafer diameters with reduced cost, GaN HEMTs grown on large size low resistivity (LR) (ρ in the range of tens of Ω cm) silicon substrates with a diameter up to 150 mm was reported.[13,14] Also, high performance passive components, such as inductors, coplanar waveguides, and transmission line, were realized on the LR Si substrates.[14–17] However, growing a high-quality insulating GaN buffer layer and fabricate high frequency devices on a large diameter Si wafer still faces significant challenges.[14] Also, it has not been reported to have the GaN-on-Si HEMTs realized on the extremely-low resistivity (ELR) silicon substrate (ρ in the range of tens of ~mΩ cm). Figure 1 shows the examples of the in-house grown GaN epitaxial layer on an 8 inch LR silicon substrate by MOCVD. As can be seen, cracks caused by plastic deformation exist at the center of the wafer, which could significantly degrade the epilayer quality and device performance.[10,18]

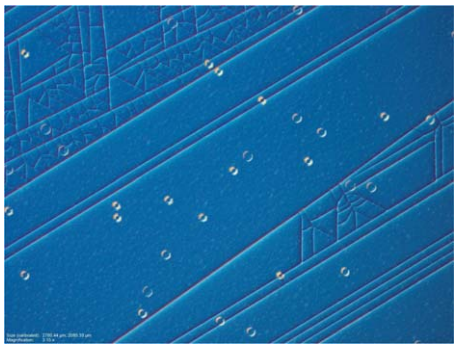


Fig. 1. (Color online) Photo of crack in the center of the wafer that GaN grown on LR silicon substrate.

In this work, the GaN HEMTs are designed and fabricated on an 8 inch ELR silicon substrate with a 2.5 mΩ cm resistivity, and the devices on the LR 60 Ω cm substrate are used as a comparison. Note that both wafers have an identical epi layer structure. We focus on design, fabrication, and analysis of GaN-on-ELR-Si substrate devices to investigate the possibility of using low resistivity silicon substrate for high frequency applications. The T-shape gate is employed by using the E-beam lithography to improve the intrinsic characteristics of the devices.[19–21] The ohmic contact is recessed to optimize the contact resistance.[22,23] The measured results for the show that the f_T and f_{max} up to 27 GHz and 71 GHz respectively for 2.5 mΩ cm substrate[14] and those are 44 GHz and 110 GHz respectively for the 60 Ω cm substrate. Also, the equivalent circuit model parameters are extracted for more in-depth analysis.

The preliminary results have been shown in the 2019 SSDM, and this paper further elaborates on the details of device fabrication and analysis.[14]

2. Experimental methods

2.1. GaN wafer preparation

The AlGaN/AlN/GaN HEMTs were grown on a 1000 μm thick 200 mm diameter P-type ELR Si substrate using MOCVD (provided by Global Wafers Co., Ltd.), as shown in Fig. 2. The wafer consists of a 5.5 μm Carbon doped layer for achieving highly resistive GaN buffers layers, followed by a 300 nm GaN channel and 1 nm AlN interlayer. Then,

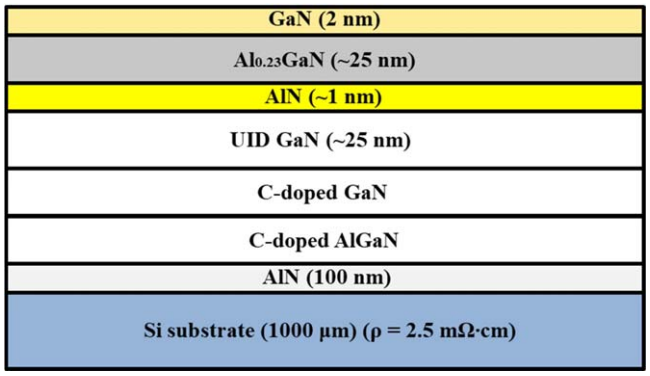


Fig. 2. (Color online) Cross-sectional view of the AlGaN/AlN/GaN HEMTs grown on the extremely-low resistivity silicon substrate.[14)]

a ~25 nm $Al_{0.23}GaN$ barrier layer was grown continuously. Finally, a 2 nm GaN layer is used to prevent aluminum from oxidizing on the AlGaN surface. The electron mobility and the sheet carrier concentration are over 1800 $cm^2 V^{-1}$ and 9×10^{12} cm^{-2}, respectively, which results in a 392 Ω/□ sheet resistance.[14)] Figure 3 shows the epitaxial quality of the optimized GaN epitaxial layer on an 8 inch ELR silicon substrate. As can be seen, there is no crack in the center, and the crack depth from the edge is only 1.2 mm. In addition, another set of experiments was performed on LR silicon substrates, which show the electron mobility and sheet carrier concentration about 1600 $cm^2 V^{-1}$ and 7×10^{12} cm^{-2}, respectively.

2.2. T-gate HEMTs fabrication

Different device geometrical parameters are used in our design to obtain optimized performance for the GaN-on-ELR-Si substrate HEMTs. The process of devices on both types of substrates was performed simultaneously to ensure the characteristic consistency for a fair comparison. The fabrication process started from mesa and used the Cl_3/BCl_3 mixed gas with an etching depth of approximately 150 nm by a reactive ion etching (RIE) system. After mesa isolation, the source/drain was recessed to a depth of 20 nm to reduce the ohmic contact resistance, and then Ti/Al/Ti/Au was deposited by thermal evaporation, followed by rapid thermal annealing at 800 °C for 30 s in N_2 ambient and lift-off process. The bilayer photoresist PMMA/copolymer was coated by an E-beam lithography system to define a T-shaped gate, followed by a Ni/Au (30/360 nm) deposition and lift-off process, as shown in Fig. 4. The sample was then immersed in dilute HCl: H_2O (1:8) for 50 s, followed by soaking in deionized water for 10 s. PECVD deposited a 25 nm SiN_X layer at 300 °C, and CHF_3/O_2 mixed gas RIE etching for via. Finally, the Ti/Au (30/400 nm) pad for RF measurements was deposited.[14)]

2.3. De-embedding and modeling

Figure 5 shows the high frequency small-signal equivalent circuit model, including the parasitic elements R_{sub} and C_{sub} introduced by the silicon substrate and buffer capacitance.[24)] The extrinsic C_{gsp} and C_{dsp} are parasitic capacitances introduced by the RF probing pads. Also, the parameters L_g, L_d and L_s, and R_g, R_d, and R_s are corresponding to the parasitics mainly from the metal interconnect and device fingers of the layout. The circuit in the red dashed box presents the intrinsic model of the device.

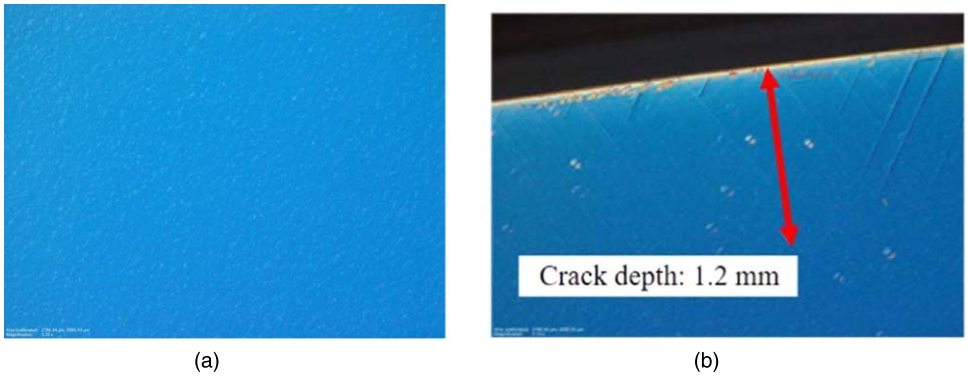
To obtain the extrinsic device characteristics, the Cold FET[25–27)] method is employed, which operates the devices under different bias voltages. As a result, the parasitic components can be extracted. For example, applying bias conditions about $V_{DS} = 0$ V and $V_{GS} \ll 0$ V makes devices work in the pinch-off, allowing neglecting the effect of parasitic resistances. The parasitic pad capacitances C_{gsp} and C_{dsp} can be obtained. Similarly, the parasitic resistances and inductors R_g, R_d, R_s, L_g, L_d, L_s can be extracted under $V_{DS} = 0$ V and $V_{GS} \gg 0$ V. The intrinsic characteristics of the component can be obtained by subtracting the external product-counting effect from the overall S-parameters.

Y-parameters transferred by the S-parameters can determine the elements of the intrinsic equivalent circuit model.[25)] Y-parameters can be derived from the equivalent model, and the mathematical expression of approximate model parameters can be extracted from the Y-parameters.

3. Results and discussion

3.1. DC characteristics

The DC *I–V* characteristics of the GaN HEMTs were measured by an Agilent B1500A semiconductor device analyzer. Figure 6 shows the DC I_D–V_{DS} and transconductance characteristics. The maximum drain current density ($I_{D,max}$) of 1.14 A mm^{-1} at $V_{GS} = 2.5$ V and a peak extrinsic $g_{m,max}$ of 247 mS mm^{-1} at $V_{GS} = -1$ V can be obtained for the device on the 2.5 mΩ cm substrate, as shown in Figs. 6(a) and 6(b).[14)] On the other hand, Figs. 6(c) and 6(d) present the DC characteristics of GaN HEMTs on 60 Ω cm Si substrate. A lower maximum drain current of 927 mA mm^{-1} at $V_G = 2.5$ V with a maximum transconductance of 206 mS mm^{-1} was observed.



(a) (b)

Fig. 3. (Color online) Epitaxial quality for ELR wafer: (a) the condition of cracking in the wafer center; (b) crack depth from the wafer edge.

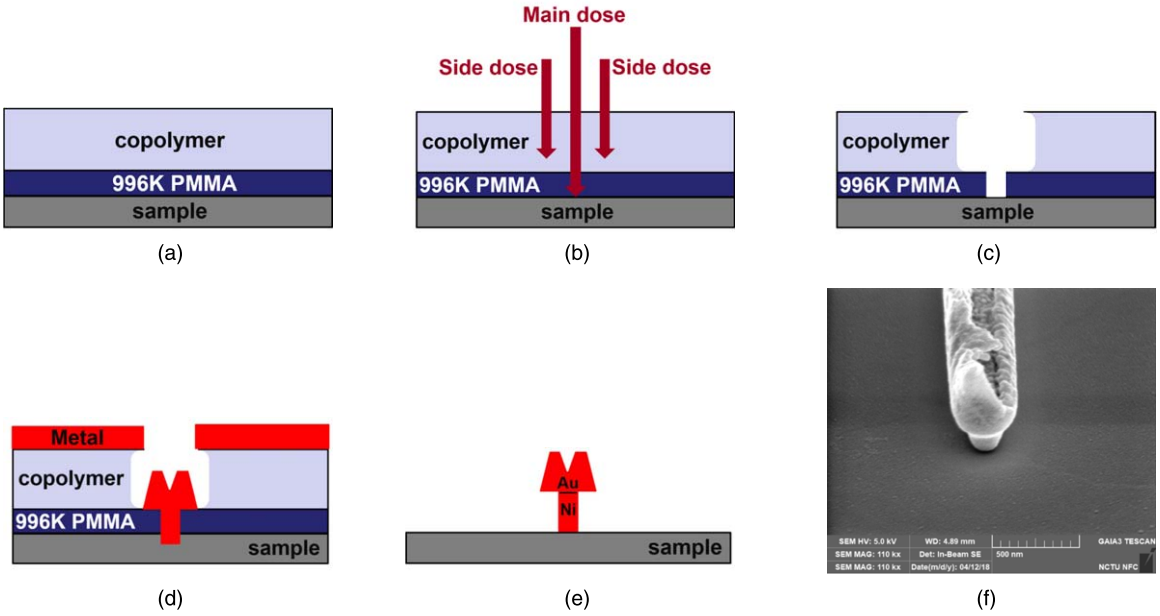


Fig. 4. (Color online) (a) Rotate coating copolymer/PMMA two-layer photoresist. (b) Define the gate line width with a high dose electron beam and widen the top line width with a low dose electron beam. (c) Top undercut structure formed after development. (d) Thermal evaporation of Ni/Au. (e) T-gate after metal lift-off. (f) SEM photo of T-gate.[14)]

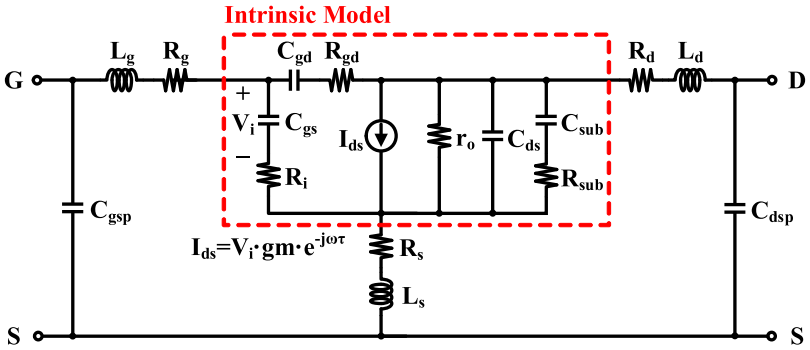


Fig. 5. (Color online) Small-signal equivalent circuit model at high frequencies of HEMT.

The better $I_{D,max}$ and $g_{m,max}$ of HEMTs on the ELR Si substrate can be mainly attributed to a better epitaxial quality compared with the LR case. According to the equations to calculate the maximum drain current and transconductance,[28,29)] the saturation carrier velocity v_s becomes the dominant parameter if comparing devices with the same structure and bias condition.[29,30)] With increased electron mobility and sheet carrier concentration in the ELR devices, the I_D and g_m are also higher than the LR devices as shown in Fig. 6. On the other hand, the gate leakage current I_G of HEMT on ELR Si substrate is higher than that of the LR one. Since the gate leakage current is highly dependent on the process of T-gate, which is difficult to be controlled in the laboratory processing environment. The results suggest that the leakage current in the reported devices are determined by the T-gate process variation, rather than the epilayer quality. As shown in Fig. 6, it should be pointed out that I_G is higher than I_D when $V_G < -4$ V (off state) indicating a higher source–gate leakage current I_{SG} than the drain-gate leakage current I_{DG}. Note that I_{SG} should be normally smaller than I_{DG} considering the much stronger E-field around the drain side,[31,32)] which is different from what we observed here. The possible reason could be the asymmetric gate–source (0.4 μm) and gate–drain (3 μm) distance in the proposed GaN devices. The gate–source E-field could be larger than that between gate and drain resulting in higher I_{SG} than I_{DG}. In addition, the smaller gate–source distance may degrade the surface passivation quality with the T-gate structure and create leaking paths, leading to higher leakage current.[33–36)] We can also see from the figures that the short channel effect is not obvious in the fabricated devices. Figure 6(b) shows a good pinch-off ($I_{on}/I_{off} \sim 3 \times 10^5$) which can be mainly attributed to the improved gate control over the channel by improving the aspect ratio between the gate length and the optimized AlGaN barrier thickness.[14)]

3.2. High-frequency characteristics

The small-signal high frequency measurements were performed using the Agilent N5245A PNA-X network analyzer, which was calibrated using the short-open-load-thru method. Figure 7(a) shows the f_T and f_{max} of GaN HEMTs on both types of substrates, obtained from the measured S-parameters in a frequency range from 1 to 50 GHz at the bias of $V_{GS} = -3.5$ V and $V_{DS} = 10$ V, respectively. With the de-embedding procedure of RF pad parasitics, the f_T and f_{max} of 27 GHz and 71 GHz are obtained by extrapolating with a slope of -20 dB/decade for the devices on the ELR substrate.[14)] In contrast, the devices on the LR substrate show f_T and f_{max} of 44 GHz and 110 GHz respectively under a bias

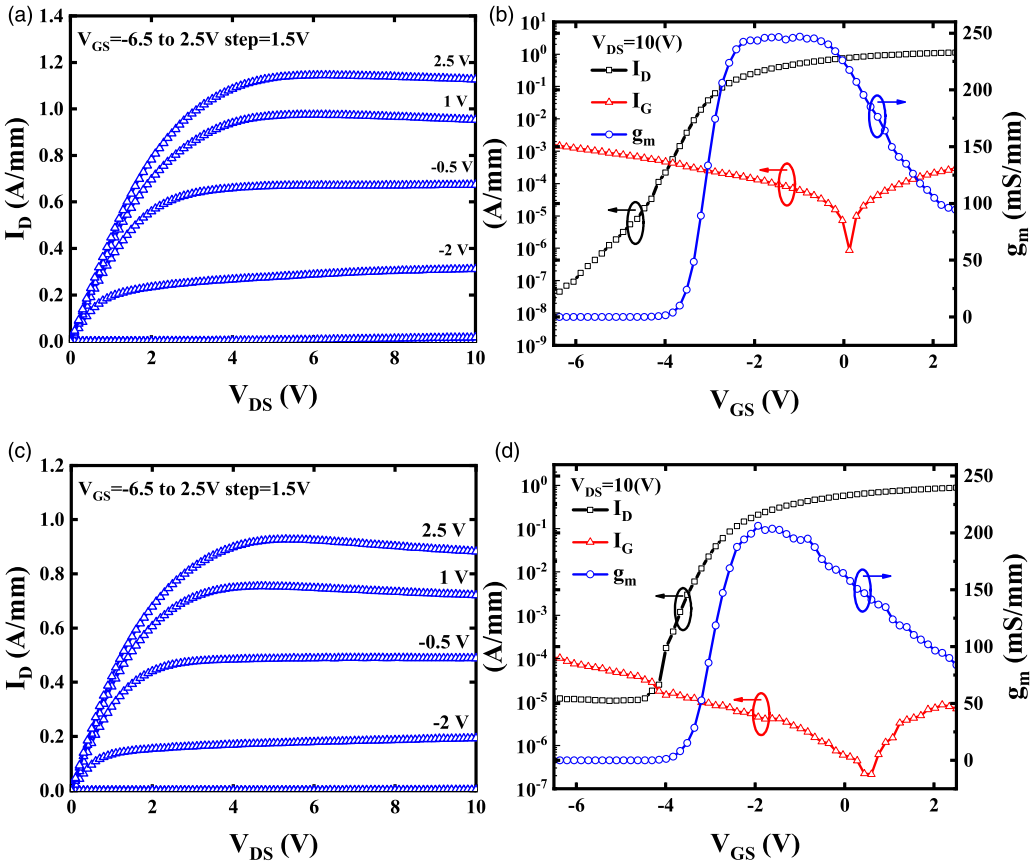


Fig. 6. (Color online) Measured results of GaN HEMTs: (a) I_D–V_{DS} characteristics with the 2.5 mΩ cm substrate;[14] (b) transfer characteristics at $V_{DS} = 10$ V with the 2.5 mΩ cm substrate;[14] (c) I_D–V_{DS} characteristics with the 60 Ω cm substrate; (d) transfer characteristics at $V_{DS} = 10$ V with the 60 Ω cm substrate.

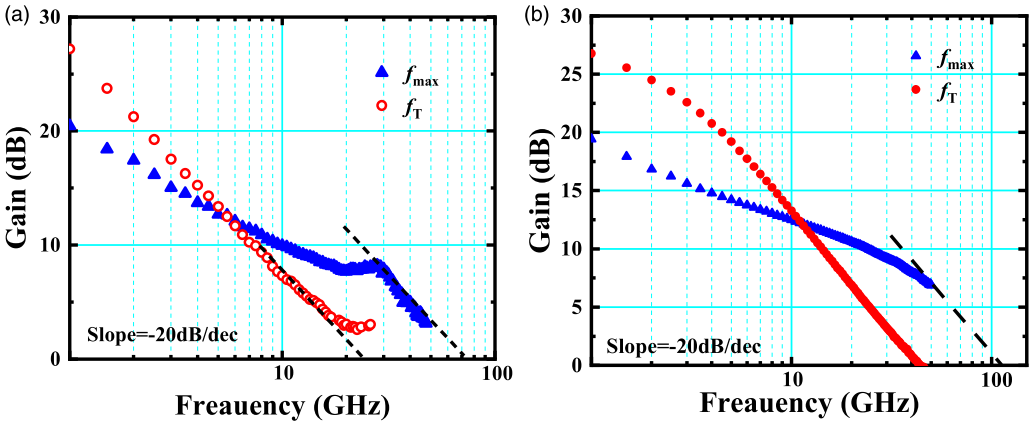


Fig. 7. (Color online) (a) Measured microwave characteristics of 2.5 mΩ mm substrate at $V_{DS} = 10$ V and $V_{GS} = -3.5$ V.[14] (b) Measured microwave characteristics of 60 Ω mm substrate at $V_{DS} = 10$ V and $V_{GS} = -2.5$ V.

of $V_{GS} = -2.5$ V and $V_{DS} = 10$ V. As can be seen, the devices on the ELR substrate show better DC characteristics in general. On the other hand, the devices on the LR have higher f_T and f_{max}. The results indicate that the impact of substrate parasitics on the device high frequency characteristics cannot be neglected. However, the devices can still operate in a range of tens of GHz with a thick and high-quality GaN buffer, which is sufficient for many RF applications.

3.3. Modeling

The intrinsic parameters extraction is implemented on Keysight Advanced Design System platform. The measured and the modeling results are plotted in the Smith Chart compared with the measured one, as shown in Fig. 8. A good agreement can be obtained between the measured and modeled results. The extracted R_{sub} is about 7.6 mΩ mm of HEMT on ELR substrate while 16 Ω mm of the other one and C_{sub} of HEMTs on ELR and LR substrates are 9.5 fF mm^{-1} and 10 fF mm^{-1}, respectively. In our previous work, we found that the frequency response is sensitive to C_{sub} if R_{sub} is relatively small,[8] which agrees well with the degradation of high frequency characteristics of HEMTs on ELR Si. The parasitics exist at the interface between substrate and GaN result in an RC pole resulting in degraded f_{max}.[37]

4. Conclusions

In this paper, the AlGaN/GaN HEMTs with a 0.1 μm T-shaped gate on an extremely LR silicon substrate (2.5 mΩ

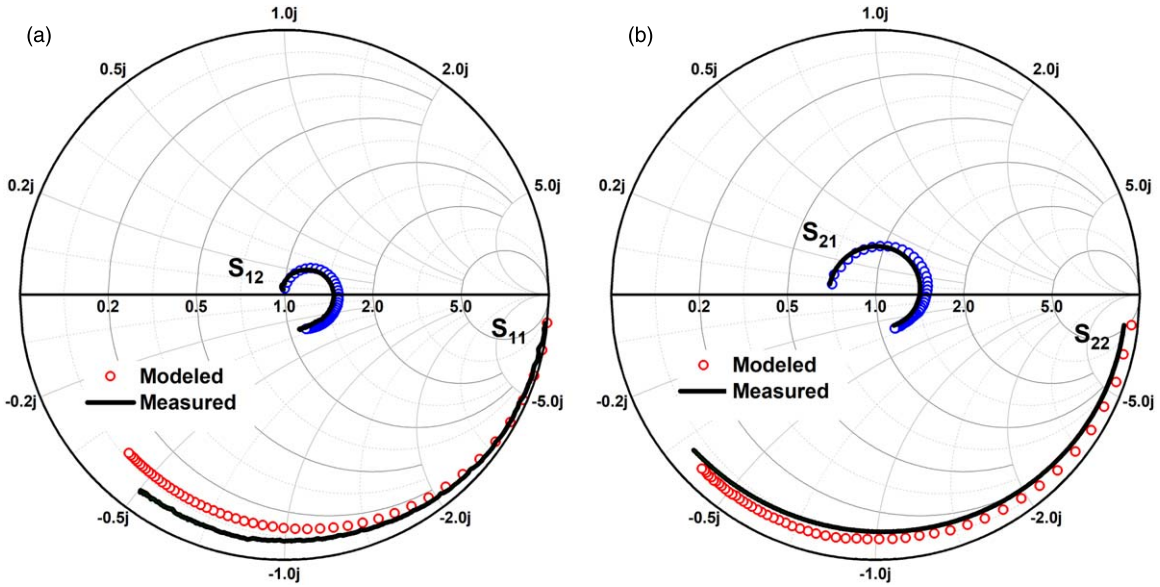


Fig. 8. (Color online) Measured and modeled frequency response of the fabricated GaN HEMT at $V_{DS} = 10$ V and $V_{GS} = -3.5$ V. The extracted f_T and f_{max} are 27 GHz and 71 GHz, respectively.[14)]

cm) were demonstrated. The obtained current gain cutoff frequency f_T, the maximum oscillation frequency f_{max}, and the maximum extrinsic transconductance $g_{m,max}$ were 27 GHz, 71 GHz, and 247 mS mm^{-1}, respectively.[14)] The results obtained from the devices on the LR substrate (60 Ω cm) suggested that ELR Si substrate results in a better epilayer quality, and the effect of substrate parasitics cannot be neglected. However, the obtained device characteristics still showed a high potential of using GaN on the ELR silicon substrate for 5 G applications.

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