Japanese Journal of Applied Physics
Vol. 46, No. 2, 2007, pp. 478–484

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# Impacts of Gate Recess and Passivation on AlGaN/GaN High Electron Mobility Transistors

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(Received June 11, 2006; revised November 3, 2006; accepted November 14, 2006; published online February 8, 2007)

In this study, the impacts of gate recess and passivation on AlGaN/GaN high electron mobility transistors (HEMTs) were investigated. The trap-related characteristics were studied in detail by several different measurements including dc current–voltage, current collapse, gate lag, and flicker noise characterizations. With a $Cl_2$/Ar-recessed gate, drain current collapse factors ($\Delta I_{max}$) of ~37.5 and ~6.9% were observed before and after SiN passivation. The gate lag measurements showed that the lagging phenomena almost disappear with SiN passivation for both $Cl_2$- and $Cl_2$/Ar-recessed devices. However, the flicker noise measurements revealed distinct noise levels of devices with different processes even after passivation. As the gate voltage ($V_G$) changed from 2 to $-4$ V, the devices recessed by $Cl_2$ exhibited lower drain noise current densities ($S_{ID}/I_D^2$ ranging from $2.8 \times 10^{-14}$ to $1.7 \times 10^{-12}$ Hz$^{-1}$ at 1 kHz) than those etched by $Cl_2$/Ar mixture gas ($S_{ID}/I_D^2$ ranging from $6.3 \times 10^{-14}$ to $6.0 \times 10^{-12}$ Hz$^{-1}$ at 1 kHz), whereas the devices without the recess process showed the lowest noise levels ($S_{ID}/I_D^2$ ranging from $2.8 \times 10^{-15}$ to $1.3 \times 10^{-13}$ Hz$^{-1}$ at 1 kHz). It was found that $S_{ID}/I_D^2$ increased monotonically when $V_G$ changed from 2 to $-4$ V. A bias dependence of the $1/f^{\gamma}$ slope $\gamma$ was observed, and a relatively large variation in the range of ~1.1 to 1.6 was found for devices recessed by $Cl_2$/Ar mixture gas. The number fluctuation model was employed to explain the observed trends. The results also indicated that the surface traps play an important role in these devices.
[DOI: 10.1143/JJAP.46.478]

KEYWORDS: gate recess, passivation, GaN, HEMT, current collapse, flicker noise

## 1. Introduction

GaN, due to its unique material properties, such as wide band gap (3.4 eV at room temperature), high breakdown field (~3 MV/cm), high electron saturation velocity (~$3 \times 10^7$ cm/s), excellent thermal stability, and strong polarization, has wide applications in optoelectronics and electronics. In addition to the well-known optoelectronic applications of light-emitting diodes (LEDs) displays and high-density optical storage, GaN-based electronic devices are also excellent candidates for RF wireless base stations, wireless broadband access, power supplies, motor controls, and automotive electronics. For RF high-power applications, the advantages of the high-power density (>10 W/mm) and high efficiency (>60%) of GaN-based high electron mobility transistors (HEMTs) enable a simpler power amplifier (PA) module design and a more compact device size to be realized, as compared with conventional Si-based and GaAs-based RF power transistors.[1] For high-power electronics applications, the high current density, low on resistance, and high breakdown voltage of GaN-based power devices can also result in an even better performance than conventional Si-based and SiC-based power devices.

For the development of GaN-based high-power HEMTs, one of the most critical issues is the understanding and control of the device surface condition, since the device performance is very sensitive to surface treatments. Studies have been performed on the degradation problem of GaN HEMTs.[2–10] Several mechanisms, involving the surface states,[2–5] the induced strain,[6,7] and the edge trapping caused by hot electrons,[8–10] have been proposed to explain the possible origins of the device degradation phenomena.

However, most of these studies focused on AlGaN/GaN HEMTs without gate recess etching. For RF applications with a recessed-gate structure, a better gate control capability of the channel carriers can be obtained to enhance the device performance. On the other hand, the recessed-gate process can also degrade the flicker noise characteristics due to the induced damage during the process, which is critical for RF circuit applications such as voltage-control oscillators (VCOs) and mixers.[11] Recently, the development of GaN power devices for automotive electronics application has led to a strong requirement for a normally-off operation to simplify the power circuits.[12] In particular, recess etching is a critical step to realize such an operation. Thus, the characterization and damage recovery of a recessed gate are of great importance for many applications in a wide frequency range. In this work, GaN HEMTs with different recess etching treatments, including $Cl_2$ plasma and $Cl_2$/Ar plasma etching, were fabricated and compared with non recessed devices. Devices with SiN passivation treatment were also compared with unpassivated devices. In addition, several different measurement techniques were used to systematically investigate the impact of surface traps on the device characteristics, including current collapse, gate lag and flicker noise measurements. These measurements provide powerful tools to investigate the traps in the devices and also useful information to further improve the gate-recess and passivation processes for GaN HEMTs.

## 2. Device Structures and Fabrication

The device structures were grown on c-plane sapphire substrates by metal-organic chemical vapor deposition (MOCVD). The epitaxial structure consisted of a GaN buffer layer, a 3 μm undoped GaN layer, and a 35 nm AlGaN barrier layer, as shown in Fig. 1. The Al mole fraction in the AlGaN layer was 0.3. Hall measurement with Van Der Pauw geometry was performed to characterize the electrical properties of the two-dimensional electron gas (2DEG) at room temperature. The room temperature electron concentration and mobility of 2DEG are $1.09 \times 10^{13}$ cm$^{-2}$ and 1470 cm$^2$/(V·s), respectively. Device isolation was achieved using the inductively-coupled plasma (ICP) etching with a $Cl_2$/Ar gas mixture. The source/drain

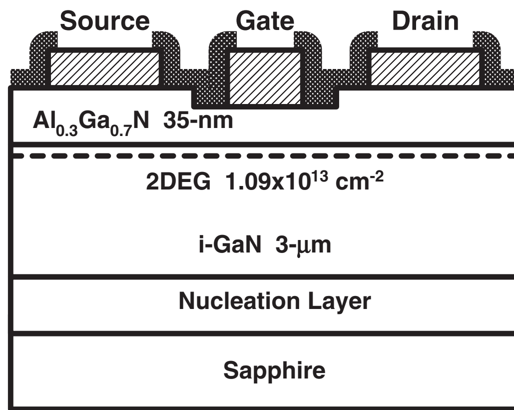



Fig. 1. Device structure of AlGaN/GaN HEMTs in this study.

ohmic contacts were formed by Ti/Al/Ti/Au deposition and rapid thermal annealing at 750 °C for 30 s in $N_2$ ambient. After fabrication of the ohmic contacts, two recess etching processes were performed for comparison with the non recessed devices: 1) pure $Cl_2$ gas (50 sccm) with 5 W RF power for 60 s, and 2) $Cl_2$/Ar mixture gas (50/20 sccm) with 10 W RF power for 30 s. The etching depths obtained by capacitance–voltage ($C$–$V$) profiling are ~50 and 80 Å for the two processes, respectively. After recess etching, no additional thermal annealing step was performed. A SiN layer about 100 nm thick was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C for passivation. The devices studied here have a gate length of 1 μm and a gate width of 50 μm, and show a good RF performance of $f_T > 12$ GHz, and $f_{max} > 20$ GHz.

## 3. Characterization Setups

In addition to conventional $I$–$V$ measurements, three different techniques were also employed to investigate the trap-related characteristics of AlGaN/GaN HEMTs in this study, namely, the current collapse, the gate lag, and the low-frequency noise measurements. Using these three techniques, the transient and frequency responses of the traps in the devices under different processing conditions were observed successfully. The details will be discussed in §4.

The current collapse measurement of the device was performed under the sweep of a 60 Hz rectified sine wave using a Tektronix 370 curve tracer. The response of the traps can be probed by the slowly changing signal, and the impact of the surface traps on the recessed gate can be observed in the $I$–$V$ characteristics of the devices.

The measurement setup for gate lag is shown in Fig. 2(a). The gate pulse voltage was biased from −8 to 0 V using a HP8114 pulse generator. The period and the duty cycle of the gate pulse voltage used were 1 s and 50%, respectively. The drain voltage of the device was biased at 5 V using a DC power supply. The source side of the device was connected with a resistor of 20 Ω to sample the output voltage. The voltage difference between the two terminals of the resistor was monitored using an oscilloscope.

The low-frequency noise measurement setup and procedure in this study were similar to those in the previous study reported by the authors.[13] Figure 2(b) shows the schematics of the flicker noise measurement system. A low-noise preamplifier with a background noise on the order of $6.4 \times 10^{-21}$ $V^2$/Hz was employed to amplify the drain noise voltage of the devices. Low-loss RF cables with excellent ground shielding were used to transmit the signal. In addition, RF ground-signal-ground probes were used for on-wafer measurements to eliminate the oscillation problems in the microwave devices. The entire system was enclosed in a shielding box to prevent interference from the environment. Moreover, high-capacity batteries were used for DC power supply to provide a stable bias source. The measured frequency range was from 10 to 100 kHz.

## 4. Results and Discussion

### 4.1 DC current–voltage characteristics

Compared with $Cl_2$ plasma, $Cl_2$/Ar plasma resulted in a more stable recess etching process. Based on our experiments, $Cl_2$ plasma only reached a limited etching depth, whereas $Cl_2$/Ar plasma had a stable etching rate, which may be attributed to the more effective bond breaking and desorption of etching by-products. However, the additional Ar resulted in larger process damage due to a more physical etching mechanism. Before passivation, the device without recess etching showed a drain current of ~37 mA at $V_{gs} = 1$ V, whereas the device treated with $Cl_2$ plasma had a lower drain current of 31 mA. In addition, the device with $Cl_2$/Ar plasma recess etching showed a much lower drain current of 17.5 mA at the same gate bias. The results suggest that $Cl_2$/Ar plasma is a more effective etching approach for gate recess in GaN HEMTs. However, the resulting drain current reduction is more noticeable due to the process damage. More discussion will be carried out later on the basis of the results of the different measurement techniques.

### 4.2 Current collapse characteristics

The measurement results of current collapse with various $V_d$ sweeps are shown in Fig. 3. In this study, we define the collapse factor, $\Delta I_{max}$, as the ratio of the decreased maximum drain current with a $V_d$ sweep of 16 V to the maximum drain current with a $V_d$ sweep of 8 V. Before SiN passivation, the non recessed device showed a clear current collapse as the drain bias increased, $\Delta I_{max} \sim 8.7\%$ [Fig. 3(a)], suggesting the existence of defects in the device. Compared with the non recessed device, the $Cl_2$-recessed and the $Cl_2$/Ar-recessed devices showed even larger current reductions as the drain bias increased [Figs. 3(b) and 3(c)]. The collapse factors $\Delta I_{max}$ are ~25 and 37.5% for $Cl_2$-recessed and $Cl_2$/Ar-recessed devices, respectively. The $Cl_2$/Ar-recessed device showed the most severe current reduction among all devices. These results indicate that the recess etching process introduces additional surface damage and traps leading to a more significant current collapse characteristic. For the $Cl_2$/Ar-recessed device, oweing to the physical ion bombardment of Ar ions and also the higher RF power applied, more etching damage was introduced than for the $Cl_2$-recessed device.

After SiN passivation, recovery in the drain current can be clearly observed for all devices, as shown in Fig. 4. The collapse factors $\Delta I_{max}$ are reduced to 6.7, 8.9, and 6.9% for non recessed, $Cl_2$-recessed, and $Cl_2$/Ar-recessed devices, respectively. For the $Cl_2$-recessed device, the collapse factor

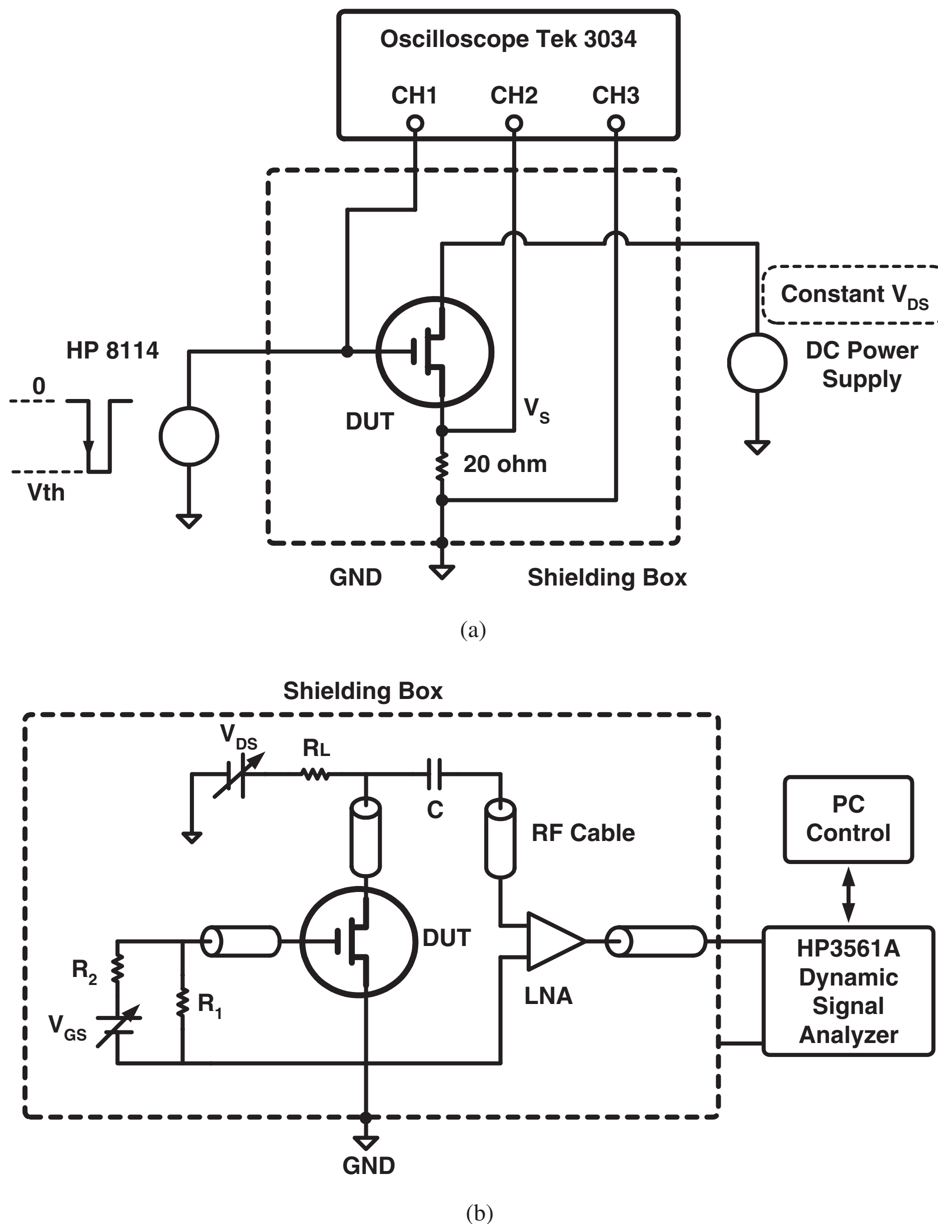



Fig. 2. Setups of (a) gate lag measurement, (b) flicker noise measurement.

reduces from 25 to 8.9%, whereas for the $Cl_2$/Ar-recessed device the collapse factor reduces from 37.5 to 6.9%. Additionally, after SiN passivation, both the $Cl_2$-recessed and $Cl_2$/Ar-recessed devices showed comparable collapse factors to the non recessed devices. Therefore, these results suggest that most of the etching damage caused by the recess etching was eliminated by the SiN passivation treatment. On the other hand, although the collapse factor was reduced to a level below 10% for all passivated devices, the current collapse phenomenon still occurred and could not be removed completely, which suggests that the surface traps were not completely eliminated. To further study the trap-related characteristics of these devices, the gate lag and flicker noise measurements were also performed to reveal more about the impacts of the gate recess and passivation on the devices.

*4.3 Gate lag characteristics*

The measured gate lag results are shown in Fig. 5. As can be seen, the drain current slowly responded to the gate pulse signal, and gradually increased and saturated, where a drain current lag within this time period was observed. In this work, we define the gate lag as the ratio of the drain current lag ($\Delta I$) to the maximum saturation drain current ($I_{max}$). Before SiN passivation, the non recessed device showed a very long gate lag of greater than 1 s [Fig. 5(a)], which is similar to the results published in ref. 4. The result indicates that some defects already exist on the surface, which is consistent with the current collapse measurements. Gate lag *w* also observed for the $Cl_2$-recessed [Fig. 5(b)] and $Cl_2$/Ar-recessed [Fig. 5(c)] devices. Compared with the non recessed device, both the $Cl_2$-recessed and $Cl_2$/Ar-recessed devices showed even more apparent gate lag degradation. In particular, the $Cl_2$/Ar-recessed device showed the most serious drain current degradation and the slowest current response among all devices. The degradation phenomena observed in the gate lag measurement is basically consistent with that in the current collapse measurement, which can be

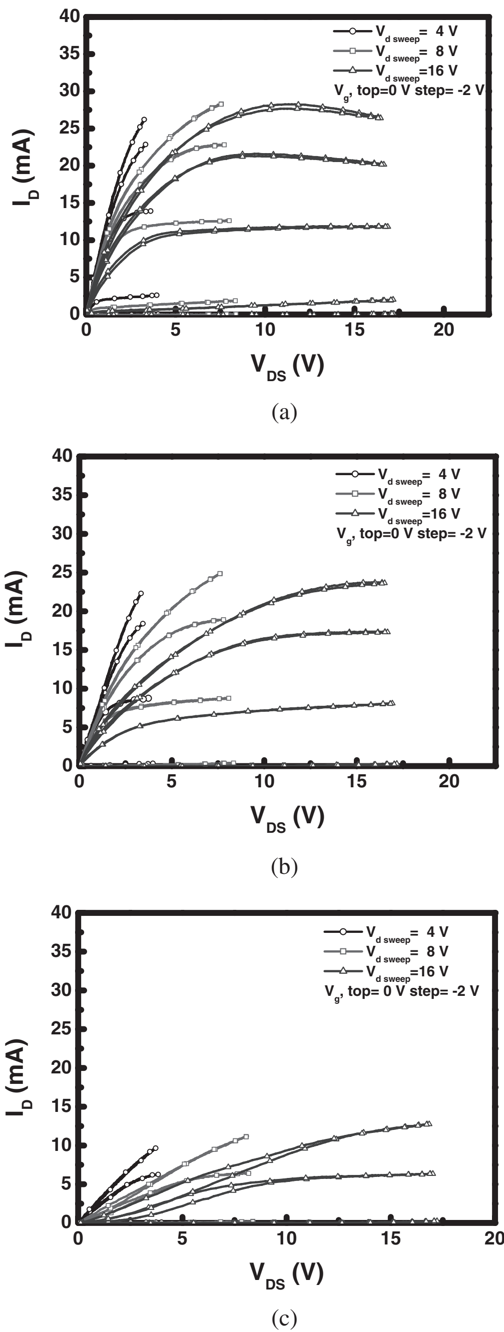



Fig. 3. Current collapse measurement results for (a) non recessed, (b) $Cl_2$-recessed, and (c) $Cl_2/Ar$-recessed AlGaN/GaN HEMTs without the SiN passivation.

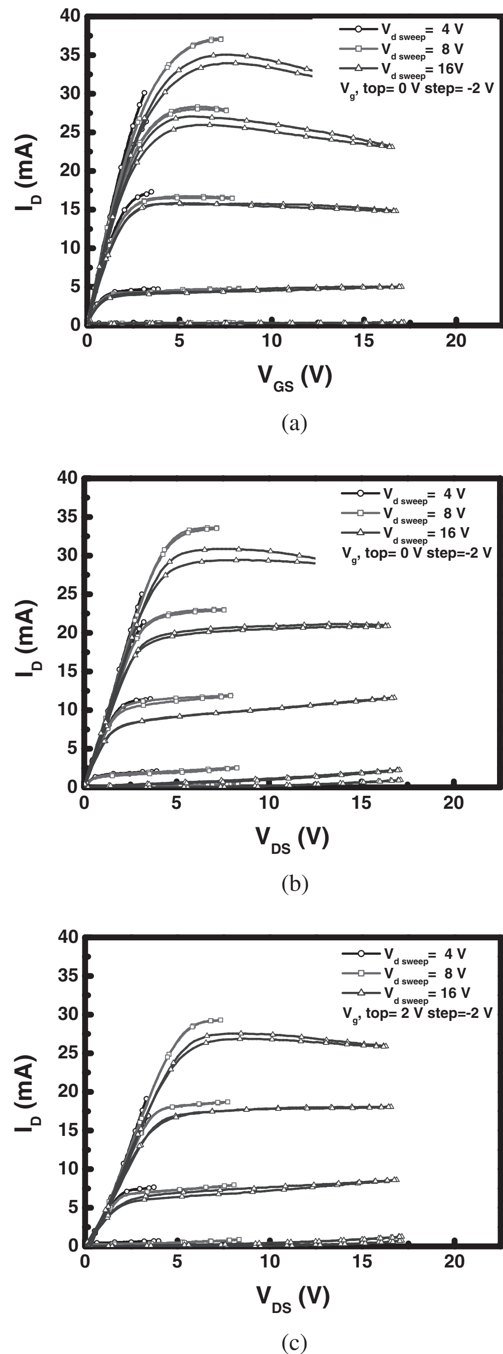
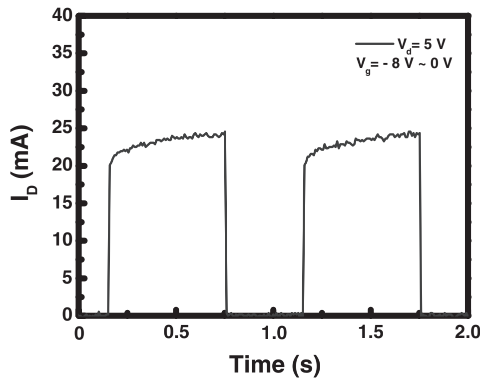



Fig. 4. Current collapse measurement results for (a) non-recessed, (b) $Cl_2$-recessed, and (c) $Cl_2/Ar$-recessed AlGaN/GaN HEMTs with SiN passivation.

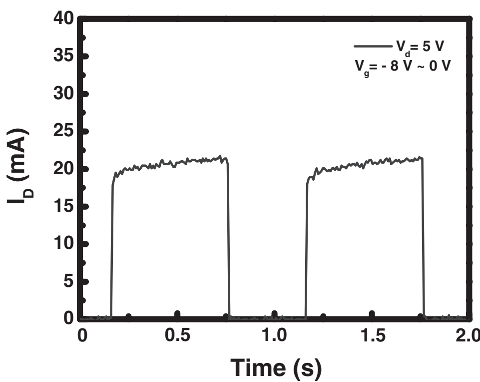
attributed to the physical ion bombardment of Ar ions and the higher RF power applied during the etching process.

After SiN passivation, none of the three devices exhibited apparent gate transient ($\Delta I/I_{\max} \sim 0$) under the same time scale, and thus clear drain current recovery was observed for all devices, as shown in Fig. 6. The $Cl_2$-recessed and $Cl_2/Ar$-recessed devices did not show a clear drain current lag, which indicates that most etching damage was eliminated by SiN passivation. These gate lag results are also in good agreement with the current collapse results.

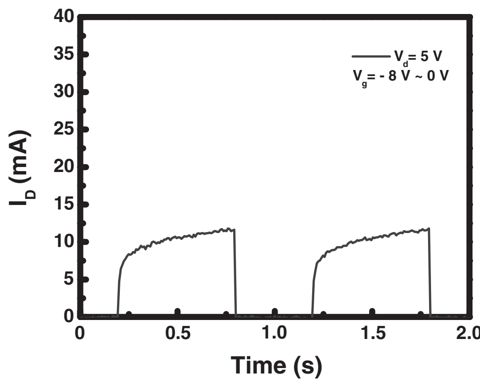
From the above results, it can be concluded that SiN passivation can improve the current collapse and gate lag degradation. Possible mechanisms have been reported, which are generally attributed to the elimination of the surface states and/or traps, or the induced strain mechanisms.[2–7] The surface trapping states are generally assumed to be associated with surface states created by dangling bonds, threading dislocations, or the polarization charge accessible at the AlGaN surface. It is also possible that the hard SiN film can modify the surface stress and thus recover the collapse degradation. Assuming a similar strain is applied on the surface of the devices after SiN passivation, the effect on the drain current should be close for both the non recessed and recessed devices. In this study, for the non recessed device, only a small improvement was obtained after SiN passivation. However, for the devices with $Cl_2$ or $Cl_2/Ar$ plasma recess treatment, SiN passivation greatly




(a)

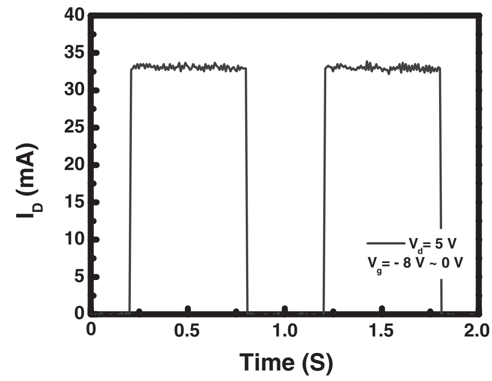



(b)

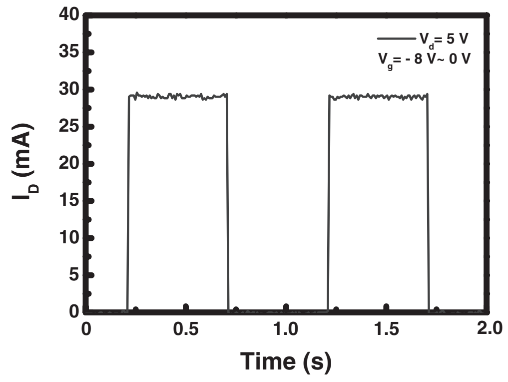



(c)

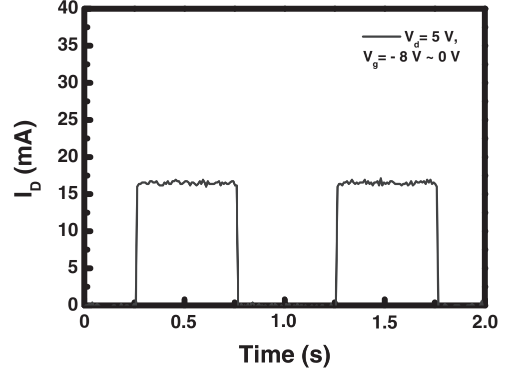
Fig. 5. Gate lag measurement results for (a) non recessed, (b) $Cl_2$-recessed, and (c) $Cl_2$/Ar-recessed AlGaN/GaN HEMTs without the SiN passivation.




(a)




(b)




(c)

Fig. 6. Gate lag measurement results for (a) non recessed, (b) $Cl_2$-recessed, and (c) $Cl_2$/Ar-recessed AlGaN/GaN HEMTs with SiN passivation.

improves their current collapse degradation. Therefore, the results suggest that the reduction and recovery of the surface traps are most likely the predominant mechanisms for the collapse suppression after SiN passivation.

### 4.4 *Flicker noise characteristics*

As discussed in §4.2 and §4.3, the trap-related phenomena were investigated by transient response (time-domain) measurement techniques. In this part, flicker noise measurements were performed in the frequency domain to further study the surface defects in AlGaN/GaN HEMTs. The correlation between the measured results from the different techniques will also be discussed. The flicker noise measurements were performed on the devices with SiN passivation. The gate terminal was AC short-circuited and the drain-current-noise spectral density was measured. The measured noise levels were well above the background noise of the measurement system. A fixed drain bias of 8 V was applied, and the gate bias was varied from −4 to 2 V.

Figures 7 and 8 show the normalized flicker noise characteristics for the non recessed and $Cl_2$-recessed devices, respectively. The results indicate that the noise level after the recess process increases by about one order of magnitude even with passivation. In addition, an increase of about two orders of magnitude was observed for the $Cl_2$/Ar-recessed device, as shown in Fig. 9. The results can be attributed to the increased number of surface states due to the recess process. Also, the more significantly increased noise level caused by the $Cl_2$/Ar etching process may also

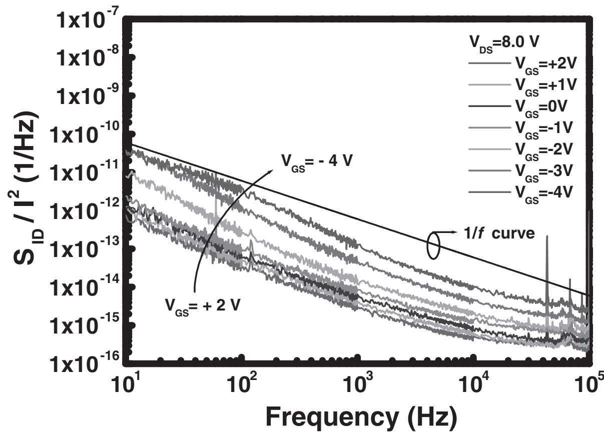



Fig. 7. Normalized drain current noise spectral density for non recessed AlGaN/GaN HEMTs as $V_{GS}$ changes from −4 to +2 V with a fixed drain bias of 8 V.

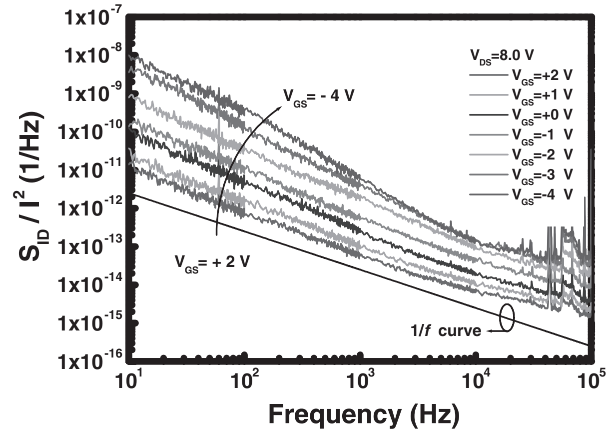



Fig. 9. Normalized drain current noise spectral density for $Cl_2$/Ar-recessed AlGaN/GaN HEMTs as $V_{GS}$ changes from −4 to +2 V with a fixed drain bias of 8 V.

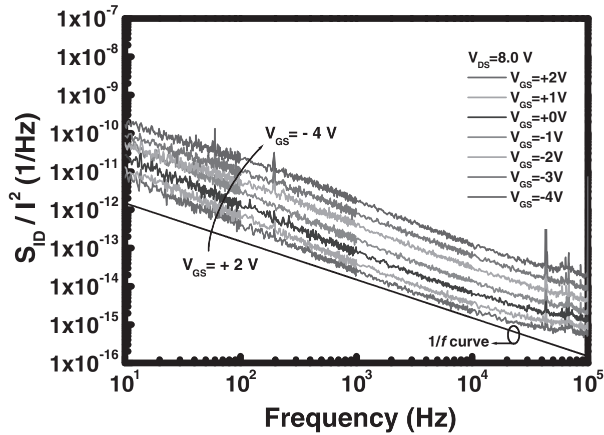



Fig. 8. Normalized drain current noise spectral density for $Cl_2$-recessed AlGaN/GaN HEMTs as $V_{GS}$ changes from −4 to +2 V with a fixed drain bias of 8 V.

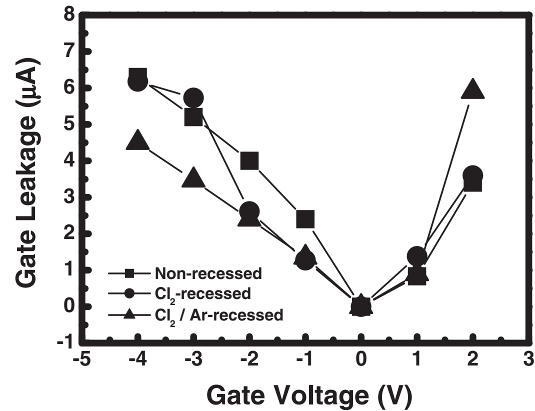



Fig. 10. Gate leakage current as a function of the gate bias from −4 to +2 V.

result from the higher RF power used and also the more physical etching process of the $Cl_2$/Ar mixture than that using $Cl_2$ only. The results shown are consistent with the previously discussed current collapse and gate lag measurements.

The results also indicate that $S_{ID}/I_D^2$ increased monotonically when the gate bias was reduced from 2 to −4 V, as shown in Figs. 7–9. Note that even though a distinct difference is observed for noise levels, the monotonically reducing $S_{ID}/I_D^2$ is consistent for the three types of devices. Various reasons have been given to explain this observed trend such as gate leakage current, screening effect, and the surface/interface states.[14–16] To further distinguish between these noise mechanisms, the gate current was measured. Figure 10 shows the leakage current under different gate voltages. As can be seen, $I_G$ showed a minimum value at $V_G$ of around 0 V, which does not agree with the monotonically changing $S_{ID}/I_D^2$ levels. The results indicate that $S_{ID}/I_D^2$ of the devices studied here is not predominated by $I_G$, which is different from previously reported results.[16,17] Not only the noise magnitudes but also the slopes of $1/f^{\gamma}$ varied under different bias conditions. For example, the $Cl_2$/Ar-recessed devices show a large variation of $\gamma$ in the range of ~1.1 to 1.6 compared with the other two types of devices (range from ~1.2 to 1.4). Note that the theoretical value of $\gamma$ is one under the assumption of uniformly distributed traps.[18] In practice, it has been reported that $\gamma$ of AlGaN/GaN HEMTs was in a range of ~1.0 to 1.3.[15] Detailed discussion on $\gamma$ of the studied devices will be given later.

In this study, the number fluctuation ($\Delta N$) model is adapted to explain the observed flicker noise characteristics. The tunneling time of carriers to the traps can be described as:[18]

$$\tau_t = t_0 \cdot \exp(\alpha_t \cdot x_i), \tag{1}$$

where $t_0$ is the tunneling time constant, $\alpha_t$ is the McWhorter tunneling parameter, and $x_i$ is the tunneling distance. Based on this model, a gate-bias dependence of the drain current noise spectral density can be expected. The monotonically increasing noise level when $V_G$ becomes more negative can be attributed to the decreased total channel carriers as the device is biased toward pinch-off. As a result, the three devices present a similar trend of $V_G$ dependence, even with substantially different noise levels.

This model can also explain the observed $\gamma$ variation. Under the $\Delta N$ framework, because the tunneling distance and trap energy are non uniformly distributed, $\gamma$ is larger

than one if the trap density increases toward the surface.[18) ] As shown in Fig. 9, $\gamma$ increases from $\sim$1.1 at $V_G$ of 2 V to $\sim$1.6 at a the gate bias of $-4$ V. The $\gamma$ values of the devices with different gate processes, as shown in the figures, are also above one under various bias conditions. The results suggest that higher trap densities exist toward the surface in these devices. Also observed in the $Cl_2$/Ar-recessed devices, the increases in noise level and $\gamma$ are relatively larger than those of the other two types of devices as $V_G$ changed, which can be attributed to the deeper etching depth and the larger amount of surface traps. As a result, the carrier tunneling procedure becomes more sensitive to the gate-voltage-induced distribution variation in tunneling distance and trap energy. The increased $\gamma$ also implies increased effective tunneling distances with a more negative gate bias due to the change in the band profile. In other words, the low-frequency transitions are emphasized, and the $\gamma$ value increases.

From the measured trap-related phenomena, the origin of current collapse, gate lag, and low-frequency noise can mainly be attributed to the surface defects in GaN HEMTs. All measurements indicate that the recess etching process with $Cl_2$/Ar resulted in a more severe damage on the device surface. In addition, SiN passivation effectively removed the surface defects, as can be observed from the current collapse and gate lag measurements. However, the flicker noise levels of the devices with the three processes showed distinct differences even after SiN passivation. The results suggest that flicker noise can be employed as a more sensitive tool for trap analysis compared with the other two approaches.

Finally, one issue that should be pointed out is the activation energy of the traps. The trap activation energy ($E_a$) in AlGaN/GaN HEMTs can be further investigated by performing the deep-level transient current spectroscopy (DLTS) measurement. According to previous studies,[5,19)] $E_a$ shows values of 0.29, 0.61, and 0.55 eV in ref. 19, and 1.434 and 1.427 eV in ref. 5. The results suggest that $E_a$ has a very wide distribution, which may be attributed to the variations of the device process and material quality. In addition, previous reports showed a reduction of DLTS signal peak intensity after SiN passivation, which is an indication of the reduced trap density. In this study, although the DLTS measurements were not performed, the gate lag and current collapse measurements show consistent results with the previously reported studies for the devices with and without SiN passivation. Moreover, the DLTS results show that even with passivation, the traps cannot be removed completely, which is also consistent with our findings from different measurements.

## 5. Conclusions

The impacts of gate recess and passivation on GaN HEMTs were investigated by several different trap-related measurement techniques. A reduction in the device drain current was clearly observed for the devices with $Cl_2$ and $Cl_2$/Ar recess treatments. The current collapse and gate lag measurements indicated that the amount of traps increased markedly after the gate recess process, particularly for the device recessed by $Cl_2$/Ar mixture gas. and can be effectively reduced by SiN passivation. In addition, the predominant origin of the flicker noise is not the gate leakage, but the surface states in the passivated devices. The recessed-gate devices had higher noise densities by at least one order of magnitude than those without the recess process due to the increased number of surface traps even after SiN passivation. The monotonically increasing $S_{ID}/I_D{}^2$ as devices were biased toward pinch-off and the variation in slope $\gamma$ of the $1/f^\gamma$ characteristics were explained by using the carrier number fluctuation model, which also suggested that the trap density increases toward the device surface.

**Acknowledgement**

The authors would like to thank the assistance of Nano Facility Center, National Chiao Tung University. This work was supported in part by the National Science Council under contract No. NSC 94-2215-E-007-005.

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