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Electro-Static Discharge Protection Design for V-Band Low-Noise Amplifier Using Radio Frequency Junction Varactor

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The RF junction varactors are employed as electro-static discharge (ESD) protection devices and co-designed with 60 GHz low-noise amplifier (LNA) fabricated in a 65-nm CMOS technology. The junction varactor acts as an ESD diode to bypass ESD current during ESD zapping, and also utilized as a capacitor to be a part of input matching network of the LNA in normal RF operation. By transmission line pulse (TLP) measurement, the ESD protection capabilities of RF junction varactors are characterized with different device parameters. The experimental results demonstrate excellent second breakdown currents (I_{t2}) and high ratios of the ESD levels to parasitic capacitances (V_{ESD}/C_{ESD}). With ESD/matching co-design methodology, the ESD-protected LNA demonstrates a second breakdown current I_{t2} of 1.4 A, corresponding to a 2-kV human-body-model (HBM) ESD protection level with a noise figure (NF) of 6.6 dB and a peak gain of 16.5 dB at 60 GHz under a power consumption of only 28 mW.

1. Introduction

As technology scaling down, the CMOS process featuring impressive f_T and low-power consumption becomes the best candidate for fully-integrated RF transceivers.[1–6] Electro-static discharge (ESD) protection is one of the most important reliability concerns in RFICs, especially for the advanced technology node with high operating frequencies.[6–10] Because the reduced gate oxide thickness and hence lowered gate oxide breakdown voltage, the device is more sensitive to ESD-induced damage.[10] Figure 1 shows the circuit blocks of a typical RF receiver with the ESD protection block. Assuming the noise contribution from the circuit blocks after the mixer can be neglected, the system noise figure can be calculated as $F_{System} = F_{ESD} + F_{LNA} + (F_{Mixer} - 1)/G_{LNA}$, where F_{System}, F_{ESD}, F_{LNA}, and F_{Mixer} represent the noise figure (NF) of the system and the individual blocks, respectively, and G_{LNA} is the power gain of the low-noise amplifier (LNA). It should be emphasized that F_{ESD} is equivalent to the loss introduced by the ESD block, and is directly added into the system noise figure.

Several conventional ESD diodes [shallow-trench isolation diode, poly-bounded diode, and local oxide of silicon (LOCOS) diode] and silicon controlled rectifier (SCR) based ESD devices,[7,8] were reported and widely used in on-chip ESD protection. However, the main issue is associated with the impact of the ESD diode on the core RF circuits (LNA) for high frequency design such as 60 GHz applications.[9] Differing from previous works,[7–9] an RF junction varactor utilized as ESD protection device is adopted in this work. Compared to the conventional ESD diodes and SCR-based ESD devices, the RF junction varactor has the advantages of simple layout, reduced parasitics, and scaleable RF model provided in foundry process design kits (PDKs), which is suitable for co-designing ESD and LNA circuits. By co-designed methodology, the ESD devices using RF junction varactors are performed as a part of input matching network of the 60-GHz LNA, which optimize RF and ESD performances simultaneously. By characterizing with transmission line pulse (TLP) measurements, the optimized geometry of the junction varactor ($L = 0.15\,\mu m$, $W = 2\,\mu m$, and $N = 25$) achieves the best figure-of-merit ($FOM = V_{ESD}/C_{ESD}$) up to 98.1 kV/fF. The obtained RF junction varactors are then employed to realize an ESD-protected LNA at 60 GHz (V-band). The ESD-protected LNA demonstrates a 1.4-A TLP current level, corresponding to a 2-kV human-body-model (HBM) ESD protection level. Also, the LNA achieves a power gain of 16.5 dB and a noise figure of 6.6 dB at 60 GHz under a power consumption of only 28 mW in 65 nm CMOS.

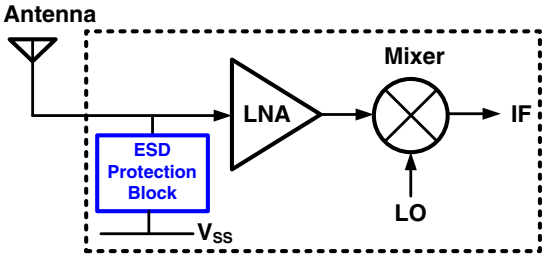

Fig. 1. (Color online) Typical RF receiver front-end including the ESD protection block connected at the RF input terminal.

2. RF ESD Protection Devices

2.1 Review of RF ESD protection devices

Various ESD protection devices for RF applications were reported. A polycrystalline silicon (poly-Si) SCR ESD device was proposed with improved Q-factor and reduced signal loss.[8] Figure 2(a) shows the cross section view of the device. The P+–N+–P+–N+ SCR structure is formed in the poly-Si layer on top of field oxide, making the noise coupling effect reduced to meet the requirements of low-capacitance ESD protection for RF applications. However, the drawback is the additional process of the field oxide formation. Figure 2(b) shows the cross section view of a poly-bounded diode (gated diode) ESD device.[9] The poly-bounded diode has no shallow-trench-isolation (STI) between the P+ and N+ diffusion, which results in a reduced series resistance. The poly gate is shorted with the cathode to reduce parasitic capacitance. Alternative to using the active ESD devices, the ESD design using inductor or transmission line were also reported.[11] A multilayer coplanar waveguide

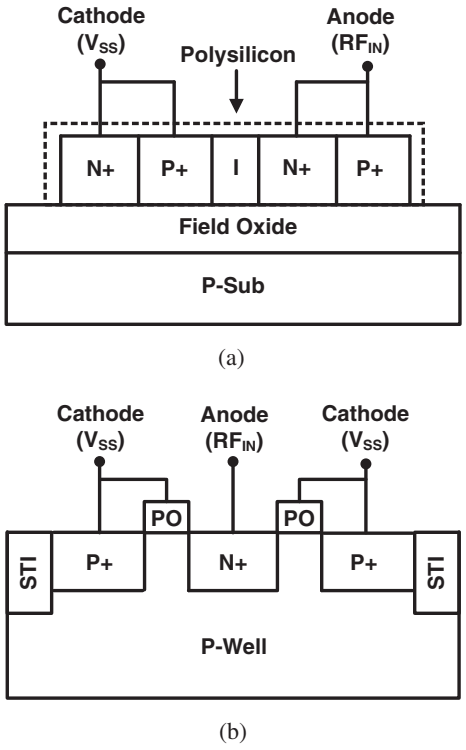

Fig. 2. (a) Cross-section view of poly-silicon SCR. (b) Cross-section view of poly-bounded diode.

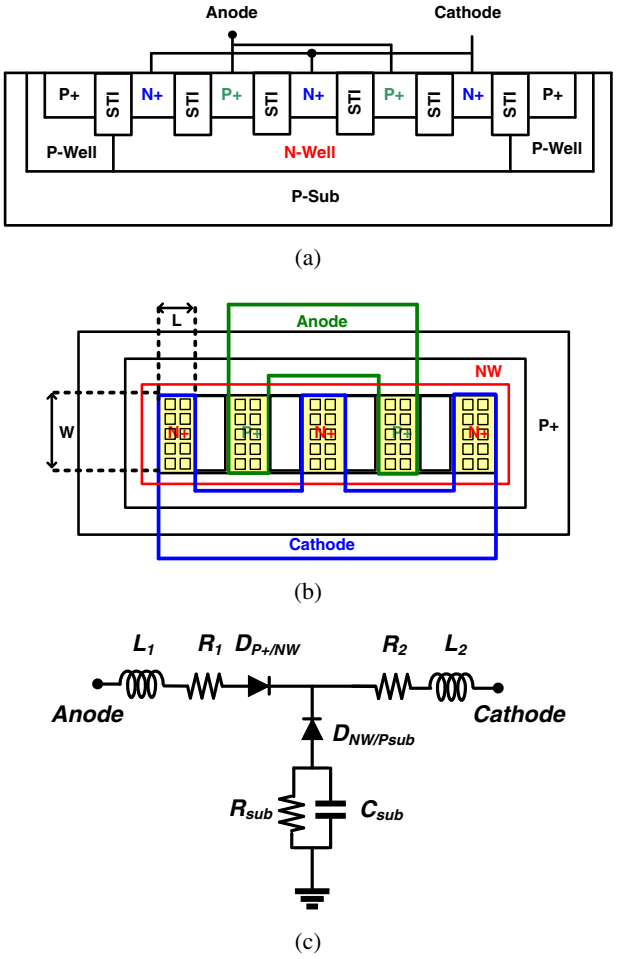

Fig. 3. (Color online) The proposed RF junction varactor for ESD protection in multi-finger topology. (a) Layout view. (b) Cross-section view. (c) Equivalent circuit model.

(MCPW) inductor L_{ESD} for grounding the ESD current was designed to tune out the pad capacitance at f_0. The inductor acts as a low-pass filter for the ESD signal, bypasses ESD current to ground, and allows the RF signal to pass to the RF core circuit (high-pass for the RF signal). The inductor can be performed by $\lambda/4$ transmission line or folded meander line. The main drawback is the inductors consume a large chip area size.

2.2 Design of RF junction varactors for ESD protection

Junction varactor usually implemented as reverse-biased p–n junction for the voltage-dependent tunable capacitor, exhibiting higher Q-factors compared to accumulation-mode MOS varactor for LC-based voltage controlled oscillator (VCO).[12] The junction varactor was also employed for tunable matching network for dynamic load modulation of high power amplifiers.[13] The junction varactor here is proposed to act as a tunable capacitor in normal RF operation (reverse bias), while functions as an ESD diode to bypass ESD current during ESD zapping (forward bias). The ESD design needs to take special considerations of small on-resistance and high failure current (I_{t2}), compared to the junction varactor design for voltage-dependent tunable capacitors or tunable matching network. When the junction varactor used as ESD protection device, the enough via number and metal width in both terminals (anode and cathode) are necessary to reduce on-resistance (R_{ON}) and prevent electron-migration issue. There is a trade-off between ESD robustness and ESD device induced parasitic. Under a fixed ESD device area, the multi-cross-finger topology of junction varactor as ESD device can handle a large ESD current with a reduced parasitic resistance and easy for metal routing, because the ESD capability is dominated by the junction edge instead of the bottom area. Note the total width of metal layers and the numbers of contact and via, along the ESD paths, determine the on-resistance (R_{ON}) during ESD zapping.

Figure 3(a) shows the cross-section view of the finger-type junction varactor with the structure of parallel connected p–n junction in the n-well for ESD protection. Figure 3(b) illustrates the corresponding layout view of RF junction varactor with a multi-finger topology. In the design of customized junction varactors, the maximum allowed contact and via density, and metal width are utilized along the ESD current path to reduce the on-resistance. Compared with the single-finger layout approach for the ESD design, the multi-finger layout can reduce the parasitic resistances and inductances owing to the parallel connected finger and reduced length of each finger for a certain total finger width. Also, the bypass current capability is enhanced since the overall junction periphery increases under a fixed device area. Figure 3(c) shows the corresponding equivalent circuit model. The $D_{P+/NW}$ models the ESD diode, the R_1, R_2, L_1, and L_2 represent the parasitic effects of the anode and cathode; and the $D_{NW/Psub}$, R_{sub}, and C_{sub} model the substrate parasitics. The multi-finger layout can reduce the parasitic resistances and inductances because of the parallel

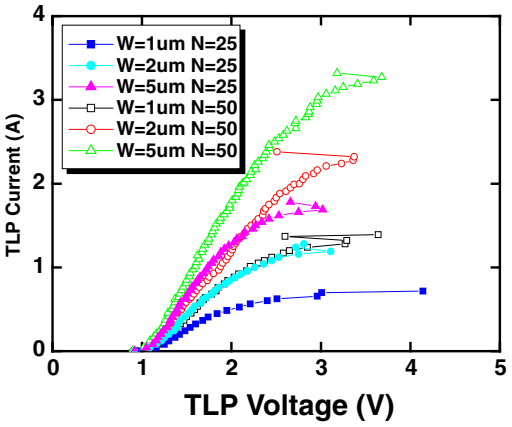

Fig. 4. (Color online) Measured TLP I–V curves with different device geometries.

connected finger and reduced length of each finger compared with the single-finger layout approach for ESD design. Also, the ESD capability is enhanced since the overall junction periphery increases under a fixed device area.

2.3 Characterization of RF junction varactors for ESD protection

The TLP measurement system is widely used for ESD characterization.[14] An ESD pulse with 10-ns rise time and 100-ns pulse width is generated to simulate the HBM ESD condition, and the DC leakage current test is performed after each ESD pulse stress to monitor the device. The secondary breakdown point I_{t2} is determined by a sudden increase of the leakage current. The relation between I_{t2} and the HBM ESD level (V_{HBM}) can be approximated as V_{HBM} (V) $\sim$ I_{t2} (A) $\cdot$ R_{HBM} (Ω), where R_{HBM} ($= 1.5\,\mathrm{k}\Omega$) is to describe the equivalent human body resistance.[14] In an effort for designing the junction varactor for ESD protection robustness, the optimization will be focused on the failure current (I_{t2}) and on-state resistance (R_{ON}) of the device. The bypass ESD current capability of junction varactor utilized as ESD device is investigated by the device width ($W = 1$, 2, and 5 µm) and finger number ($N = 25$ and 50). The minimum device length of 0.15 µm was selected to increase the total peripheral. Figure 4 shows the TLP measurement current–voltage (I–V) curves of junction varactors with different device parameters. In Fig. 5(a), for a fixed finger number (N), I_{t2} increases proportional to the device width due to the linearly reduced on-resistance. In Fig. 5(b), for a fixed device width (W), I_{t2} increases proportional to the finger number. Under the estimated HBM ESD level from TLP failure current, ESD robustness of the junction varactor increases as device size increasing with proportionally increased capacitance. Table I summarizes the ESD performance characterization results of junction varactors with different device parameters. By taking the extracted parasitic capacitance into consideration in Table I, the optimal device size of W2N25 ($W = 2\,\mu\mathrm{m}$ and $N = 25$) can be obtained, which exhibits the best FOM up to 98.1 V/fF. Further, from the equivalent circuit model shown in Fig. 3(c), as the diode size becomes larger, the increased substrate parasitic capacitance C_{sub} is correlated to the increased loss of the diode at high frequencies, which induces a low-impedance

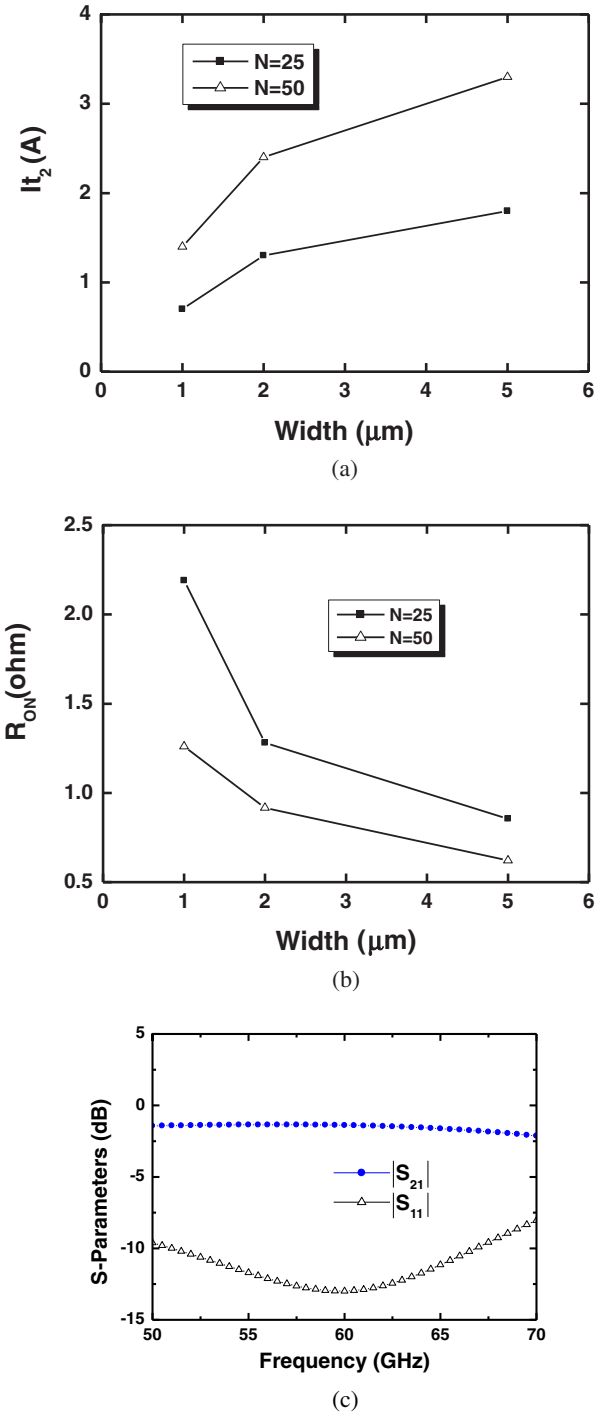

Fig. 5. (Color online) (a) Measured secondary breakdown currents of junction varactors with different width and finger number. (b) Measured on-resistance of junction varactors with different width and finger number. (c) Simulated insertion loss of the RF junction varactor (W2N25) under conjugate matching.

signal path to the substrate directly. This indicates the increased periphery of the device will ideally increase the ESD capability, however, the associate increased series parasitic resistance in both larger width ($W = 5\,\mu\mathrm{m}$) and long interconnects saturate the ESD capability and introduce additional losses. The AC characteristics of RF junction varactors are also performed by the simulation of insertion loss. Figure 5(c) shows the simulated insertion loss of the RF junction varactor (JV_{T} and JV_{B} shunted to the ground

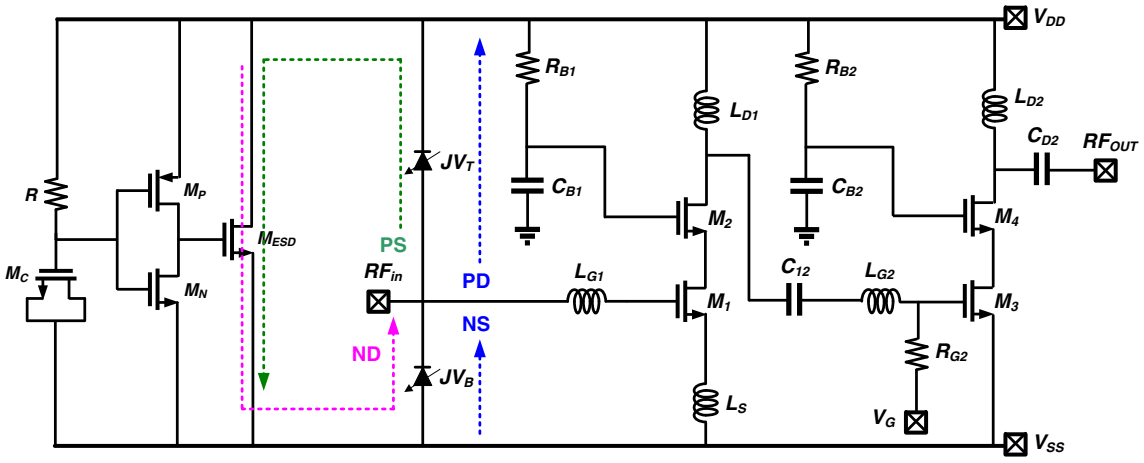

Fig. 6. (Color online) Circuit schematic of the 60-GHz LNA with diode-based ESD protection, using the RF junction varactors (JV_T, JV_B) and a power clamp.

Table I. ESD characteristics with different device sizes.

	W (μm)	L (μm)	N	I_{t2} (A)	V_{ESD} (kV)	C_{ESD} (fF)	V_{ESD}/C_{ESD} (V/fF)
W1N25	1	0.15	25	0.7	1	10.9	91.7
W1N50	1	0.15	50	1.4	2.1	21.7	96.7
W2N25	2	0.15	25	1.4	2.1	21.4	98.1
W2N50	2	0.15	50	2.4	3.6	47.9	75.2
W5N25	5	0.15	25	1.8	2.7	56.6	47.7
W5N50	5	0.15	50	3.3	4.9	118	41.5

with the size of $W = 2\,\mu m$ and $N = 25$, W2N25) with ideal conjugate matching at 60 GHz. As can be seen, the insertion loss is 1.4 dB. The extra loss will add an equivalent amount of NF to the LNA directly, as illustrated in Fig. 1. These experimental studies demonstrate that the junction varactor can be utilized for RF ESD protection design.

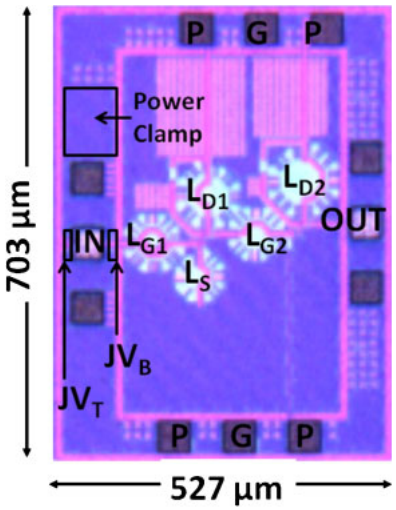

Fig. 7. (Color online) Chip micrograph of the proposed ESD-protected LNA using junction varactors.

3. Circuit Design

3.1 ESD protection network

The ESD protection network is typically a dual-diode topology, which consists of junction varactors (JV_T and JV_B) together with power clamp (M_{ESD}, M_P, M_N, R, and M_C) to complete the ESD paths (PD, PS, ND, and ND modes)[7,15] as shown in Fig. 6. The power clamp provides a low-impedance path from the power supply to ground during an ESD zap. The power clamp with gate driven topology has a low turn-on voltage, high turn-on speed, and relatively small leakage current, which is suitable for ESD design in advanced technology nodes with a small gate-oxide breakdown voltage.[16] The MOS capacitor M_C and P-type poly resistor R produce a RC time delay to ensure M_{ESD} functions correctly during an ESD event. Note that parasitic resistances and capacitances introduced by the power clamp are not that critical for the RF characteristics since this block is connected between the power rails only.

3.2 LNA configuration

The complete ESD-protected LNA is also shown in Fig. 6. The LNA employs a two-stage cascode topology. The inductive source degeneration (L_S) is used for simultaneous noise and power matching, which forms the input matching with L_{G1}, JV_T, and JV_B. Also, the inductive loads (L_{D1} and L_{D2}) are used for gain peaking and impedance matching. The capacitor C_{12} performs as the DC block between the two stages, and works together with L_{G2} and L_{D1} as the inter-stage matching. The inductor L_{D2} and capacitor C_{D2} are also utilized as the output matching network. The transistor size is determined by investigating the noise and gain characteristics as a function of finger width and bias. Note that gate terminals of M_2 and M_4 are connected to V_{DD} through RC circuits (R_{B1}, C_{B1} and R_{B2}, C_{B2}) instead of direct tied to V_{DD}, respectively, for better ESD immunity and AC ground.

4. Results and Discussion

The ESD-protected LNA was fabricated in a 65-nm CMOS GP process. This process features a gate oxide thickness of ~2 nm and a top metal thickness of 3.4 μm. Figure 7 shows the chip micrograph of the implemented 60-GHz LNA

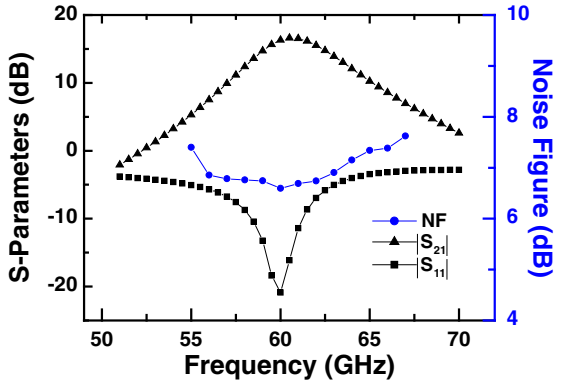

Fig. 8. (Color online) Measured NF, S_{21}, and S_{11} of the proposed ESD-protected LNA.

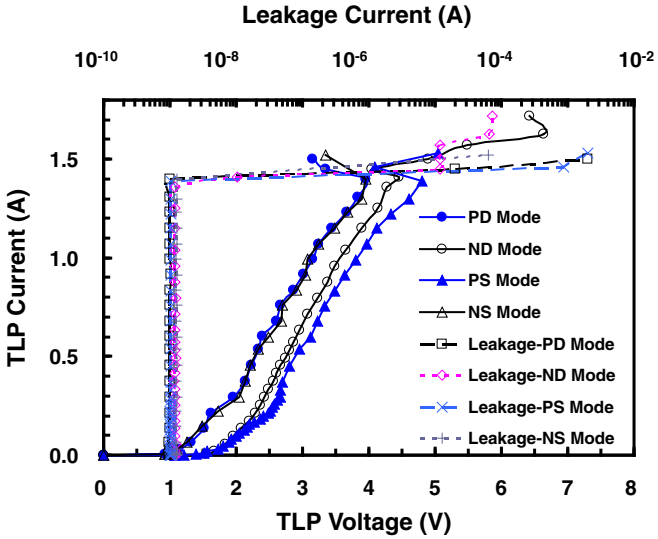

Fig. 9. (Color online) Measured TLP I–V curves of the proposed ESD-protected LNA.

with ESD protection using junction varactors. The chip of the proposed ESD-protected LNA is with an area size of $0.52 \times 0.7\,\text{mm}^2$, including the probing pads for on-wafer testing.

4.1 RF measurements

The RF characteristics were measured on-wafer using Cascade G-S-G microwave probes with a 100-μm pitch. The S-parameters and noise measurements were performed by the power network analyzer (PNA) and noise figure analyzer, respectively. The short-open-load-thru (SOLT) calibration and loss compensation have been done before the measurements. The LNA operates from a 1.0 V supply and draws a current of 28 mA. Figure 8 shows the measured S_{11}, S_{21}, and NF of the LNA, respectively. The LNA presents a peak power gain of 16.5 dB, an input return loss of 22 dB, and a NF of 6.6 dB at the center frequency of 60 GHz.

4.2 ESD testing results

Figure 9 shows the TLP test results of different testing modes (PD, PS, ND, and NS) for the ESD-protected LNA. In the PD mode, the I–V curve presents a linear characteristic, indicating the ESD bypass current enters the RF input pad and flows through JV_T to V_{DD}. The almost identical I–V curves of the NS mode and PD mode are due to the same ESD device size used for both JV_B and JV_T. In the PS mode, the I–V curve also illustrates a linear characteristic, suggesting the ESD bypass current travels through JV_T to V_{DD}, and flows to power clamp and then reaches V_{SS}. In the four testing modes, a minimum second breakdown current (I_{t2}) up to 1.4 A is achieved, corresponding to a 2-kV HBM ESD level. Note the measured TLP I–V characteristic of the power clamp is larger than 5.2 A, demonstrating the ESD performance is limited by the junction varacters (JV_T, JV_B) at RF input pad. In addition, an ESD zap tester system was employed to characterize the machine model (MM) protection effectiveness. The stress voltage starts from 25 to 500 V with voltage step of 25 V. Also, the TLP testing system has been modified for the charge-device-model (CDM) ESD protection, called very fast TLP (VFTLP). Unlike the CDM stress, which stresses one terminal of device after having charged it, the VFTLP is a two terminal test. The pulse width is reduced from 100 ns (standard TLP for HBM) to 1 ns in VFTLP, and rise time is reduced from 10 to 0.2 ns, respectively. Table II summarizes the ESD testing results of different pin combinations for different ESD models (HBM, MM, and CDM), respectively. The proposed ESD-protected LNA can achieve 2 kV HBM, 200 V MM, and a minimum VFTLP current of 4.5 A ESD level. Table III compares this work with other published LNAs at V-band, where FOM[1] and FOM[2] (including ESD protection levels) are as follows:

$$\text{FOM}^1 = \frac{\text{Gain [abs]} \times f_C\ \text{[GHz]}}{(\text{NF} - 1)\ \text{[abs]} \times P_{DC}\ \text{[mW]}} \quad (1)$$

$$\text{FOM}^2 = \frac{\text{Gain [abs]} \times f_C\ \text{[GHz]} \times \text{ESD [kV]}}{(\text{NF} - 1)\ \text{[abs]} \times P_{DC}\ \text{[mW]}}. \quad (2)$$

With low noise, high gain, low power consumption, and high ESD protection level, the proposed LNA using junction varactors achieves excellent figure-of-merits.

Table II. Summary of ESD testing results includes different models for different pin combinations.

ESD-LNA	PD	PS	ND	NS
HBM (kV)	2	2	2	2
MM (V)	200	200	200	200
VFTLP (CDM) (A)	4.8	4.6	4.5	4.8

Table III. Comparison of the proposed LNA with prior works.

Reference	This work	Ref. 4	Ref. 5	Ref. 6	Ref. 17
Technology (nm)	65	130	65	130	40
Frequency (GHz)	60	60	60	60	57–66
Power (mW)	28	65	35	54	35
NF (dB)	6.6	8.6	6.1	8.8	5.5
S_{21} (dB)	16.5	20.4	19.3	12	30
HBM (kV)	2	1.5	—	—	4
FOM[1]	4.01	1.55	5.14	0.67	21.2
FOM[2]	8.02	2.32	—	—	85.1

5. Conclusions

In this paper, an ESD-protected 60-GHz LNA was realized in 65-nm CMOS technology using the proposed RF junction varactors as the ESD devices. With the investigation on the ESD protection capability, the modified RF junction varactors were co-designed as a part of the LNA matching network. The LNA demonstrated a minimum 1.4-A TLP failure level, which is corresponding to a 2-kV HBM ESD protection. Also the LNA can achieve 200 V MM and a 4.5-A VFTLP current ESD performance. Under a power consumption of only 28 mW, the ESD-protected LNA achieved an excellent NF of 6.6 dB and a peak power gain of 16.5 dB.

Acknowledgments

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