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Interfacial trap characteristics in depletion mode GaAs MOSFETs

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Abstract

The trap-related characteristics in depletion mode GaAs metal-oxide-semiconductor field-effect-transistors (MOSFETs) were studied using two different electrical characterization techniques of current collapse and low-frequency noise measurements. With a high-quality MBE-grown gate oxide layer $Ga_2O_3(Gd_2O_3)$~30 nm thick in situ on GaAs, an extremely small drain current collapse factor ΔI_{max} of less than 5% was observed even with a high drain bias of 16 V. In addition, no kink effect was observed in the low-frequency AC *I–V* characteristics. Moreover, a normalized drain noise current spectral density in the range of 10^{-11}–10^{-9} Hz^{-1} (at 10 Hz) was obtained, which is comparable to modern 0.13-μm Si complementary MOS (CMOS) technology under similar biasing conditions. The results indicate low interfacial trap densities for the studied GaAs MOSFETs.
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1. Introduction

The GaAs metal-oxide-semiconductor field-effect-transistors (MOSFETs), due to the superior electron mobility of GaAs and the availability of semi-insulating substrates, have great advantages over their Si-based counterparts for high-speed, low-power logic integrated circuits. Compared to the conventional GaAs-based FETs, such as metal-semiconductor FETs (MESFETs) and high electron mobility transistors (HEMTs), which exhibit small forward gate voltage operation limited by the Schottky barrier, the GaAs MOSFETs allow a much larger logic swing for greater flexibility in circuit design.

The GaAs MOSFETs, after extensive pursuing over the past few decades, have been realized with a solution in the molecular beam epitaxy (MBE) grown $Ga_2O_3(Gd_2O_3)$ in situ deposited on GaAs [1–7]. A low interfacial density of state less than $10^{11}\,cm^{-2}\,eV^{-1}$, has been attained. The employment of $Ga_2O_3(Gd_2O_3)$ as the gate dielectric has led to the demonstration of the first inversion-channel GaAs MOSFET [3–5]. The DC and RF characteristics of depletion-mode (D-mode) GaAs MOSFETs have demonstrated a drain current density up to 450 mA/mm and, an f_T and f_{max} of 17 and 60 GHz, respectively [6,7].

However, the trap-related device characteristics with $Ga_2O_3(Gd_2O_3)$ as a gate dielectric, have not been reported and analyzed in detail. In this study, the current collapse and the flicker noise measurements are employed to study the trap characteristics of the interface between Ga_2O_3 (Gd_2O_3) and GaAs. A low interfacial trap density of the devices has been identified, which also provides valuable information on possible noise origins and directions to further improve the material quality and device performance.

2. Experimental procedure

The sample growth was performed in a multi-chamber MBE system, which includes a solid source GaAs-based MBE chamber, an arsenic-free oxide UHV chamber, and in situ transfer modules [1]. All chambers are connected via

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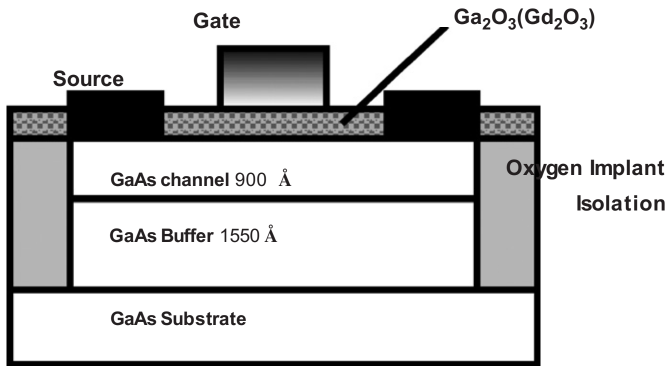

Fig. 1. The cross section of fabricated depletion-mode n-channel GaAs MOSFETs. The oxide thickness is 300 Å.

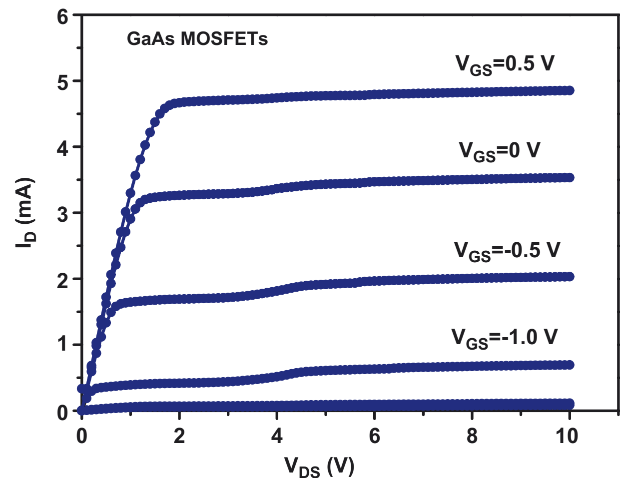

Fig. 2. The DC current–voltage characteristics for depletion-mode GaAs MOSFETs with gate length 1.5 μm and a gate width 100 μm.

UHV transfer modules where the background pressure is maintained at less than 10^{-10} Torr. Device structures, which consisted of an undoped GaAs buffer and a 900 Å GaAs channel layer with a Si doping concentration of 4×10^{17} cm^{-3}, were epitaxially grown on semi-insulating GaAs (1 0 0) substrates. After the epi growth, the sample was in situ moved to the As-free oxide growth chamber. The gate dielectric of $Ga_2O_3(Gd_2O_3)$ 30 nm thick was deposited by electron-beam evaporation from a single crystal $Ga_5Gd_3O_{12}$ garnet. The fabricated depletion-mode (D-mode) n-channel GaAs MOSFET was shown in Fig. 1. Device isolation was achieved by oxygen implantation (190 and 100 keV, 1×10^{14} cm^{-2}), followed by an activation annealing at 480 °C for 5 min in N_2 gas ambient. Prior to metal deposition, the oxide was removed using an HCl-based solution. Then, the ohmic metal AuGe/Ni/Au with thickness 500 Å/200 Å/1500 Å was deposited, followed by a 400 °C, 5 min alloying process in a N_2 ambient. The gate metal, Ti/Pt/Au (300 Å/100 Å/1200 Å), was deposited using e-beam evaporation. Finally, a post annealing at 375 °C for 3 h in forming gas ambient was used to further reduce interfacial trapped charges which were induced during the fabrication processes.

3. Results and discussion

Fig. 2 presents the DC *I–V* curves for a device with a gate width (*W*), and a gate length (*L*) of 100 and 1.5 μm, respectively. The well-defined pinch-off characteristics at $V_{GS}=-1.5$ V were demonstrated. The drain current kink was observed in the saturation region of the *I–V* characteristics, at around $V_{DS}=4$ V, which is probably due to the interfacial charges in the open unpassivated gate region [6]. In particular, a breakdown voltage higher than 10 V was measured, which is substantially higher than typical Si-based MOSFETs and excellent for high-power applications. In addition, a large output resistance above 10 kΩ was observed in the saturation region, which is also beneficial for circuit design.

The current collapse measurement of the device was performed under the sweep of a 60 Hz rectified sine wave using a Tektronix 370 curve tracer. The response of the traps was probed by the slowly changed signal, and the impact of the interface traps was observed by the *I–V* characteristics of the devices. The measured current collapse with various V_d sweeps, ranging from 4 to 16 V, is shown in Fig. 3. The collapse factor, ΔI_{max}, is defined as the ratio of the decreased maximum drain current with a V_d sweep of 16 V to the maximum drain current with a V_d sweep of 8 V. As a whole, there is no obvious drain current reduction observed, even under a very high drain bias of 16 V. The ΔI_{max}'s are all below 5% for all gate biasing conditions.

In contrast to the DC *I–V* results, there is no kink observed in the current collapse measurement. These results indicated the excellent passivation of using $Ga_2O_3(Gd_2O_3)$, the novel gate dielectric in situ deposited on GaAs surface and the low interfacial state density in the oxide/GaAs interface. Compared with the previous report [6,7], the D-mode GaAs MOSFET exhibited improved *I–V* characteristics, with negligible drain current collapse even under very high drain biases and also no kink, due to the excellent passivation.

To further study the interfacial trap characteristics of the D-mode GaAs MOSFET devices, the flicker noise measurements were also performed to reveal more about the impacts of interfacial traps on these devices. Fig. 4 shows the normalized drain noise current spectral density as a function of gate bias under $V_{DS}=2.5$ V. As can been seen, S_{ID}/I_D^2, where S_{ID} is the drain noise current and I_D is drain current, reduces with increasing the gate bias, which is due to a screening effect from the channel carriers. The increase in total channel carriers as the device was biased away from pinch-off has attributed to the monotonically reduced noise density with increasing V_G. Compared to modern Si CMOS technology, the typical normalized noise spectral density in 0.13-μm NMOS technology is in a range of 10^{-11}–10^{-9} Hz^{-1}(at 10 Hz, under similar biasing conditions) [8], which is comparable to that in the GaAs MOSFETs reported here. Note that the comparison is

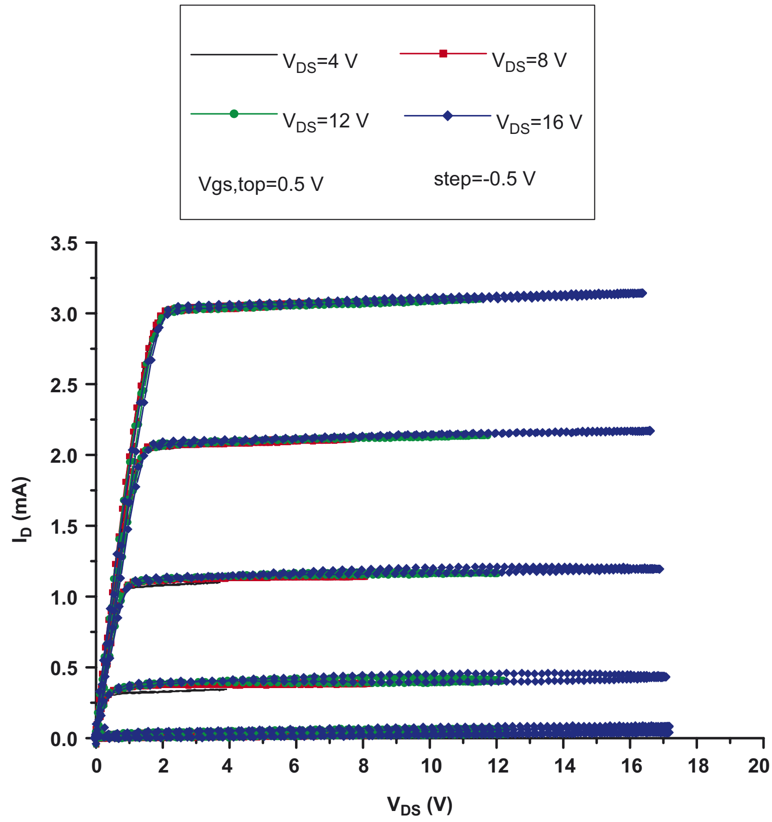

Fig. 3. The current collapse characteristics for depletion-mode GaAs MOSFETs with a gate length 1.5 μm and a gate width 100 μm.

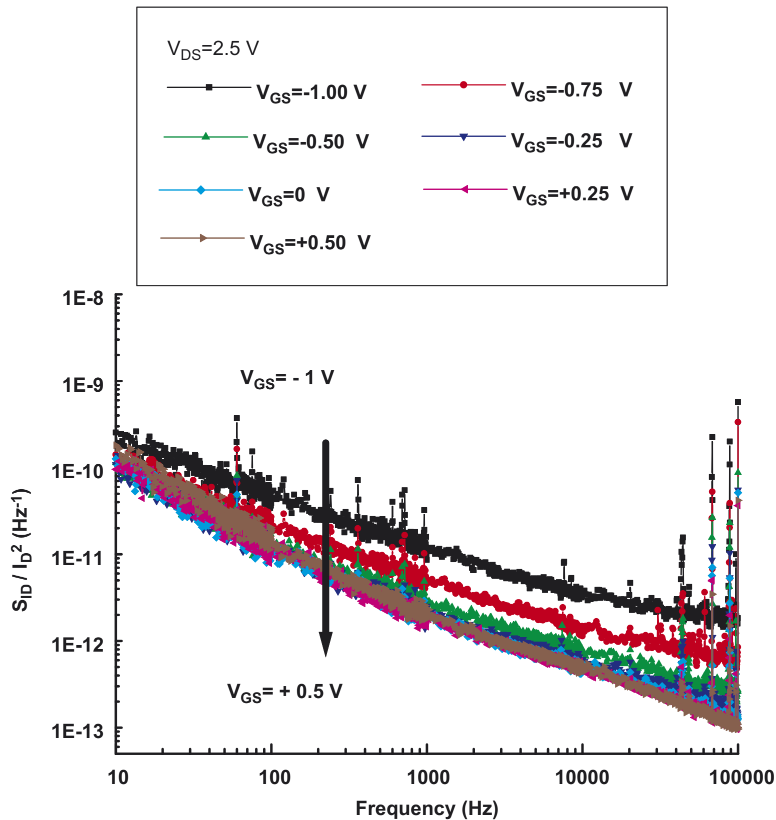

Fig. 4. The normalized drain noise current spectral density for GaAs MOSFETs with $V_{DS} = 2.5$ V and V_{GS} from −1 V to 0.5 V.

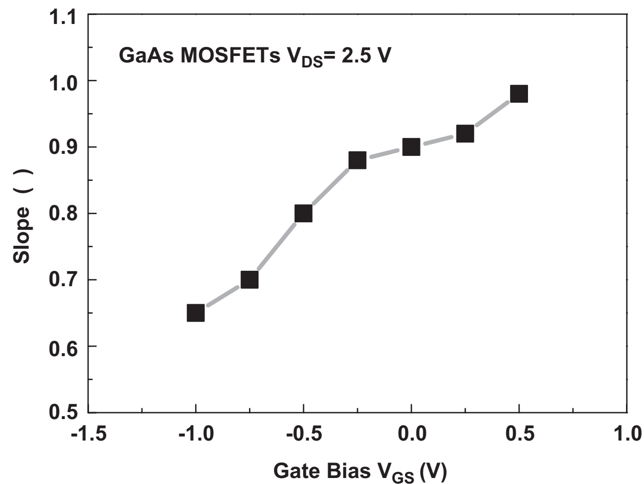

Fig. 5. The slope γ of the $1/f^{\gamma}$ noise spectral density under different gate biases. The drain terminal is biased at 2.5 V.

based on a normalized drain current level for both GaAs- and Si-MOSFETs, which minimizes the impact of the geometry introduced current difference on the noise level.

Fig. 5 plots the slope (γ) of the $1/f^{\gamma}$ characteristics as a function of the gate bias. It was found that the extracted slope values are ranged from ~0.65 to 1, and also increase with the gate bias. The results can be explained by the distribution of the traps in the device. Theoretically, the slope γ should be based on the assumption of uniformly distributed traps [9]. By employing the number fluctuation model, as the carrier tunneling distance and the trap energy are non-uniformly distributed, a gate-bias dependence of γ can be expected. The observed trend of $\gamma < 1$ reveals that the trap density increases toward the $Ga_2O_3(Gd_2O_3)$/GaAs interface. Moreover, the gate-bias dependence of γ suggests that trap distribution is also non-uniform as a function of energy. As the band bending increases with a higher gate bias, the amount of effective traps increase, resulting in an increased slope γ [9,10].

4. Conclusion

The interfacial trap characteristics of the D-mode GaAs MOSFETs were investigated. There is no kink observed in the low-frequency AC *I–V* characteristics. In addition, the current collapse measurement showed a negligible drain-current reduction, even with an applied drain bias up to 16 V. Investigation of the flicker noise characteristic showed a drain noise current density similar to that in modern CMOS technology. Studies on the bias dependence and the slope γ suggest that the main noise origin located close to the interface between $Ga_2O_3(Gd_2O_3)$ and the channel. The various measurements all indicate a low interfacial trap density for the studied GaAs-based MOSFETs. In addition, this study identified the possible flicker noise origins and locations, which provide a direction to further improve the material quality and device performance of the GaAs MOSFETs.

Acknowledgments

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